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Optimization of uLED electrical properties with AlGaIn/GaN Tunnel Junction layer

A Thesis submitted in partial satisfaction of the
requirements for the degree Master of Science
in Electrical and Computer Engineering

by

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June 2023

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June 2023

ABSTRACT

Optimization of uLED electrical properties with AlGa_N/Ga_N Tunnel Junction layer

by

Yuandong Fei

As the quest for high-efficiency light-emitting diodes (LEDs) intensifies, researchers are increasingly focusing on advanced materials such as III-Nitride semiconductors, including AlN, GaN, and InN. Despite their potential, the performance of these LEDs is often impeded by factors such as defect density, quantum-confined Stark effect (QCSE), and suboptimal light extraction efficiency. In this investigation, we explore the impact of incorporating an aluminum gallium nitride (AlGa_N) interlayer on the efficiency of III-Nitride LEDs, employing a combination of experimental and computational methodologies.

The synergy of experimental results and computational simulations reveals that the introduction of an AlGa_N interlayer significantly enhances the overall efficiency of LEDs. This improvement is achieved by ameliorating threading dislocations, attenuating QCSE, and elevating light extraction efficiency. Moreover, the interlayer facilitates superior carrier confinement and diminished electron leakage, resulting in an increased internal and external quantum efficiency [1].

By conducting meticulous lab experiments and employing sophisticated software simulations, we optimized the growth parameters of the AlGa_N interlayer, encompassing aspects such as thickness, and alloy composition. The optimized AlGa_N interlayer-based III-Nitride LED demonstrated a substantial increase in efficiency compared to its conventional

counterparts lacking the interlayer. Additionally, the AlGa_N interlayer imparts enhanced thermal stability and robustness to the LEDs [2].

This research elucidates the significance of integrating AlGa_N interlayers into III-Nitride LED structures, resulting in markedly improved device performance. The insights garnered from the experimental and computational approaches contribute to the advancement of next-generation high-efficiency LEDs, promoting sustainable and energy-efficient lighting solutions across a diverse range of applications.

TABLE OF CONTENTS

| | |
|---|----|
| 1. Introduction..... | 1 |
| 1.1. History of Application | 1 |
| 1.2. Research Motivation..... | 5 |
| 1.3. Research Objectives..... | 10 |
| 2. Simulation..... | 11 |
| 2.1. SILVACO Overview | 11 |
| 2.2. SILVACO Simulation Methods | 12 |
| 2.2.1. Simulation Parameters | 12 |
| 2.2.2. Simulation Equations..... | 14 |
| 2.2.3. Simulation Models..... | 14 |
| 2.3. Fabrication and Measurement..... | 16 |
| 2.3.1. Layer 1: Mesa | 16 |
| 2.3.2. Layer 2: 3 Terminal Pattern..... | 17 |
| 2.3.3. Layer 3: Contact Outline | 18 |
| 2.3.4. Layer 4: Metal Contacts..... | 19 |
| 2.3.5. Measurements | 20 |
| 3. Results and Discussion | 23 |
| 3.1. Fabrication Round 1: Test trial | 23 |
| 3.2. Fabrication Round 2: 15% - 20% Al composition comparison | 27 |
| 3.3. Fabrication Round 3: Electrical properties comparison of interlayers | 30 |
| 3.4. Simulation Round 1: Reduced mass AlGa _N interlayer simulation | 33 |

| | |
|---|----|
| 3.5. Simulation Round 2: Thickness and composition variation sweep | 39 |
| 4. Conclusion and Future Directions | 44 |
| 5. Reference | 45 |

1. Introduction

1.1. History of Application

Light Emitting Diodes (LEDs) have catalyzed a revolution in the field of optoelectronics, offering energy-efficient, environmentally friendly, and long-lasting light sources. These devices have gained widespread acceptance in diverse applications, such as display technology, solid-state lighting, and optical communication systems [3]. The evolution of LEDs traces back to the early 20th century, culminating in the invention of the first practical LED by Nick Holonyak Jr. in 1962, which produced light in the visible red spectrum [4]. Subsequent research has expanded the material systems for LED fabrication, thereby achieving devices that emit light across the ultraviolet (UV), visible, and infrared spectra.

The swift advancements in optoelectronics following the invention of the first LED have had a profound impact on semiconductor materials. III-Nitride compounds, comprising aluminum nitride (AlN), gallium nitride (GaN), and indium nitride (InN), have emerged as a critical category of materials exhibiting substantial potential for diverse optoelectronic applications [5,6]. Their broad bandgap, spanning from ultraviolet to near-infrared, renders III-Nitride materials apt for fabricating high-performance light emitting diodes (LEDs), laser diodes, and photoreceptors.

The groundbreaking work of Shuji Nakamura in the early 1990s led to the creation of the first high-brightness blue LED, based on GaN [7]. This marked a pivotal moment in research on solid-state lighting. The subsequent advent of white LEDs utilizing phosphor coating has further transformed energy-efficient lighting applications [8]. With the

application of phosphor coating designed to absorb specific wavelengths and emit different ones, the light transmitted through the coating combines to create an impression of white light to the human eye. This approach has facilitated the creation of visible band light sources via phosphor coating [9].

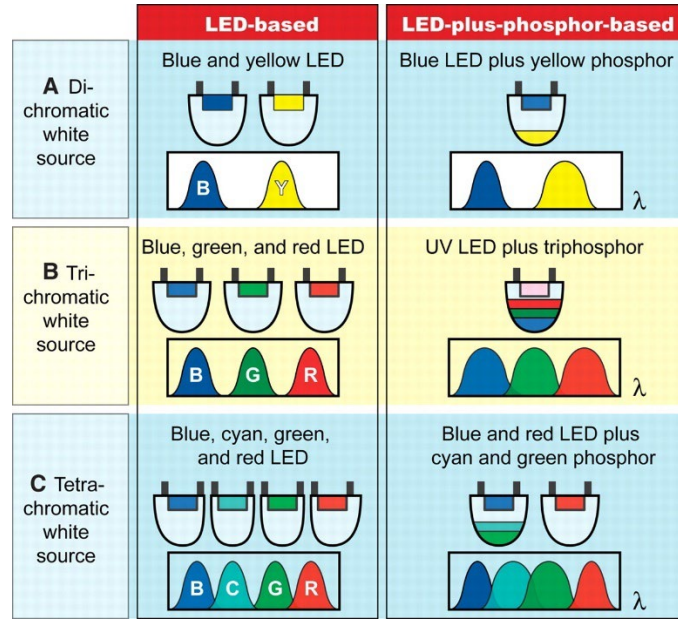


Figure 1: Multiple methods of creating LEDs which emit white light through phosphor coating. [9]

In addition to the invention of visible band LEDs, III-Nitride materials have exhibited superior performance in high-power and high-frequency electronic devices, owing to inherent properties such as high breakdown voltage, high electron mobility, and impressive thermal stability [10]. Devices constructed with III-Nitride materials, ranging from LEDs to lasers, all incorporate a p-type region necessitating magnesium (Mg) as the p-type dopant. This introduces a challenge recognized since the 1990s - the high resistivity of p-type GaN layers [11]. Under room temperature, the activation energy of Mg, the most used acceptor dopant in GaN, is approximately 200meV. This value escalates as the bandgap widens for

III-Nitride materials, reaching roughly 630meV for AlN. Consequently, devices constructed with these materials exhibit substantial inefficiency when operated at room temperature.

Apart from the issue stemming from activation energy, the growth of the crystal introduces excess, unwanted hydrogen molecules (H^+) that become trapped within the crystal, passivating the p-type GaN through binding to the Mg molecules. The growth of GaN material with Metal-Organic Chemical Vapor Deposition (MOCVD) necessitates additional post-treatment to the samples to electrically activate the acceptor dopant. Such treatments include N_2 ambient thermal annealing above 600 degrees Celsius or low-energy electron beam irradiation. These processes release the H^+ molecules from the sample, thereby increasing the resistivity of the grown GaN sample [12].

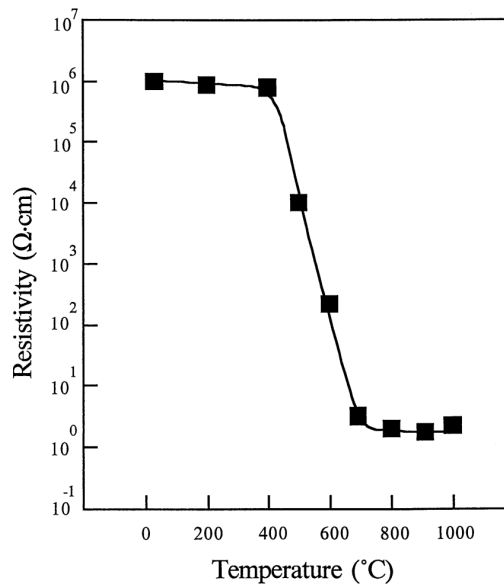


Figure 2: Resistivity of GaN film as a function of N_2 ambient annealing temperature.

[12]

Given the low electrical conductivity of p-GaN, researchers have implemented an additional layer to enhance the current flow, commonly referred to as a current spreader. Among the most prevalent current spreaders are Transparent Conducting Oxides (TCOs),

which encompass Indium Tin Oxide (ITO), Zinc Oxide (ZnO), and Gallium-doped Zinc Oxide (GZO) [13]. However, TCOs represent a significant source of electrical and optical loss within the device. Generally, TCOs exhibit higher resistivity, engendering non-uniform current spreading, current crowding, and localized heating within the device, which in turn reduces overall efficiency. Additionally, electrical losses can occur at the interface between the TCOs and the p-GaN layer. In terms of optical losses associated with TCOs, these primarily arise from absorption and reflection due to impurities, defects, or free carriers. The disparity in refractive indices between the p-GaN layer and the TCOs layer also contributes to optical losses [14].

1.2. Research Motivation

To improve upon these disadvantages, MOCVD-grown tunnel junctions (TJ) are developed as an alternative to TCOs. Tunnel junction layers can provide the same level of current spreading without the additional electrical and optical loss, with peak external quantum efficiency (EQE) 34% [15]. A tunnel junction consists of a highly doped n^{++} and p^{++} GaN layers, shown in Figure 3.

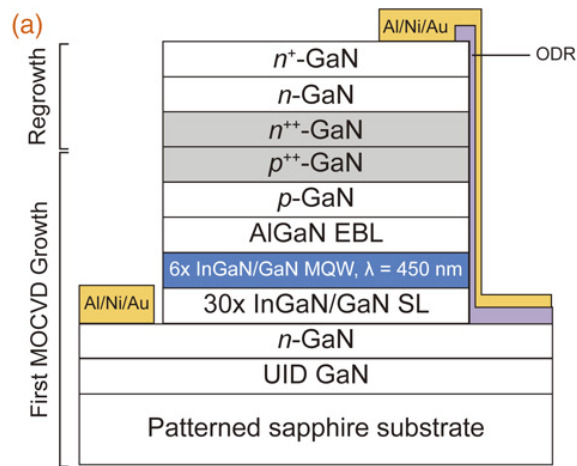


Figure 3: Cross section of a MOCVD grown uLED with GaN Tunnel Junction. [14]

(EBL: electron blocking layer, MQW: multiple quantum well, SL: superlattice, UID: unintentionally doped)

Despite this structure can improve the efficiency of the device, the hydrogen cannot diffuse through the n -type GaN due to trapping by defects in the crystal [16], which requires additional treatment to the device. This results in incomplete activation of the device, which goes back to the problem described earlier. The overall activation between layers is not as ideal as the topmost layer of the device. It can be induced that this issue would be more

problematic for large area LEDs. There have been various research aiming to resolve this issue through decreasing the LED device size [17], utilizing chemical methods to treat the sidewall to improve better hydrogen movement [18, 19], and inserting an interlayer (IL) between the tunnel junction (TJ) layers to improve the tunneling probability [20, 21]. For couple of years, people have been putting more attentions to tunnel junction interlayers (TJIL), as it could provide significant benefits without adding additional loss. This seems to be most efficient way to improve the electrical property of LED devices, since only one layer of material would be added between tunnel junctions.

Hence, the objective of our research is to explore the potential of tunnel junction interlayers in improving the performance of III-Nitride devices. It is postulated that such an interlayer might enhance the tunneling probability, an effect that could be approximated using the renowned Wentzel-Kramers-Brillouin approximation [22]. However, it is important to note that this is a hypothesis, and the actual effectiveness of this approach remains to be confirmed by our investigation.:

$$T_n = \exp\left(-2 \int_0^{x_n} \frac{\sqrt{m_e^* q^2 N_D t^2}}{\hbar^2 \epsilon} dt\right) \quad (1)$$

$$T_p = \exp\left(-2 \int_0^{x_p} \frac{\sqrt{m_p^* q^2 N_A t^2}}{\hbar^2 \epsilon} dt\right) \quad (2)$$

$$x_n = \sqrt{\frac{2\epsilon\Delta E_C}{q^2 N_D}} \quad (3)$$

$$x_p = \sqrt{\frac{2\varepsilon\Delta E_V}{q^2 N_A}} \quad (4)$$

$$T_{net} = T_n T_p = \exp\left(\frac{-4\sqrt{2m^* E} g^{3/2}}{3q\hbar\zeta}\right) \quad (5)$$

In these equations, T_n and T_p are the tunneling probability. x_n and x_p are the width of the depletion region, N_D and N_A are the donor and acceptor doping density. m_e^* and m_p^* are the effective mass of electrons and holes of the n++ region and the p++ region of the tunnel junction respectively. ΔE_V and ΔE_C are the valence and conduction band difference, ζ is the electric field applied to the device and ε is the permittivity.

Based on these equations, the net tunneling probability can be determined. It is apparent that enhancing the tunneling probability may be achieved by either reducing the bandgap or the effective mass of carriers, thereby increasing the device's tunneling probability. Furthermore, a reduction in the width of the depletion region on either the n or p side of the material, as inferred from Equations 1 and 2, can also contribute to improving the tunneling probability.

Prior research has extensively investigated the use of InGaN as an interlayer material. Given that GaN has a band gap of 3.4eV and InN has a band gap of 0.6eV, employing $\text{In}_x\text{Ga}_{(1-x)}\text{N}$ as an interlayer would result in a decreased band gap, regardless of the InN composition. This, as previously mentioned, could lead to an increase in tunneling probability. Simulations of III-Nitride devices with an InGaN interlayer have been conducted by Yan et al. [21]. Their study modeled the electrical properties of III-Nitride

devices with InN compositions ranging from 15% to 100%. Their results revealed a significant increase in tunneling current when the InN composition exceeded 25%. Additionally, empirical evidence supporting the enhanced performance with an InGaN interlayer has been provided by multiple collaborative studies [24,25].

Besides InGaN, one other ternary alloy people have focused on is AlGaN. Even though AlN has a high band gap of 6.0eV, there has been proof that the growth of AlN on GaN performs better than expected. The AlN grew by thin layer MBE demonstrates a higher polarization field, which, from the equations listed above, will increase the tunneling probability. The increment from the polarization field created by the strain between surface exceed the downside from the increasing bandgap [19, 28].

Owing to these factors, there have been few studies focusing on tunnel junction LEDs with AlGaN interlayers. In 2019, Kuroiwa et al. found that the out-of-plane effective mass could be reduced to one-tenth of its original value when a 0.04% tensile strain is applied [26]. Given this reduction in the out-of-plane effective mass, and based on the equations previously mentioned, we hypothesize that it should be possible to experimentally increase the tunneling probability. However, a challenge arises from the need for tensile strain with GaN. When InGaN thin films are grown onto GaN, the material is subject to compressive strain. Conversely, AlGaN experiences tensile strain, making it a suitable candidate for this purpose. Consequently, we posit that using AlGaN as an interlayer between tunnel junctions could potentially enhance device performance, despite AlGaN's larger band gap. This disadvantage could be counterbalanced by the benefits derived from the reduced effective hole mass.

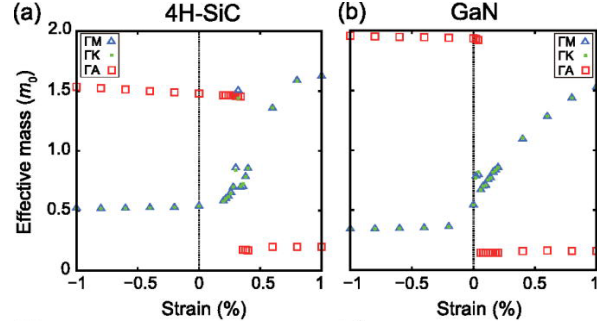


Figure 4: Hole effective mass under biaxial strain for 4H-SiC and GaN, for ΓA , the effective hole mass is $1/10$ when strained. [25]

Another advantage of using an AlGa_N interlayer, as opposed to an InGa_N interlayer, relates to the ease of implementation in laser structures. Kiyohara et al. demonstrated that VCSEL devices with InGa_N interlayer tunnel junctions suffered from high absorption losses due to the challenges associated with accurately aligning the InGa_N interlayer with the node of the optical intensity profile [23]. A misalignment of merely 10nm resulted in the internal loss from the InGa_N interlayer rising to 40 cm^{-1} from an expected 0 nm. Due to InGa_N's small bandgap, a broader range of wavelengths are absorbed, necessitating precise device growth. This increases the complexity of mass fabrication of these devices. Conversely, the AlGa_N interlayer exhibits a low absorption coefficient throughout the visible spectrum. Consequently, the absorption rate for a p⁺⁺ AlGa_N interlayer depends solely on the doping profile concentration. This suggests that the absorption from AlGa_N could be significantly lower than that from an InGa_N interlayer, given similar doping levels and thicknesses.

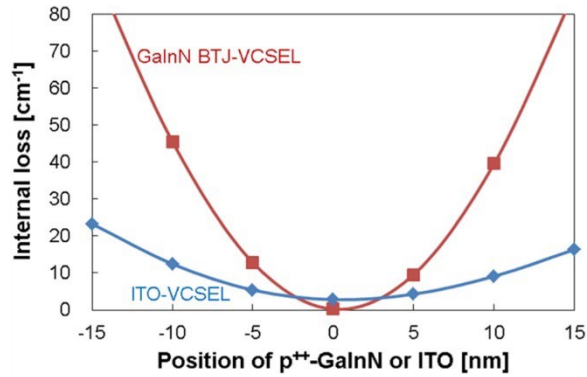


Figure 5: Internal loss of VCSEL device versus position of InGaN interlayer. [23]

1.3. Research Objectives

The primary objective of this research is to explore the potential enhancement in electronic efficiency offered by AlGaIn when deployed as a tunnel junction interlayer, compared to other materials. To this end, computational simulations were utilized to ascertain the optimal alloy composition and thickness of the AlGaIn interlayer. These theoretical predictions were then validated experimentally. Therefore, this study encompasses several specific aims.

Firstly, the research aims to demonstrate the superiority of AlGaIn tunnel junction interlayers over analogous materials in terms of enhancing electronic efficiency, utilizing industry-standard software simulations. Secondly, the study leverages simulation data to facilitate multiple experimental iterations, encompassing the fabrication of LEDs to collect empirical performance data, and to evaluate the practical applicability of the theoretical insights. Lastly, the investigation endeavors to determine the optimal AlGaIn composition and tunnel junction thickness to maximize electronic efficiency, synthesizing the findings from both simulations and experiments.

2. Simulation

2.1. SILVACO Overview

For the simulation portion of the project, we utilized SILVACO ATLAS Simulation Software to simulate the GaN tunnel junction. SILVACO, an industry-standard software, is widely employed for simulating a variety of semiconductor devices due to its advanced computational capabilities and extensive library of material properties. This allows us to integrate diverse interlayer properties into the system and obtain precise calculations. Utilizing simulation software such as SILVACO significantly expedites the LED fabrication process, traditionally a procedure that takes over two weeks. SILVACO not only provides us with a comprehensive understanding of the electrical properties intrinsic to our simulated devices but also enables us to test various conditions of our tunnel junction with the interlayer by merely altering the codes.

The primary emphasis of this research will be on device fabrication, deviating from the growth process of substrates. Regarding the simulation, our effort involves modeling the tunnel junction integrated with an interlayer within the device. This device comprises four distinct layers: an ultra-high doping concentration of GaN (n^{++} GaN), AlGa_N interlayer, heavily doped p-type GaN (p^{+} GaN), and a base p-type GaN (p GaN).

To understand the influence of the interlayer on the device and identify optimal conditions for the interlayer, the simulation will be divided into two distinct sections. The first part will investigate variations in the thickness of the interlayer, while the second will analyze changes in the composition of the AlGa_N interlayer.

2.2. SILVACO Simulation Methods

2.2.1. Simulation Parameters

The parameter used in modelling the tunnel junction in SILAVO can be summarized in

Table 1.

| Parameter | Value | Definition |
|-----------------------|----------------------------|---|
| mesh loc | | Location of mesh grid defines the position of each layer. |
| spac | 0.0001 | Spacing interval between each layer. |
| material | GaN / AlGaN | Defines material type. |
| qtregion | | Defines quantum region of the device simulated. |
| conc | 8e19 (p-GaN example) | Defines concentration of the doping region |
| model | calc.strain / bbt.nonlocal | Defines physical model used to simulate tunnel junction |
| me.tunnel / mh.tunnel | 0.254 / 0.261 | Defines electron and hole effective mass in tunnel junction |

| | | |
|---------|-------------------------|---|
| method | Newton (Newton-Raphson) | Defines methods use to solve the equations. |
| itlimit | 90 | Defines number of iterations used to solve the equations. |

Table 1: Essential parameters used in SILVACO for simulating tunnel junctions.

In SILVACO, certain crucial parameters are defined by us to ensure an accurate simulation of the tunnel junction. The location and spacing of each mesh grid are selected to be small during the interlayer and moderate at thicker layers. This approach optimizes computational resources during the simulation. The spacing at the interlayer is set at 0.0001 micrometers (0.1 nm), a value sufficiently small to accurately model the behavior of the interlayer.

Another significant factor that could influence the simulation results is the method we employ to solve the equations. Given that this simulation models each molecule within the tunnel junction, it necessitates a vast number of calculations. The methods we utilize aim to reduce the computation time by approximating the final answer, rather than solving for the exact number. We apply the Newton-Raphson method, a successive approximation method. This method uses the initial terms of the Taylor series to find the root of the equations. We can specify the number of terms and iterations of approximation needed to enhance the accuracy of the results. The number of iterations is set to 90, and the trap number is set to 70, translating to over 5 minutes of computation.

2.2.2. Simulation Equations

The equations used in SILVACO to solve for the electrical properties of the simulated tunnel junctions are shown from Equation 1 to 5. These are the major equations applied in the software for solving for electrical properties like band-to-band tunnelling probability, current across device, band diagram, and electron mobility within device.

2.2.3. Simulation Models

The example reference tunnel junction structure applied in the simulation is shown in Figure 6.

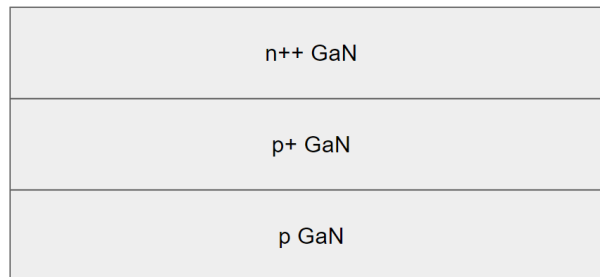


Figure 6: Example reference tunnel junction structure simulated in SILVACO (not to scale).

This is an example reference tunnel junction structure used in this research. This structure has been used before for multiple LED structures. The doping profile for these is shown in Table 2. The n++ GaN is doped with 10^{20} cm^{-3} Si, p+ GaN is doped with $8 * 10^{19} \text{ cm}^{-3}$ Mg, and the p GaN is doped with $6 * 10^{19} \text{ cm}^{-3}$ Mg.

| Type of Material | Doping Concentration (cm^{-3}) |
|------------------|------------------------------------|
| n ++ GaN | 1E20 Si |
| p+ GaN | 8E19 Mg |
| P GaN | 6E19 Mg |

Table 2: Doping profile for example reference tunnel junction.

We use the following structure for AlGa_N interlayer tunnel junction, shown in Figure 7.

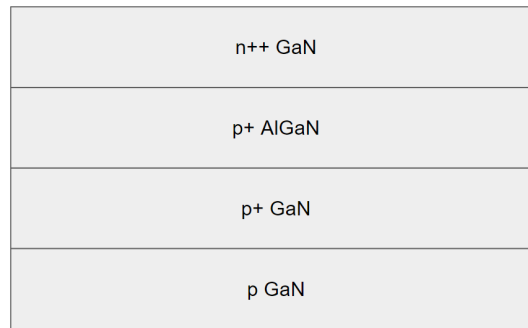


Figure 7: Example AlGa_N interlayer tunnel junction structure simulated in SILVACO
(not to scale).

Figure 7 demonstrates the example simulated tunnel junction with AlGa_N interlayer.

The doping profile for this structure is also same as listed in Table 2.

2.3. Fabrication and Measurement

In this section, the LED device fabrication process flow and the measurement specifics will be discussed.

2.3.1. Layer 1: Mesa

This layer is to develop the mesa outline of the device. It consists of a lithography process and a dry etch process.

The lithography and dry etch process is through the following steps listed in Table 3:

| | STEP NAME | PARAMETER |
|---|---------------------|---------------------------------------|
| 1 | Photoresist Coating | SPR3 with recipe 5 and 10k ramp |
| 2 | Soft Bake | 115°C for 90 seconds |
| 3 | Exposure | Heidelberg Maskless Aligner, 405nm |
| 4 | Hard Bake | 115°C for 60 seconds |
| 5 | Develop | AZ300 for 55 seconds |
| 6 | Asher | 30 seconds |
| 7 | Cl_2 Etch | RIE 5, 11 mins |

Table 3: Layer 1 lithography and etch process flow.

2.3.2. Layer 2: 3 Terminal Pattern

This layer is to develop the three-terminal pattern, which is the second layer of our LED pattern. In this layer, another mesa lithography is applied as well as the same RIE 5 dry etch process. Instead of using Cl_2 as the etchant, we are using $SiCl_4$, which has a slower etch rate around 18 nm per minute. After the standard lithography step and the dry etch step, thermal activation will be applied to the substrate to increase the hydrogen diffusion within the substrate, which would improve the electrical and thermal properties of the device. The specific parameters and steps are listed in Table 4.

| | STEP NAME | PARAMETER |
|---|---------------------|---------------------------------------|
| 1 | Photoresist Coating | SPR3 with recipe 5 and 10k ramp |
| 2 | Soft Bake | 115°C for 90 seconds |
| 3 | Exposure | Heidelberg Maskless Aligner, 405nm |
| 4 | Hard Bake | 115°C for 60 seconds |
| 5 | Develop | AZ300 for 55 seconds |
| 6 | Asher | 30 seconds |
| 7 | $SiCl_4$ Etch | RIE 5, 7.5 mins |
| 8 | Thermal Activation | Annealer, 730 °C, 1.5 hrs |

Table 4: Layer 2 lithography and etch process flow.

2.3.3. Layer 3: Contact Outline

This layer is to grow the SiO_2 dielectric layer for the LED device. This step consists of using atomic layer deposition (ALD) for SiO_2 growth and another lithography step to develop the pattern for third layer, as well as a BHF dip to remove the SiO_2 around the contacts, which will be covered with metal in the next step for testing. The specific parameters and steps are shown in Table 5.

| | STEP NAME | PARAMETER |
|---|---------------------|---------------------------------------|
| 1 | ALD SiO_2 growth | 25 nm, 300 cycles |
| 2 | Photoresist Coating | HDMS with recipe 5 and 10k ramp |
| 3 | Photoresist Coating | SPR 3 with recipe 5 and 10k ramp |
| 4 | Soft Bake | 115°C for 90 seconds |
| 5 | Exposure | Heidelberg Maskless Aligner, 405nm |
| 6 | Hard Bake | 115°C for 60 seconds |
| 7 | Develop | AZ300 for 55 seconds |
| 8 | Asher | 30 seconds |
| 9 | <i>BHF Dip</i> | 30 seconds |

Table 5: Layer 3 lithography and etch process flow.

2.3.4. Layer 4: Metal Contacts

This layer is to develop the metal contact, which is used for testing the electrical characteristics of the device. We will first go through a standard lithography and etch step to develop out the pattern we need for growing the metal at specific place. Then, a layer of titanium and gold layer will be applied to the substrate to cover the metal contact area for testing. The steps and specific parameters are shown in Table 6.

| | STEP NAME | PARAMETER |
|----|---------------------|--|
| 1 | Photoresist Coating | HDMS with recipe 5 and 10k ramp |
| 2 | Photoresist Coating | LOL-2000 with recipe 5 and 10k ramp |
| 3 | Bake | 200 °C for 5 mins |
| 4 | Photoresist Coating | SPR-3.0 with recipe 5 and 10k ramp |
| 5 | Soft Bake | 115°C for 90 seconds |
| 6 | Exposure | Heidelberg Maskless Aligner, 405nm |
| 7 | Hard Bake | 115°C for 60 seconds |
| 8 | Develop | AZ300 for 63 seconds |
| 9 | UV Ozone | 10 mins |
| 10 | <i>HCL Dip</i> | 3 mins |

| | | |
|----|-------------|----------------|
| 11 | EBeam Ti/Au | 40 nm / 400 nm |
|----|-------------|----------------|

Table 6: Layer 4 lithography and etch process flow.

Between processes, we sometimes fail to make the next step in time. In this case we put our samples in NMP solution, which is a photoresist stripper and put them in heated water to keep them free from external contamination. Also, during material growth period, we added test samples along the substrates to verify the thickness of the growth. This would allow us to calibrate the condition of the device.

2.3.5. Measurements

There are several steps along the fabrication of the device that need measurements to calibrate for errors and make sure the desired thickness of layer is satisfied.

To calibrate for the growth of SiO₂ layer, a test piece is placed with the samples into the ALD chamber, which is later measured by ellipsometry to confirm the thickness grown on the wafer. The ellipsometer used in UCSB Nanofab is shown in Figure 8.



Figure 8: Woollam Ellipsometer in UCSB NanoFab. [30]

An ellipsometer operates by generating a beam of polarized light, typically deriving its light source from a laser. This light is polarized in a known manner, either utilizing a polarizer to generate linearly polarized light or a combination of a polarizer and a quarter-wave plate to produce circularly polarized light. The polarized light is subsequently directed onto the sample at a specific angle of incidence. Upon interacting with the sample, the polarization state may alter in a way that is contingent on the optical properties of the sample, including the refractive index and the thickness of any thin films present on the surface. Following reflection (or transmission) from the sample, the light traverses an analyzer, another polarizing element. The intensity of the light post-analyzer is quantified with a detector. By juxtaposing the initial and final states of polarization, one can infer information about the optical properties of the sample. The power of ellipsometry resides in its sensitivity to minute changes in the sample, enabling the precise measurement of thin film thicknesses and refractive indices.

Our focus on the device is to measure the IV (current, voltage) characteristic of the device. Like other devices fabricated within UCSB clean room, we also test our device using the IV probe station, Figure 9.



Figure 9: IV probe Station in UCSB NanoFab. [30]

With this device, connecting the probes with a multimeter, we can measure the current response when we apply a voltage across the device. Therefore, we are able to observe whether the device functions through observing whether the LED luminesces.

3. Results and Discussion

In this section, we will discuss the results of both our simulation and fabrication.

3.1. Fabrication Round 1: Test trial

At the inception of this investigation, the potential enhancements in electrical properties provided by the AlGa_N interlayer, relative to the existing tunnel junction structure, were not entirely discernible. Similarly, it was uncertain whether AlGa_N represented the most suitable interlayer material, particularly when contrasted with alternatives such as InGa_N and ITO (Indium Tin Oxide). Consequently, an array of LEDs was fabricated with diverse interlayers to ascertain their respective impacts on LED performance. The methodological approach, encompassing both the fabrication process flow and subsequent measurement techniques, aligns with those delineated in the preceding section. The structural representation of this initial fabrication cycle, denoted as Round 1, is depicted in Figure 10.

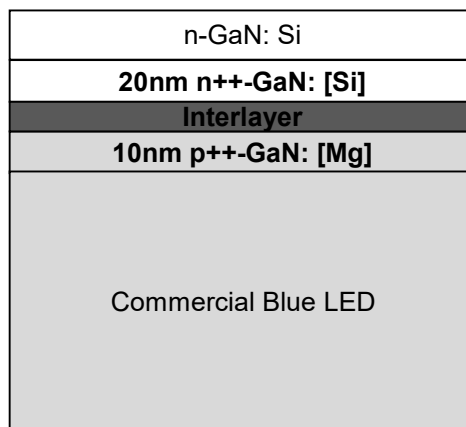


Figure 10: Round 1 LED structure with Ga_N based interlayer.

The reference LEDs are standard LED without the interlayer shown in Figure 10. Each sample contains six different sizes of LEDs, which are 5 um x 5um, 10 um x 10 um, 20 um x 20 um, 30 um x 30 um, 40 um x 40 um, and 100 um x 100 um. The structure of our LED lithography mask is shown in Figure 11.

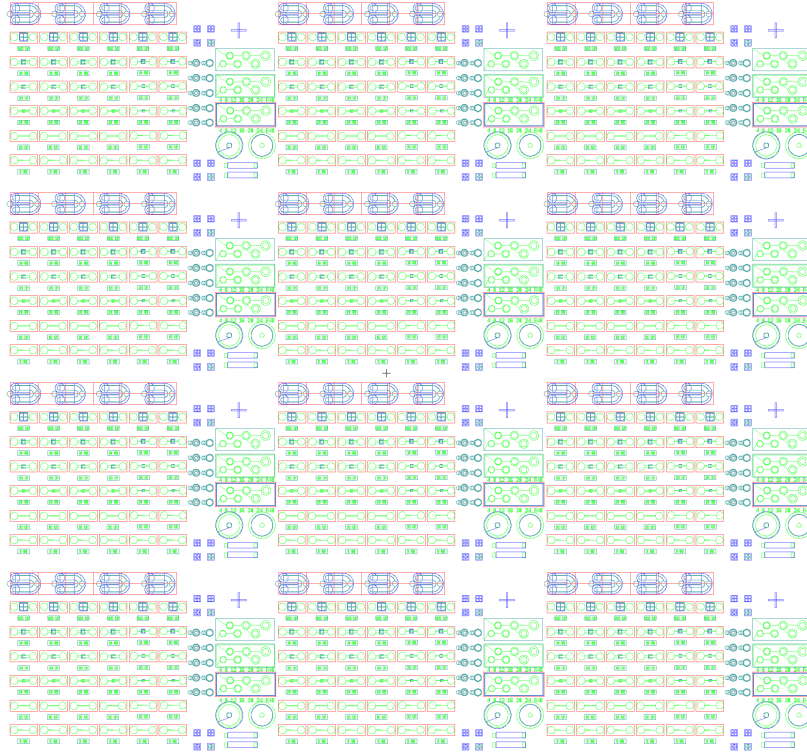


Figure 11: Structure of LED lithography mask shown in L-Edit.

The results measured are shown in Figure 12. In Figure 12, it could be seen that devices with AlGa_N interlayer, which has an Al composition of 10% to 15%, and with a thickness of 1 nm, outperforms the reference samples in all three sizes. Devices with size 10um and 20um improve greatly in voltage compared to other sizes. The voltage difference at 1kA/cm² for 10um and 20 um devices is 1V, and 1.3V for 40 um between devices with and without interlayer. However, devices with ITO outperform all the other devices greatly. The

difference between ITO interlayer devices and our best performing 10 μm devices is around 1.5 V for a current density of 1 kA/cm^2 .

We also compared the current state of the art tunnel junction [29], ones with chemical treatments, with our AlGa_N interlayer LED and reference LED. The results are shown in Figure 13.

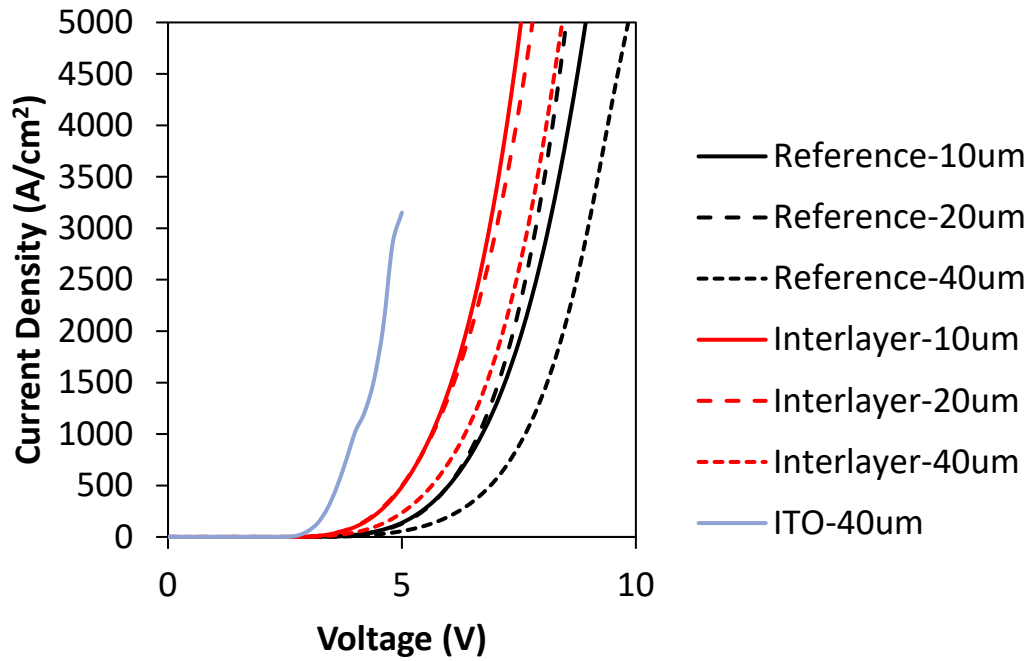


Figure 12: Current density (kA/cm^2) versus Voltage (V) plot for reference sample, AlGa_N IL sample and ITO sample for various LED mesa sizes.

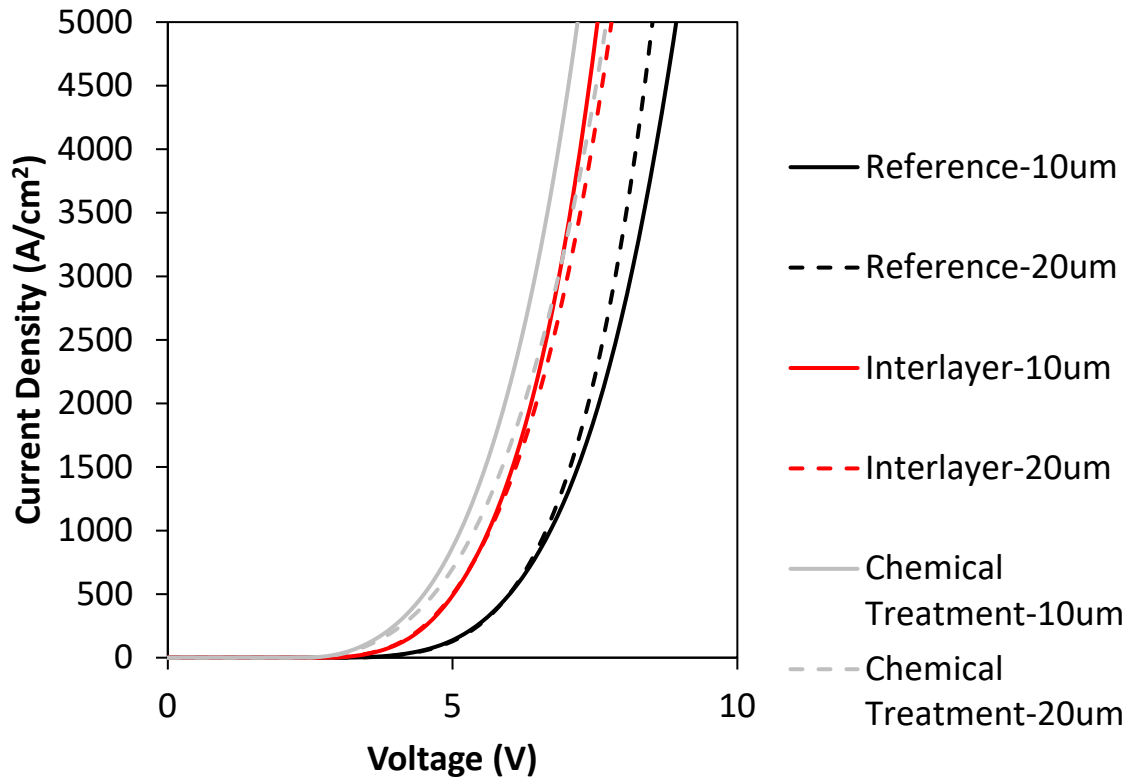


Figure 13: Current density (kA/cm^2) versus Voltage (V) plot for reference sample, AlGaN IL sample and State-of-the-art LED with TJ of various mesa sizes.

As delineated in Figure 13, devices incorporating the AlGaN interlayer initially demonstrated inferior performance compared to tunnel junction devices subjected to chemical treatment. However, an intriguing observation emerges as the current density escalates; the voltage differential between tunnel junction devices and AlGaN interlayer (IL) devices narrows significantly. In fact, at a current density threshold of 3000 kA/cm^2 , devices featuring AlGaN IL exhibit superior performance relative to their chemically treated counterparts. This initial fabrication cycle thus substantiated the potential utility of the AlGaN interlayer in augmenting the electrical performance of LED devices. The

forthcoming investigative phase will seek to identify the most efficacious composition and thickness for the AlGa_N interlayer.

3.2. Fabrication Round 2: 15% - 20% Al composition comparison

Drawing on the insights gleaned from the initial fabrication round, we confirmed the viability of incorporating an AlGa_N interlayer within our tunnel junction to enhance the electrical properties of our LED devices. Informed by these findings, we proceeded to conduct a second fabrication round predicated on the specifications derived from the first iteration. Six distinct samples were prepared, as outlined in Table 7. While the aluminum composition was not meticulously calibrated to a precise value, it varied within a range of 15% to 20%. We also fabricated devices with both InGa_N and AlGa_N interlayer to investigate whether aluminum was the key to improvement.

| Sample | Thickness (nm) |
|---|----------------|
| AlGa _N IL | 0.5 |
| AlGa _N IL | 1 |
| p-GaN | 0.5 |
| p-GaN | 1 |
| p-InGa _N + AlGa _N | 0.5 |
| p-InGa _N + AlGa _N | 1 |

Table 7: Sample characteristic and thickness fabricated in round two.

Table 7 elucidates the varying aluminum compositions of samples A, B, and C. Paired samples A1 and A2 share identical material compositions but feature divergent thicknesses of the interlayer, a characteristic also mirrored in pairs B1, B2, C1, and C2. The objective of this experimental iteration was to discern the approximate composition at which the performance of devices equipped with an interlayer would be enhanced. The outcomes of these trials are illustrated in Figure 14.

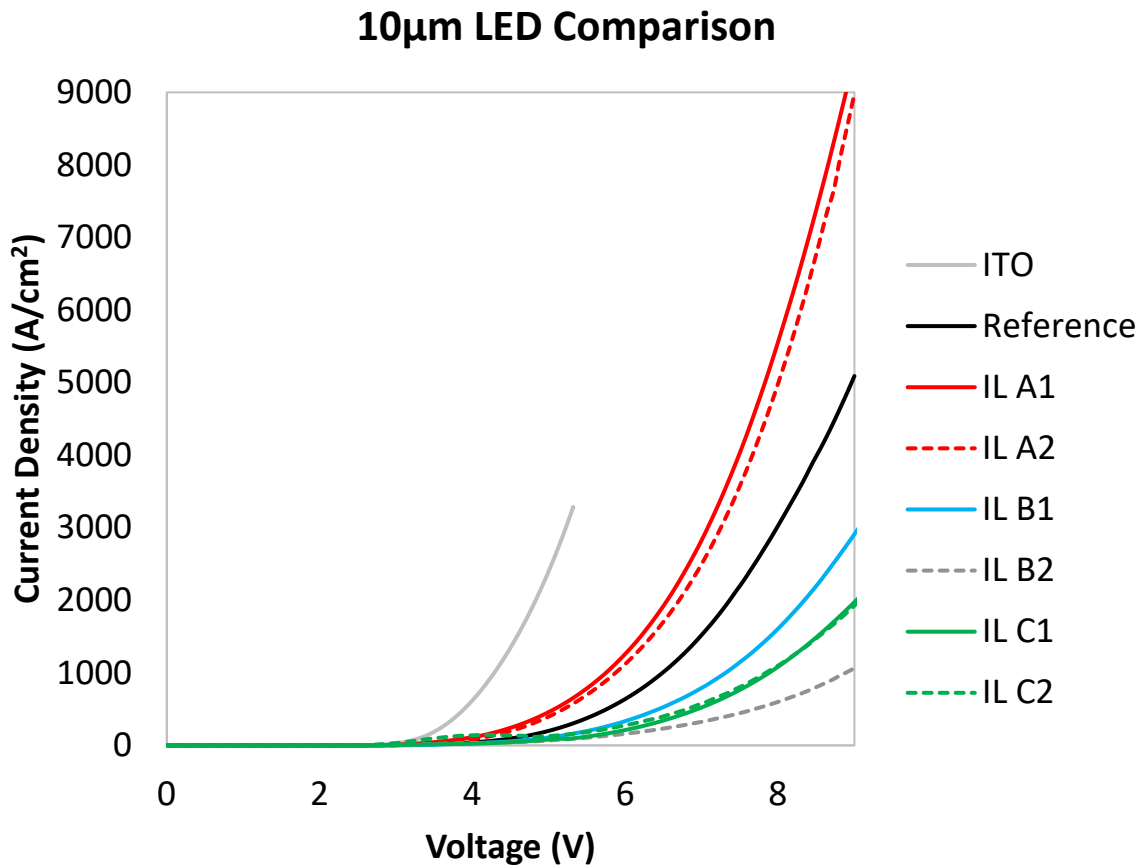


Figure 14: Current density (kA/cm^2) versus Voltage (V) for 10um LED for various samples processed in Round 2.

The empirical findings revealed that samples A1 and A2, boasting an approximate aluminum composition of 15%, displayed optimal performance. Their functionality surpassed that of the reference device devoid of an interlayer, albeit their performance remained inferior to devices furnished with an ITO interlayer. Sample B2, with a 1 nm thickness, was identified as the least effective. Notably, despite sharing an identical aluminum composition with Sample B1, B2's elevated slope resistance and discrepant thickness resulted in inferior electrical performance. This underscores the notion that variance in thickness can deleteriously affect the electrical performance of a device.

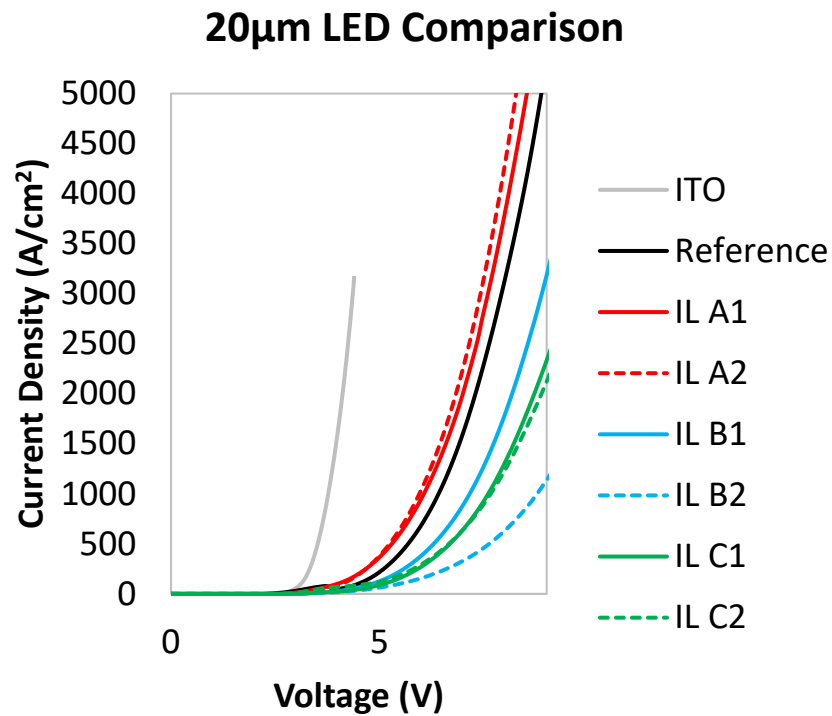


Figure 15: Current density (kA/cm^2) versus Voltage (V) for 20um LED for various samples processed in Round 2.

Figure 15 presents the outcomes for LED devices with a larger surface area of 20 μm . Notably, sample A2 outperforms sample A1 in these larger devices, albeit the difference in their performance is marginal. However, when juxtaposed with the ITO device, a substantial voltage differential at high current densities becomes apparent between the ITO devices and those with an A interlayer. There is a marked increase in slope resistance between these two categories. This disparity could be attributed to the enlargement of the depletion region, which may consequentially heighten the challenge for electrons to traverse this area.

As can be discerned from Figures 14 and 15, devices incorporating both InGaN and AlGaIn as interlayers did not exhibit superior performance compared to devices with an InGaN interlayer alone. This observation indicates that the inclusion of aluminum in the interlayer is likely to confer the most substantial performance benefits to the device.

3.3. Fabrication Round 3: Electrical properties comparison of interlayers

The second round of fabrication yielded crucial insights, namely that samples with a lower aluminum composition exhibited reduced slope resistance, indicative of superior electrical properties. Consequently, the third round of fabrication was designed to decrease the aluminum composition while maintaining the distance parameter employed in the second round. Given that a 15% aluminum composition yielded the most favorable performance in the previous round, this composition was selected for further trials. Moreover, this fabrication cycle sought to contrast the performance of the AlGaIn interlayer with that of an InGaN interlayer, and a reference GaN tunnel junction. These specifications are detailed in Table 8. The composition of the InGaN interlayer was not meticulously calibrated, resulting in an indium content ranging from 15% to 20%.

| Sample Number | Thickness (nm) | Interlayer Parameter |
|---------------|----------------|--------------------------|
| 1 | 0.5 | p+ $Al_{0.15}Ga_{0.85}N$ |
| 2 | 1 | p+ $Al_{0.15}Ga_{0.85}N$ |
| 3 | 0.5 | p+ $InGaN$ 850°C |
| 4 | 1 | p+ $InGaN$ 850°C |
| 5 | 0.5 | p+ GaN |
| 6 | 1 | p+ GaN |

Table 8: AlGa_N interlayer tunnel junction LED, InGa_N interlayer tunnel junction LED, and Ga_N interlayer tunnel junction LED processed in round 3.

As previously mentioned, the aluminum composition was chosen as 15% because the best results from round 2 fabrication was from the device with 15% aluminum composition. The current density versus voltage plot is shown in Figure 16 below.

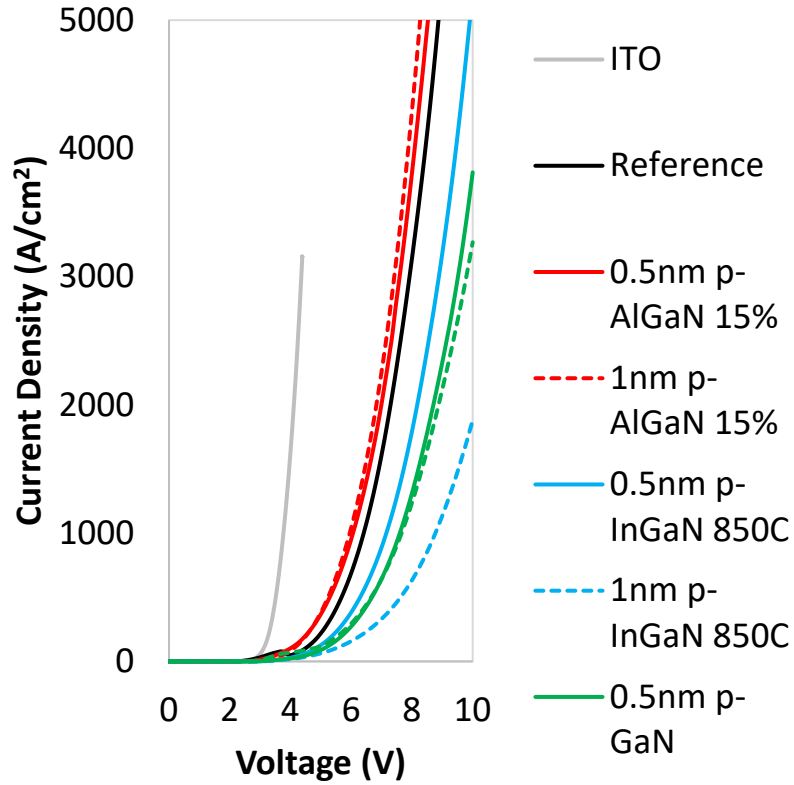


Figure 16: Current density (kA/cm^2) versus Voltage (V) for 20um LED for various samples processed in Round 3.

Figure 16 illustrates that Sample 2, featuring a 1 nm p+ $Al_{0.15}Ga_{0.85}N$, exhibits the highest performance. The current density at an equivalent voltage surpasses that of the reference sample, as well as those of the InGaN interlayer and GaN interlayer samples. Slope resistance is comparable across devices with interlayers, with the exception of Sample 4, 1 nm p+ InGaN 850 °C, although the slope resistance of the ITO interlayer is lower. A comparative analysis of the AlGaN interlayer sample against all previously processed tunnel junction LEDs reveals a consistent pattern: the AlGaN interlayer sample generally surpasses the performance of devices without an interlayer, as corroborated by Figure 17.

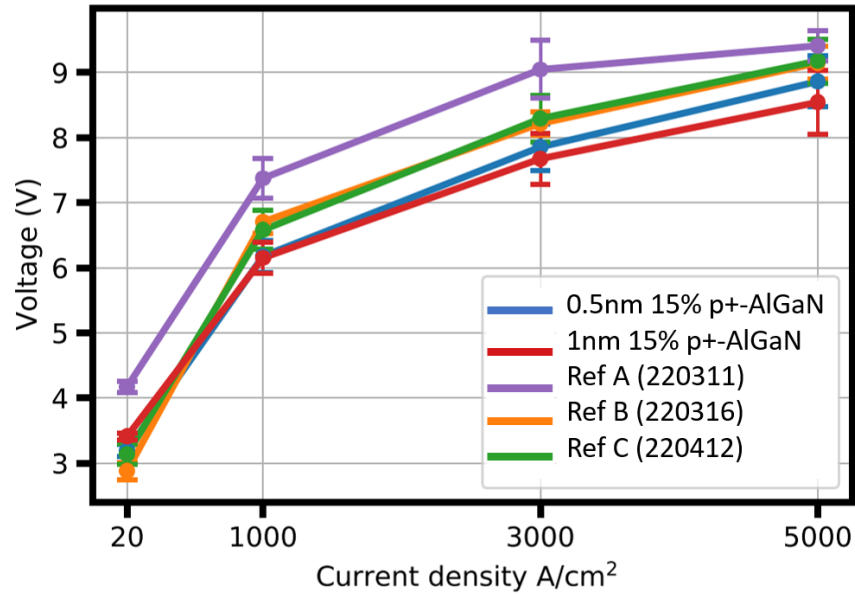


Figure 17: Voltage (V) versus current density (A/cm^2) for AlGaIn interlayer tunnel junction LED and several reference samples from previous fabrication rounds with $N = 6$.

In Figure 17, both the AlGaIn interlayer LEDs are performing better than the reference samples. The results are averages of six different devices with the same 20um size.

3.4. Simulation Round 1: Reduced mass AlGaIn interlayer simulation

Having identified the optimal composition and thickness of the AlGaIn interlayer, the subsequent investigative phase necessitates the determination of more precise parameters to maximize device performance. However, the extensiveness of the three preceding fabrication rounds, in terms of both time and effort, renders this approach inefficient for pinpointing exact specifications. As such, we elected to utilize SILVACO to simulate the device with an interlayer between the tunnel junctions. This simulation approach affords

comprehensive control over device parameters and offers significant time savings compared to the physical processing of samples.

Furthermore, from Kuroiwa et al, when the tensile strain between AlGa_N and Ga_N reaches 0.04%, the effective hole mass of the material will decrease by 1/10. This can be utilized to increase the tunnelling probability through Equation 6 and 7 [26].

$$T = \exp\left(-2w \sqrt{\frac{2m^*}{\hbar^2} E_g}\right) \quad (6)$$

$$m^* \approx \frac{m_e m_h}{m_e + m_h} \quad (7)$$

The probability of tunneling can be enhanced by reducing either the effective hole mass or the effective electron mass. In our specific context, the tunneling probability of the device sees an increase when the Ga_N is subjected to a tensile strain of 0.04%. This leads to a significant ten-fold decrease in the effective hole mass. Therefore, to conduct a more in-depth investigation of the interlayer thickness and ascertain the degree to which a reduction in effective hole mass amplifies the tunneling rate, we elected to employ simulations rather than experiments for reasons of efficiency. In this simulation phase, six distinct structures were modeled, as depicted in Figure 18. The doping profile corresponding to the materials simulated is presented in Table 2.

| No AlGaN | 1nm AlGaN, Al=6% |
|--------------|----------------------|
| n++ GaN | n++ GaN |
| 11 nm p+ GaN | 1 nm p+ AlGaN, Al=6% |
| p GaN | 10 nm p+ GaN |
| | p GaN |

| 1nm AlGaN, Al=11% | 2nm AlGaN, Al=11% |
|-----------------------|-----------------------|
| n++ GaN | n++ GaN |
| 1 nm p+ AlGaN, Al=11% | 2 nm p+ AlGaN, Al=11% |
| 10 nm p+ GaN | 10 nm p+ GaN |
| p GaN | p GaN |

| 1nm AlGaN, Al=11% Reduced m* | 2nm AlGaN, Al=11% Reduced m* |
|-------------------------------------|-------------------------------------|
| n++ GaN | n++ GaN |
| 1 nm p+ AlGaN, Al=11% Reduced m* | 2 nm p+ AlGaN, Al=11% Reduced m* |
| 10 nm p+ GaN | 10 nm p+ GaN |
| p GaN | p GaN |

Figure 18: Simulated structures for comparing AlGaN interlayer LED device with reduced effective mass.

In this simulation, the last two structure used the reduced effective hole mass of AlGaN, which can be calculated using Vegard's Law. For different composition of AlGaN, we need to find out the effective mass for each. The calculation of effective mass of the AlGaN interlayer, which is required for simulation can be calculated:

$$m^* = Y * m_{AlN} + (1 - Y) * m_{GaN} \quad (8)$$

Through this equation, we will be able to figure out the correct effective mass used for various compositions in the simulation.

The effective mass for holes and electrons for AlN and GaN is found in [27]. The effective hole and electron mass is shown in Table 8, and the simulated results are shown in Figure 19.

| Material | Hole Mass | Electron Mass |
|----------|-----------|---------------|
| AlN | 3.53 | 0.35 |
| GaN | 2.0 | 0.19 |

Table 8: Effective hole and electron mass for AlN and GaN material. [27]

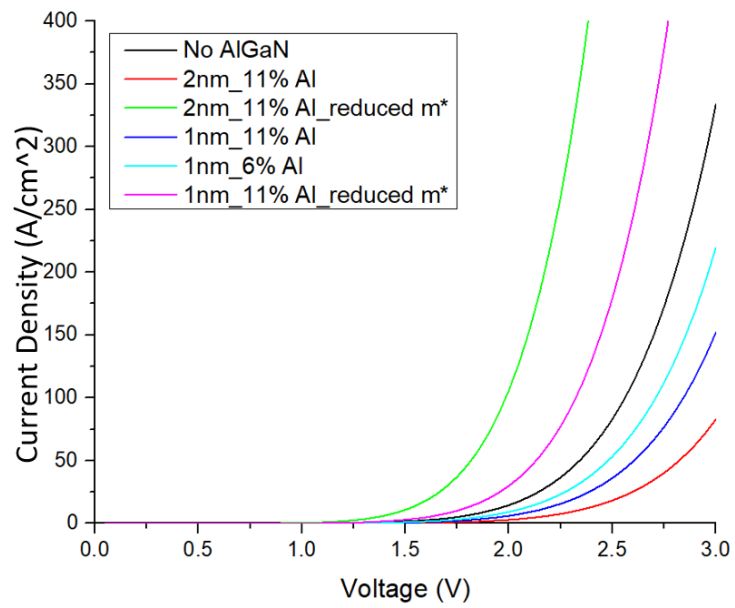


Figure 19: Current density (kA/cm^2) versus Voltage (V) for various structures simulated.

Figure 19 reveals that samples with a reduced mass demonstrate substantial enhancements in turn-on voltage and slope resistance. The most successful structure is the 2 nm $Al_{0.11}Ga_{0.89}N$ interlayer tunnel junction LED device, closely followed by the same structure, albeit with a thickness of just 1 nm. The simulation underscores the significant impact of reduced mass in augmenting the electrical properties of the device. Devices with a diminished mass display a lower voltage at the same current density relative to other devices, potentially increasing the power efficiency of the device. This aligns with the central aim of this research: to boost device efficiency while preserving a comparable electrical output power. The band diagram and electron tunneling rate are illustrated in Figure 20.

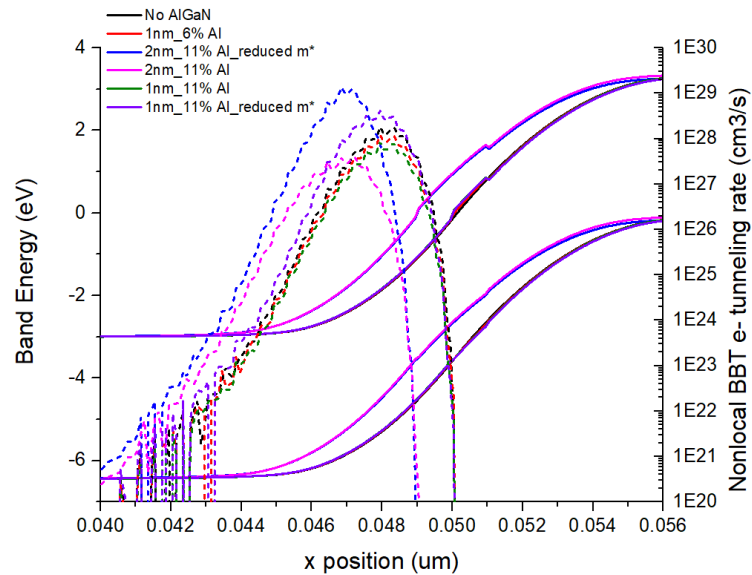


Figure 20: Electron tunneling and band diagram rate of six different structures simulated using SILVACO.

The plot features the blue and purple lines, which represent the AlGa_N interlayer with reduced effective hole mass. The non-local band-to-band electron tunneling rate for the 2 nm AlGa_N structure with reduced mass is approximately $2 * 10^{29} cm^3/s$, and roughly $8 * 10^{28} cm^3/s$ for the 1 nm structure. Both these configurations exhibit an electron tunneling rate around 7 to 10 times higher than that of the reference sample simulated, which is a Ga_N tunnel junction devoid of an AlGa_N interlayer structure. This data substantiates the influence of a decreased effective hole mass on the electron tunneling rate, which in turn affects the electrical efficiency of the device. As indicated in the Kuroiwa paper, a decrease in effective hole mass by one tenth occurs when Ga_N material is subjected to a tensile strain of 0.04%, as shown in Figure 4b. Utilizing Vegard's law, a correlation between AlGa_N and Ga_N tensile strain and AlGa_N composition can be computed. A tensile strain of 0.04% equates to an $Al_{0.01}Ga_{0.99}N$ composition. This represents the ideal aluminum composition percentage that simultaneously provides optimal electrical efficiency for the device and satisfies the 0.04% tensile strain of the Ga_N material necessary for a one tenth decrease in effective hole mass. Consequently, another round of simulations was conducted to determine the ideal thickness for the AlGa_N interlayer

3.5. Simulation Round 2: Thickness and composition variation sweep

In an attempt to establish the optimal aluminum composition and interlayer thickness, simulations were conducted under three different scenarios. The first scenario involved varying the aluminum composition in the AlGa_N interlayer from 1% to 10%. The second scenario examined the effects of varying the thickness of the AlGa_N interlayer from 1 nm to 10 nm. The device structure employed in these simulations is illustrated in Figure 21, and the doping profile is outlined in Table 2. The findings from these simulations are presented in Figures 22 and 23.

| Ref | 1nm AlGa _N , Al=X% | X nm AlGa _N , Al=3% |
|--------------|-----------------------------------|-----------------------------------|
| n++ GaN | n++ GaN | n++ GaN |
| 11 nm p+ GaN | 1 nm p+ AlGa _N , Al=X% | X nm p+ AlGa _N , Al=3% |
| p GaN | 10 nm p+ GaN | 11-X nm p+ GaN |
| | p GaN | p GaN |

Figure 21: Three different simulated structures for AlGa_N interlayer composition and thickness sweep.

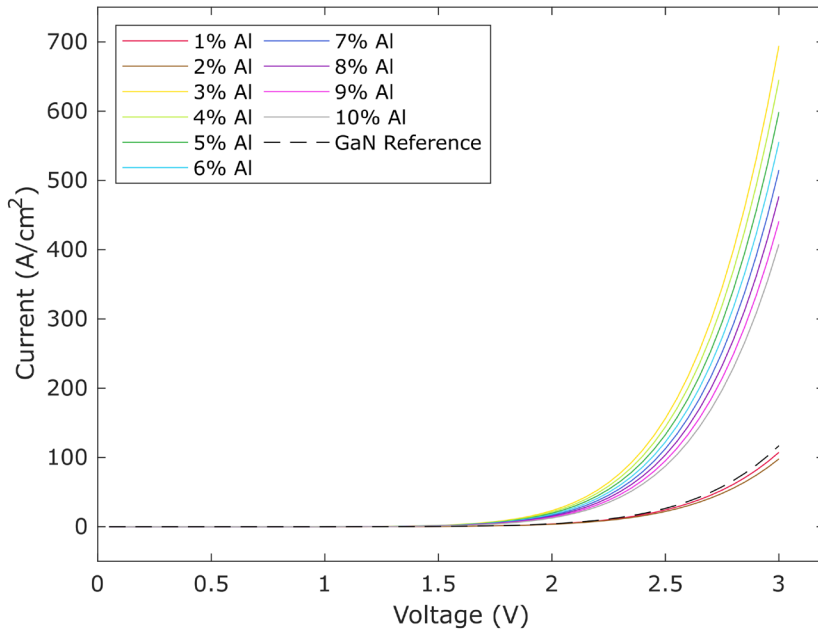


Figure 22: Current density (kA/cm^2) versus Voltage (V) for aluminum composition variation.

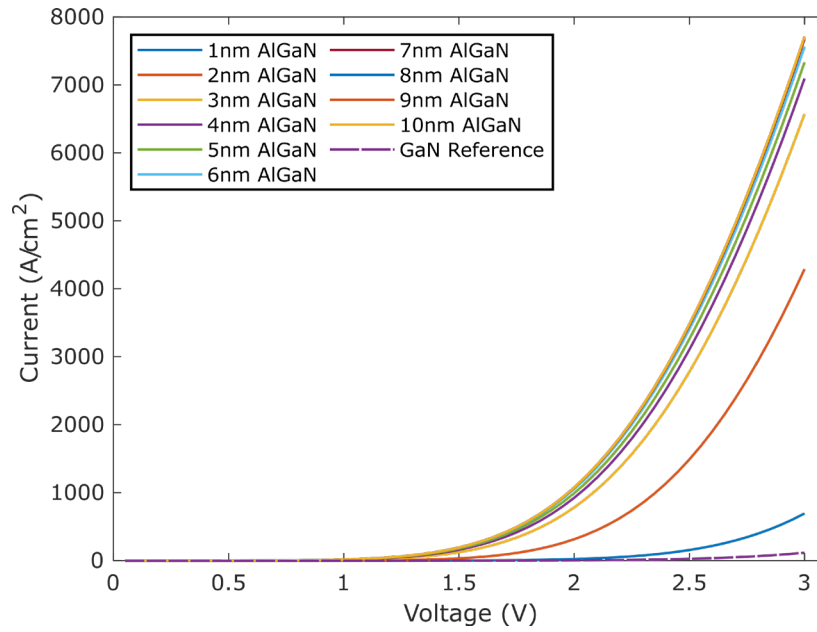


Figure 23: Current density (kA/cm^2) versus Voltage (V) for AlGaIn interlayer thickness variation.

If we plot these two figures with aluminum composition and AlGaN interlayer thickness, the optimal parameter would be visible, shown in Figure 24 and 25.

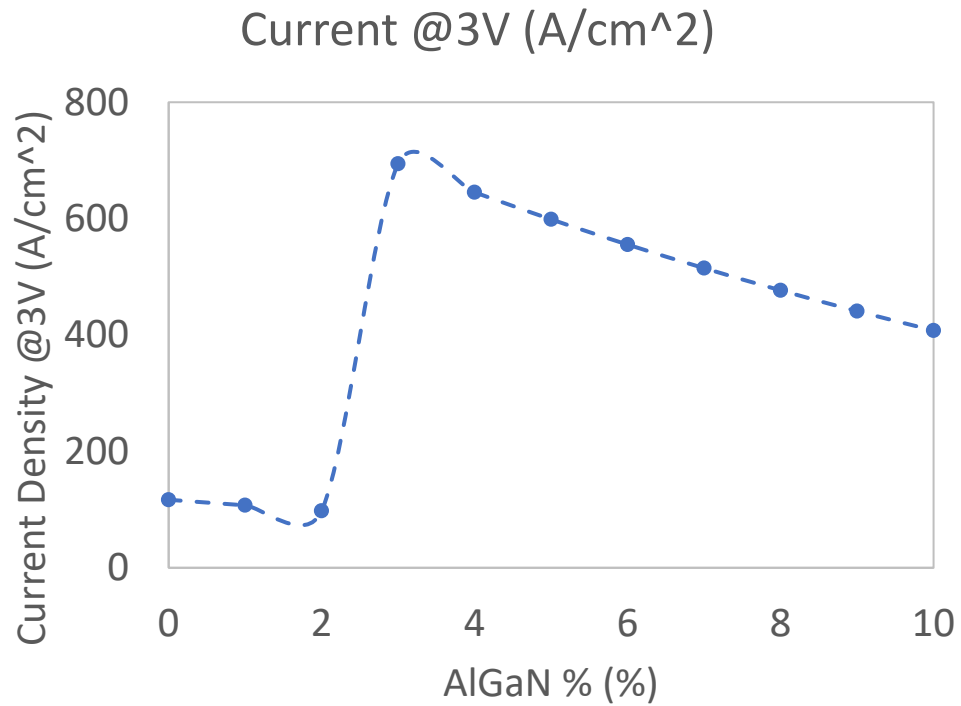


Figure 24: Aluminum composition versus current density (kA/cm^2) at 3V.

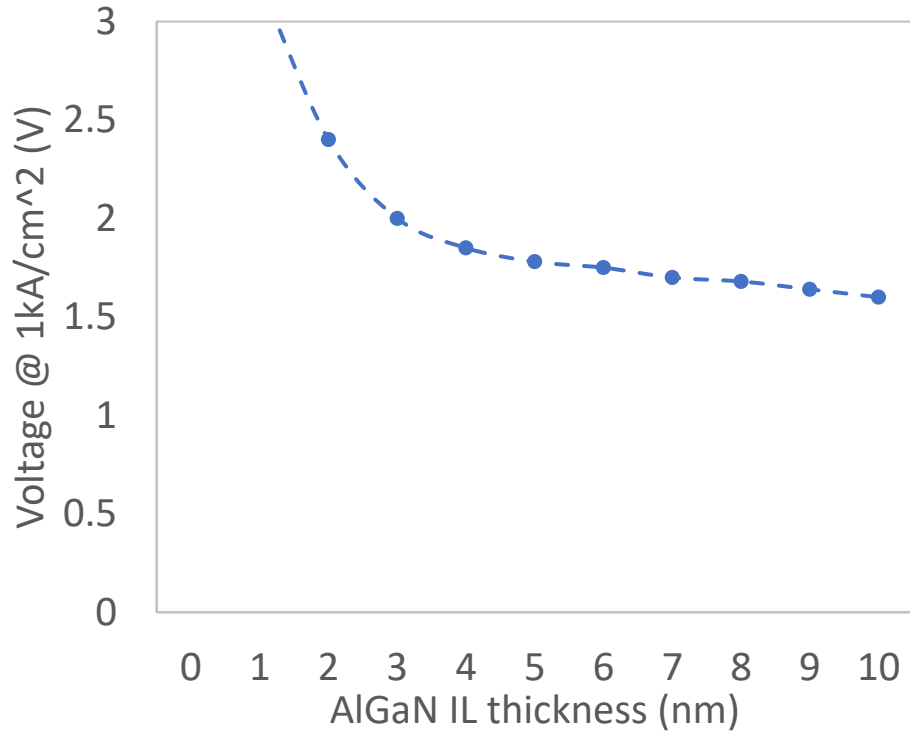


Figure 25: AlGaIn interlayer thickness (nm) versus voltage (V) at $1kA/cm^2$.

Through Figure 23 and 24, the optimal aluminum composition should be a bit over 3 percent, around 3.2%. This number is similar to what we calculated using Vegard's law using 0.04% tensile strain conversion. The optimal AlGaIn interlayer thickness should be between 3 to 10 nm, since the voltage required is smaller for the same amount of current density.

Indeed, a discrepancy was observed between the simulation results and theoretical findings from Kuroiwa et al [27]. The simulation indicated an optimal aluminum composition of approximately 3.2%, compared to the theoretical calculation of 1%. This variance could potentially stem from the specific constants and equations used during the simulation, where rounding errors might have influenced the outcome. Fabricating an AlGaIn interlayer with an aluminum composition of 1% and subjecting it to XRD analysis

presents significant challenges. For future experimental endeavors, it is noteworthy that the minimal aluminum composition that can still be analyzed using XRD is 3%. This value is closely aligned with the simulated result of 3.2%, offering a feasible avenue for verification in subsequent studies.

4. Conclusion

In the scope of this investigation, both simulated and experimental methodologies were employed to ascertain the optimal conditions for the incorporation of an AlGa_N interlayer within the Ga_N tunnel junction commonly utilized in standard LED devices. Our experimental findings, conducted over three distinct iterations, confirmed enhancements in the electrical properties of certain exemplary LED devices. Nevertheless, the prevalent trend remains inadequately defined to conclusively sway the interpretative stance of observers. Conversely, simulation outputs, derived from the use of SILVACO, facilitated the identification of an optimal composition and thickness for the AlGa_N interlayer in the devices under examination. Despite potential inaccuracies in the simulation data, attributed to the use of approximation tools to expedite computational processes, the results provided a parameter range that could be pursued for experimental validation. Regrettably, constraints related to materials and instrumentation precluded the direct experimental application of the simulated parameters, presenting an opportunity for future enhancement. Additionally, the cultivation of the substrates utilized in this investigation could potentially serve as a limiting factor. The primary objective of this research was the fabrication of the device, as opposed to substrate growth. Consequently, prospective improvements may be achieved by redirecting focus towards growth techniques and parameters. Armed with these insights, it is plausible to anticipate the experimental validation of improvements in electrical properties for devices incorporating an AlGa_N interlayer. Such advancements may pave the way for next-generation lighting solutions.

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