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Fabrication and Characterization of High Performance Silicon Nanowire Field Effect Transistors

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of the requirements for the degree of

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by

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Dedicated
to my parents

ABSTRACT OF THE DISSERTATION

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Quasi one-dimensional (1-D) field-effect transistors (FET), such as Si nanowire FETs (Si NW-FETs), have shown promise for more aggressive channel length scaling, better electrostatic gate control, higher integration densities and low-power applications. At the same time, an accurate bench-marking of their performance remains a challenging task due to difficulties in definition of the exact channel length, gate capacitance and transconductance. In 1-D Si FETs, one also often observes a significant degradation of their mobility and on/off ratio. The goal of this study is to implement the idea of the FET performance enhancement while simultaneously performing a more rigorous data

extraction. To achieve these goals, we fabricated dual-gate undoped Si NW-FETs with various NW diameters The Si NWs are grown by Au-catalyzed vapor-transport For our top-gate NW-FET, the subthreshold swing was determined to be 85-90 mV/decade, whereas the best subthreshold swings for Si NW-FETs until now were ~135-140 mV/decade. We achieved a ON/OFF current ratio of 10^7 due to improved electrostatic control and electron transport conditions inside the channel. This is on the higher end of any ON/OFF ratios thus far reported for NW FETs The hole mobility in our NW-FETs was around 250–400 cm^2/Vs, according to different extraction procedures. In our mobility calculations we included the NW silicidation effect, which reduces the effective channel length. We calculated the top gate capacitance using Technology Computer Aided Design (TCAD) Sentaurus simulator, which gives more accurate value of capacitance of the NW over any analytical formulas. Thus we fabricate and rigorously study Si NW's intrinsic properties which are very important for digital logic circuit application. In the second part of the study, we carried out simulation of Si NW FET devices to shed light on the carrier transport behavior that also explains experimental data.

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Chapter 1
Introduction

1.1 Historical Perspective

The invention of solid state transistor and the further development of silicon based integrated circuit fabrication techniques have led to unprecedented levels of growth in the semiconductor industry in the past decades. In the past years the scaling of transistor to smaller dimensions has led to a phenomenal improvement in the device performance in terms of speed, energy efficiency and chip area. This shrinkage of component size and subsequent increase in the number of components on the chip was first predicted by Gordon E. Moore [1] in 1965 and was predicted to last a decade. Beginning in 1975 this slope changed to doubling every 18 months or a fourfold increase every three years. This trend came to be known as Moore's law and is still the central guide to the semiconductor industry. With exceptional developments in processing techniques, mainly in photolithography, Moore's law has proved its validity well into the 21st century. Moore's law has yet to be violated but fundamental thermodynamic limits are being reached in critical areas and innovative changes need to be made both in basic transistor materials and device structures so that the current rate of improvement can be maintained.

1.2 Motivation for Scaling

The central idea to scale down device feature is to increase its intrinsic speed which is related to its effective gate length L_g ,in addition to accommodate more and more transistors in limited real estate of the chip. For digital circuits, a figure of merit for MOSFETs for unloaded circuits is *CV*/*I*, where *C* is the gate capacitance, *V* is the voltage swing, and *I* is the current drive of the MOSFET [2]. For loaded circuits, the current drive of the MOSFET is of paramount importance.

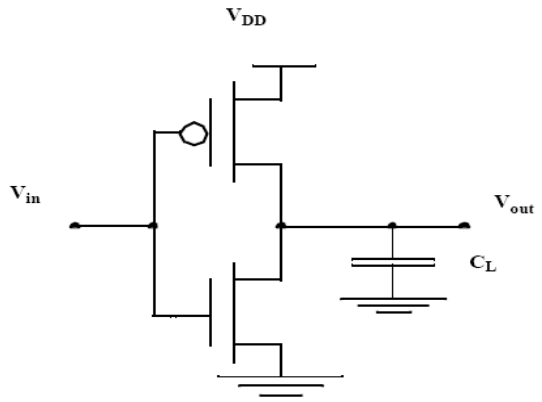

Figure 1.1: Simple Inverter circuit implemented with CMOS technology.

Keeping in mind both the *CV*/*I* metric and the benefits of a large current drive, we note that device performance may be improved by 1) inducing a larger charge density for a given gate voltage drive; 2) enhancing the carrier transport by improving the mobility,

saturation velocity, or ballistic transport; 3) ensuring device scalability to achieve a shorter channel length; and 4) reducing parasitic capacitances and parasitic resistances. These options generally fall into two categories: new materials and new device structures. In many cases, the introduction of a new material requires the use of a new device structure, or vice versa better understood in order to advance the technology.

1.3 Background of Nanowires

The success in device scaling is imperative for maintaining the successive and longlasting improvements in IC technology. As the MOSFET channel length enters the nanometer regime, however, short channel effects (SCEs), such as threshold voltage (*VT*) roll-off and drain-induced-barrier-lowering (DIBL), become increasingly intolerable, which hinders the scaling capability of planar bulk or silicon-on-insulator (SOI) MOSFETs. At the same time, the relatively low carrier mobility in silicon (compared with other semiconductors) may also degrade the MOSFET device performance (e.g., ON-current and intrinsic device delay). For these reasons, many novel device structures and materials such as silicon nanowire transistors [3] [4], carbon nanotube FETs [5] [6], new channel materials (e.g., strained silicon, pure germanium) [7] [8], molecular transistors [9], et al. – are being extensively explored. Among all these promising post-CMOS structures, the silicon nanowire transistor (Si NW) has its unique advantage – the Si NW transistor is based on silicon, a material that the semiconductor industry has been working on for over forty years; it would be really attractive and lucrative to stay on silicon and also achieve good device metrics that nanoelectronics provides. Hence, the

silicon nanowire transistor has obtained vast attention from both the semiconductor industry [10] [11] and academia [3] [12] [13]. According to the fabrication technology, recently reported Si NWs can be categorized into two groups: 1) The first-type SNWTs can be described as 'narrow-channel' SOI MOSFETs made by using a traditional 'top-down' approach [10] [11] [12] [13] [14] [15]. Distinct from planar SOI FETs, the channel (Si body) widths of Si NWs are lithography-defined and comparable to the Si body thicknesses, so the gate stacks can be made to wrap around the wire channels to realize multi-gate or gate-all-around FETs, which gives better gate control than planar MOSFETs [4] [13] [16]. In present experimental Si NW structures [10] [11] [12] [13] [14] [15], the wire dimensions such as Si body thickness and width range from 10nm to 100nm. At the scaling limit, where the device gate length is would be shorter than 10nm [17], this dimension has to be scaled down to the sub-10nm regime to maintain good electrostatic integrity. [4] For this, very-high resolution lithography (e.g., <5nm) is necessary to define the nanowire widths. Therefore, the ultimate scaling of the top-down Si NWs could be limited by the highest resolution of lithography that can be achieved in practice. It should also be mentioned that the minimum lithography-defined length in the circuits based on the top-down Si NWs should be the Si NW channel (Si body) width instead of the transistor gate length. 2) To avoid very-high-resolution lithography in the Si NWs fabrication, a number of experimental groups [3] [18] [19] [20] [21] [22] [23] are trying to synthesize semiconductor (e.g., Si, Ge, GaN) nanowires by using 'bottom-up' approaches, such as the Vapor-Liquid-Solid (VLS) growth technique [19] [22] [23]. With this technology, single-crystal Si nanowires with a diameter as small as 2-3nm have been

achieved. [19] [20] Based on these bottom-up nanowires, various types of devices and circuit components have been experimentally demonstrated, e.g., field-effect transistors (FETs) [3] [18] [24], logic gates [26], memory [27], decoders [28], nanowire heterojunctions [22] [23] [25], bipolar transistors [29], thin-film transistors [30], light emitting diodes (LEDs) [31], lasers [32] [33], photodetectors [33], and nanosensors [33]. For the FET application, in particular, the bottom-up technique offers a possible, low-cost solution to achieve nanowires with ultra-small diameters and relatively smooth interfaces, which are essentially important for scaling the transistor gate length below 10nm.

In brief, the rapid progress in nanofabrication technology has shed light on the potential use of silicon nanowire transistors in future electronics.

1.4 Outline of the Thesis

This thesis is divided in five chapters. The first chapter discusses the historical background of CMOS technology and lays the foundation of scaling. It also deals with the background of nanowire.The second chapter describes the literature review on nanowire mostly. Its starts with some discussion on commonly used terms to characterize a FET device. The third chapter elaborately describes about the growth and fabrication of silicon nanowire FET devices. It also shed light on some common issues that could potentially fail device fabrication.The fourth chapter discusses on electrical characterization of NW FET, mobility and other properties extraction. The fifth and final chapter gives the concluding thought about the accomplishment of the Dissertation.

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Chapter

Literature Reviews

2.1 Introduction

Traditional Planar MOSFETs have been going through an steady down scaling in terms of device channel length since its inception [1]. Moore's Law [2] has been dictating the downscaling roadmap for years until now. Over this period of time, the physical channel length of MOSFETs have been scaled down from 100 μm to 20 nm [3], the later refers to the channel length in commercial IC chips expected to be in the market by the end of 2011.Owiing to improvement of their performance such as faster intrinsic speed and low power consumption, MOSFETs have taken the instrumental place to lead IC industry for high performance application.

According to ITRS [3], by the year of 2015, the channel length of MOSFETs is projected to be less than 10 nm. Following Moore's law is being difficult for these upcoming technology nodes, where the main challenging point for device scaling is the off-state leakage current [4]. Planar MOSFETs with gate length as short as 5 nm has been demonstrated [5] , however owing to huge off-state current, they are not feasible for future ICs. The limitation of the downscaling of single gate, planar bulk MOSFETs is the inherent poor electrostatic control of the gate over the channel, poor transport properties of carrier. Therefore it is imperative to do intense and novel research in academia and industry to find out solution that encompasses materials to new architecture for future technology nodes before we exhaust current ones.

Scaling is further upheld by changing the device architecture from planar bulk to silicon-on-insulator (SOI) technology. Ultra-thin body SOI MOSFETs shows better performance over traditional bulk MOSFETs [6]. The electrostatic of the nanoscale length CMOS devices dramatically enhanced when additional gates are introduced such as FinFET [7] , tri-gate [8], dual-gate [9]. Due to the improvement of short channel effect of non-planar devices, one of these devices will replace current bulk planar MOSFETs architecture for future nodes. The screening length for planar and nanowire FETs can be

$$\lambda = \sqrt{\frac{\varepsilon_{ch}}{\varepsilon ox} d_{ox} d_{ch}} \tag{2.2}$$

$$\lambda = \sqrt{\frac{\varepsilon_{nw} d_{nw}^2 \ln(1+\frac{2d_{ox}}{d_{nw}})}{8\varepsilon_{ox}}} \tag{2.3}$$

expressed by the equation 2.2 and 2.3 respectively. In order to avoid short channel effectgate length L_g should be at least greater than four time higher of screening length λ .It can be shown for 8 nm thick SOI planar device with 1 nm of SiO_2 as gate, dielectric screening length is 5 nm which suggests minimum gate length to be 20 nm where as for same geometry such as 8 nm diameter NW with 1 nm SiO_2 gate, screening length turns out to be 2.3 nm which suggests minimum gate length to be 9 nm. This is a practical example how better electrostatic control helps to scale down a device without sacrificing short channel effect behavior.

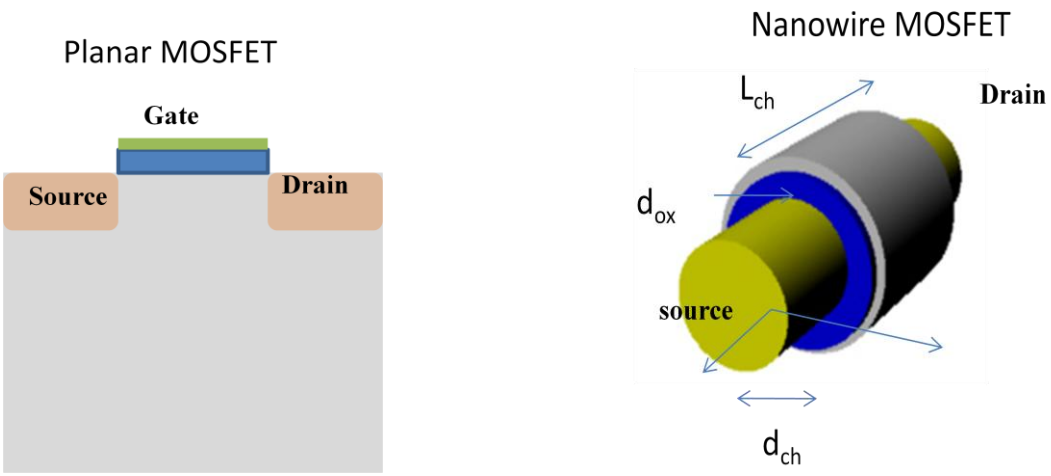

Fig 2.1: (left) geometry of a planar bulk MOSFET and (right) geometry of a NWFET device.

The Moore's law will survive if the gate insulator scaling, which is reduced to 1.2 nm in 65 nm technology node, can be made reliable. Further reduction in thickness of oxide results in severe degradation in reliability and exponential increase in tunneling current through gate dielectric. Intel has implemented innovative high-κ that replaces SiO_2 and metal gate which replaces highly doped poly silicon [10] to overcome these issues and pushed the scaling limit to 32 nm.

In this chapter, I will discuss various aspect of nanowire, their growth mechanism techniques, characteristics and potential application. I also discuss some electrical characteristic of MOSFET devices, crucial for electronic application such as mobility, subthreshold swing, on-off ratio and benchmarking techniques for CMOS devices.

2.2 Intrinsic Properties of FET Devices

Carrier mobility (μ) is an important parameter in determining device performance in electronics. It is vital for describing the operation of semiconductor devices such as a MOS transistor. It is one of the important input parameters for expressing electrical current in devices. Here by carrier mobility we mean the electron mobility μ_n and hole mobility μ_p .Mobility is an important parameter for carrier transport as it describes how strong the motion of an electron or a hole is influenced by an applied electric field.

The electrons (or holes) in a semiconductor move rapidly in all directions at room temperature. In the absence of an applied electric field, the carrier exhibits random motion and carriers move quickly through the semiconductor and frequently changes direction. When an electric field is applied, the random motion still occurs but in addition to that, there is on an average motion along the direction of the field. Due to their different electronic charge, holes move on in the direction of the electric field while electrons move in the opposite direction

The random motion of electrons leads to zero net displacement of an electron over a sufficiently long period of time. The average distance between collisions is called the mean free path and the average time between collisions is called the mean free time (τ_c).For the typical value of $1x10^{-5}$ cm mean free path, the mean free time (τ_c) is about 1 ps (~ 10^{-12} s) On application of a small electric field (E) on the semiconductor sample, each electron experiences a force –qE along the field (in the opposite direction of the field) between collisions. Hence an additional velocity component is superimposed upon

the thermal motion of electrons called drift velocity (v_n). So the net displacement of the electrons is in the direction opposite to applied field due to combined effect of drift velocity and random thermal motion. The electron drift velocity is proportional to the applied electric field. The proportionality factor depends on the mean free time and the effective mass. This proportionality factor is the electron mobility (or hole mobility) in the units of cm^2/V-s given as

$$\mu_n = \frac{q\langle \tau_c \rangle}{m^*} \tag{2.1}$$

where μ_n is the electron mobility,

q is the charge on a electron,

τ_c is the mean free time and

m* is the effective mass of the electron.

There are four key metrics to evaluate a MOSFET performance [11], which are: 1) intrinsic speed versus L_g ; 2) energy-delay product versus L_g ; 3) transistor subthreshold slope versus L_g ; and 4) CV/I versus I_{ON}/I_{OFF} ratio. These four metrics reflects the four fundamental device parameters for logic applications; namely 1) speed; 2) switching energy; 3) scalability; and 4) off-state leakage.

2.3 Nanowire Growth

Semiconductor NWs can be synthesized using a lot of growth techniques including organo-metallic vapor phase epitaxy (OMVPE) molecular and chemical beam epitaxy,

laser ablation, and low temperature solution methods wafer annealing, chemical vapor deposition. In most of these NW synthesis techniques, a metal seed is used to initiate the one dimensional growth. In OMVPE, epitaxial growth of compound semiconductors via chemical reactions is achieved by final decomposition of the input reactants/precursors at the surface. This technique utilizes metal organics such as tri-methyl-indium (In(CH3)3) and hydrides such as Arsine (AsH3) as input precursors. SA-OMVPE enables the selective epitaxy of compound semiconductors over masked regions typically with thin layers of SiO_2. MBE growth uses ultra-high vacuum chambers and solid as well as gas sources, where a beam of the reactants is directed toward the growth substrate, at which they condense and react at very slow growth rates when compared to OMVPE. CBE is a hybrid of OMVPE (source-wise) and MBE (species transport-wise) and sometimes is referred to MOMBE, which employs non-reactive atomic and molecular beams with long diffusion lengths at low chamber pressures. Wafer annealing is a process in which a solid source or a wafer is heated to high temperatures to produce an excess of group III or group V in the vapor that is thermally transported to a low-temperature zone at which layer epitaxy occurs. In CVD, high quality epitaxy can be performed when the substrate is exposed to one or more volatile precursors that decompose or react at its surface. Laser ablation is a process in which a laser beam is used to heat and subsequently remove material from a solid source, which may then be used for layer epitaxy in a similar manner to CVD. Finally, solution growth techniques enable layer epitaxy in solution at much lower temperatures than those employed for vapor phase epitaxy, however, with lower control over crystalline behavior and purity.

2.4 Nanowire Electronic Devices

Silicon NWs (Si NWs) have been most extensively studied partly due to the dominance of Si devices in the semiconductor industry and partly due to the well-developed recipes to grow Si NWs with controlled size and doping level. In a typical device structure, the Si NWs are first transferred into liquid suspension after growth via gentle 5 to 10 seconds sonication, then they are dispersed on a degenerately doped Si substrate with a thermally grown SiO_2 layer. Devices in the form of field-effect transistors can then be studied after source–drain electrode formation which is normally carried out by e-beam or photo-lithography, with the degenerately doped Si substrate serving as the back gate. Metal contacts are commonly used in a nanowire device unlike conventional MOSFETs in which the source/drain contacts are formed by degenerated doped Si. In this regard, a nanowire FET device is essentially a Schottky barrier device. Typically positive Schottky barriers are observed at the metal/semiconductor interface due to the combined effect of metal work function and Fermi level pinning by surface states. As a result, the device performance is to a large degree affected by the contact properties. For example, Cui *et al* observed that after thermal annealing which was believed to improve the source/drain contacts, the average transconductance of the Si NW devices increased from 45 to 800 nS and the deduced average mobility μ increased from 30 to 560 cm2 (V s)−1. In Cui's study, boron-doped (p-type) Si NWs with diameters in the 10–20 nm range were used. The nanowire FETs were fabricated using Ti or Ni S/D contacts, and transport characteristics were studied as a function of annealing. Ti was used since it is known that Ti can form a

stable conducting silicide with a low Schottky barrier height on p-type silicon. In general, the I_{ds}–V_{ds} curves become more linear and symmetric, and the transport behavior becomes more stable after annealing, with the measured conductance increasing by several folds.

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[11] Robert Chau, Suman Datta, Mark Doczy, Brian Doyle, Ben Jin, Jack Kavalieros, Amlan Majumdar, Matthew Metz, and Marko Radosavljevic, "Benchmarking Nanotechnology for High-Performance and Low-Power Logic Transistor Applications," *IEEE Trans. Nanotechnol.*, vol. 4, no. 2, 2005.

Chapter 3

Fabrication of Silicon Nanowire Field-Effect Transistors

3.1 Introduction

The experiments in this thesis all involves with silicon nanowire field effect transistors (Si NW-FET) with electrical contacts shown in figure 3.1. This chapter will discuss the fabrication steps involve in making FET devices.

Fabrication is closely linked to the facilities and equipments available in University of California, Riverside that has world class resources in Center for Nanoscale Science and Engineering (CNSE) with class 100 cleanroom equipped with all modern fabrication and characterization tools necessary for nanoscale research as well as knowledgeable staffs.

As an final goal, figure 3.1 shows a schematic of a dual gated Si NW FET device. This is basic starting point of our experiments and will be the final result of device fabrication steps described below.

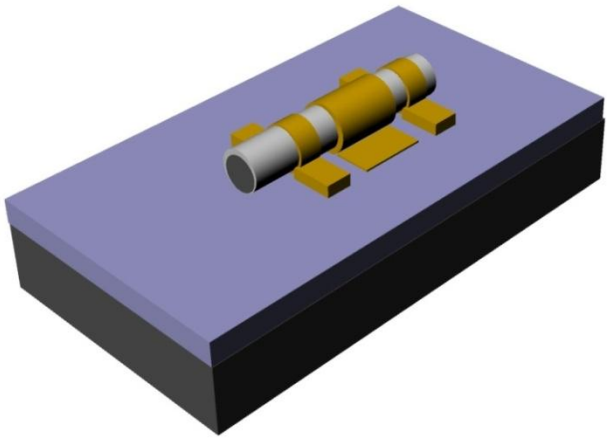


Figure 3.1: Schematic of a dual gated Si NW. Bottom dark grey part is degenerately p doped 540 μm thick silicon substrate with back contact with gold. The blue part is 300 nm thick thermally grown silicon dioxide. Nanowire is shown in light grey which is the silicon dioxide shell on silicon core (dark grey).Gold is nickel/gold contact for source, drain and top gate for the NW-FET.

Ideally, we look for long, straight nanowires for device fabrication. We want the nanowires to conduct well with good electrical contact and have gate dependent conductance. Straight nanowire allows easier and more accurate length measurements, prevents complication from loop.

3.2 Nanowire Growth

Silicon nanowires are grown on Au-coated Si substrate by vapor transport. Silicon substrates are covered with 0.5 nm of Au (99.99 %) in E-beam evaporator at a base pressure below 10^{-6} mTorr. Thickness of the metal is monitored by in situ quartz crystal. Si powder is kept at temperature ~1250 °C .Si substrate is kept at 800 °C in Ar gas .The NWs are tens of microns in length, and their average diameter is between 20 and 30 nm.

Thick oxide shell arises from phase separation of SiO into SiO2 and Si when the precursor vapor condenses to form SiNW at temperature around 800 °C.

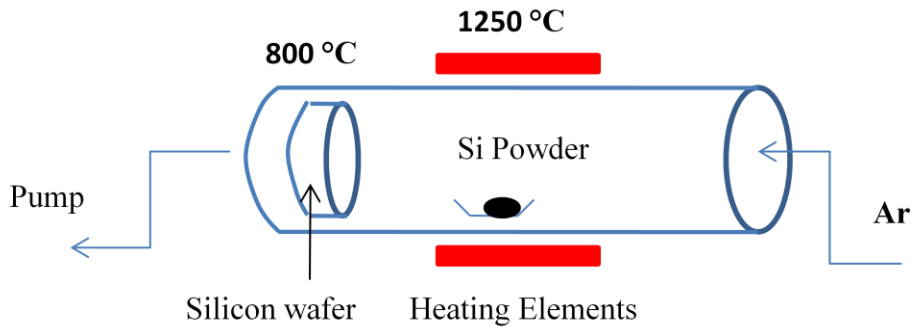


Figure 3.2: Schematic of a tube furnace where silicon nanowires are grown.

After growing, nanowires are first characterized by transmission electron microscopy (TEM) to study their crystalline structure .The figure 3.3 shows the a SiNW and its selected area diffraction (SAED) pattern .The next figure 3.4 is high resolution TEM image showing lines of silicon atoms in the nanowire. This study confirms that our grown SiNW are single crystal and very high quality which are imperative properties for electronic applications.

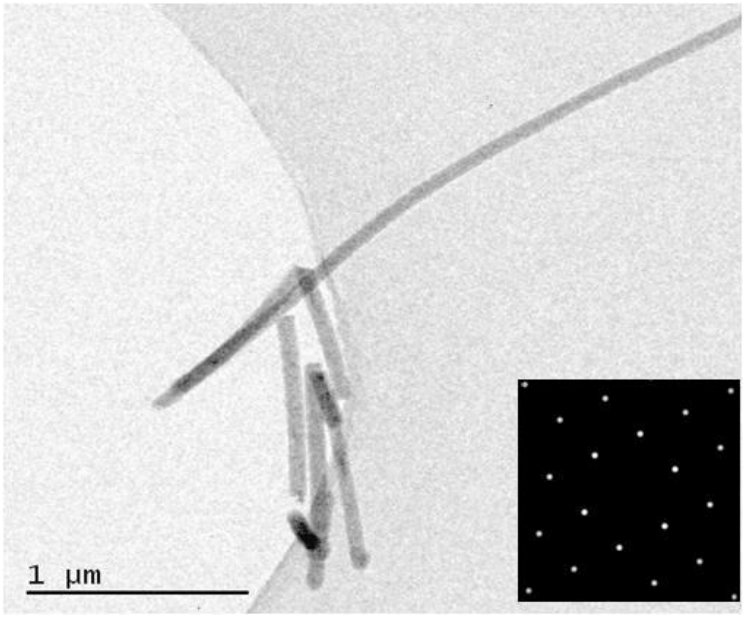


Figure 3.3: TEM image of a Si nanowires. Inset shows the selected area diffraction pattern suggesting crystallinity of nanowires.

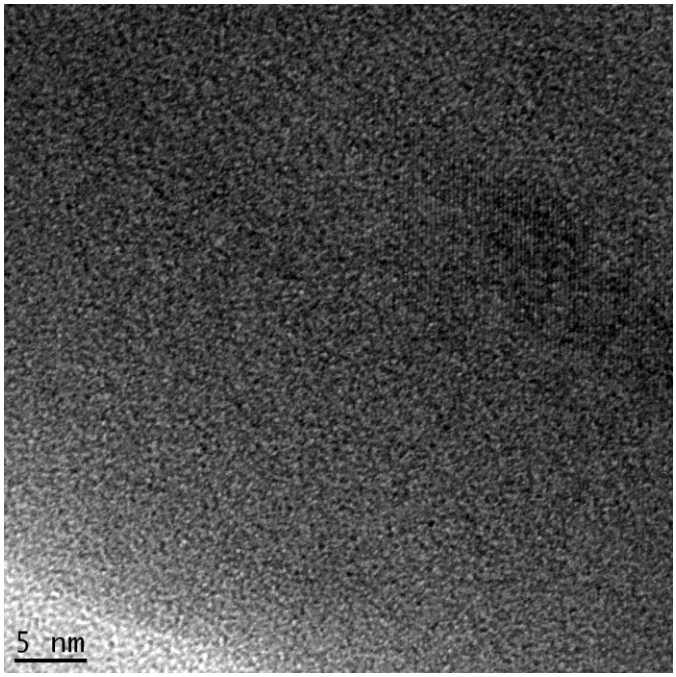


Figure 3.4: HRTEM image of a Si NW shows lines of Si atoms.

3.3 Wafer Preparation

After the nanowires are grown, electrical devices such as FET are fabricated with them. The base platform of the devices is the wafer. We used degenerately p-type doped silicon wafer of 540 μm thickness and 300 nm of thermally grown silicon dioxide on it..The reason for degenerate doping is so that it can be backgated without much voltage drop. These type of wafers are bought from commercial vendors.

The first step of the fabrication starts with patterning some marker on SiO_2 where NWdevice will be fabricated. The purpose of the alignment marker is to give some reference points so that NW can be indenfied later on scanning electron microscope (SEM) without much effort in a relatively large wafer chip .The figure 3.5 shows a optical image of such wafer. The backside of the wafer where silicon is exposed, is covered with 100 nm thick Au using E-beam evaporator to make ohmic contact that serves as global backgate.

We used Karl Suss mask aligner and Shipley 1813 photoresist to define marks. First the 4 inch wafers were spin coated with the photo resist at 3000 rpm in a spin coater to have a thickness of 1.5μm thick resist on it. Then it was baked in 120°C for 5 minutes. It was then exposed to g-line light by the mask aligner for 10 s. After the exposure the wafer chip was developed with AZ400K for 1 minute at room temperature to make opening in the exposed region where metal would be deposited. The next step involved electron beam evaporator which evaporate metal at low pressure ($8e10^{-6}$ Torr) by

hitting the metal with electron beam. The developed chip was the placed in the E-beam evaporator chamber and the chamber was pumped down to the base pressure mentioned above which took around 30-45 minutes. 5-9 nm of titanium was deposited as an adhesion layer to silicon dioxide which is followed by 50 nm deposition of Au. The wafer chip was then taken out to dip in acetone for 2 hours for lift off the metal. After the lift off process the metal only remain only at the places where photoresist was developed. The wafer chip is then flipped and placed in the evaporator again to make backgate contact. Again 10 nm of Ti and 90 nm of Au is deposited on the backside. The top side of the final chip where markers are on the silicon dioxide exist looks like the figure shown in figure 3.5.

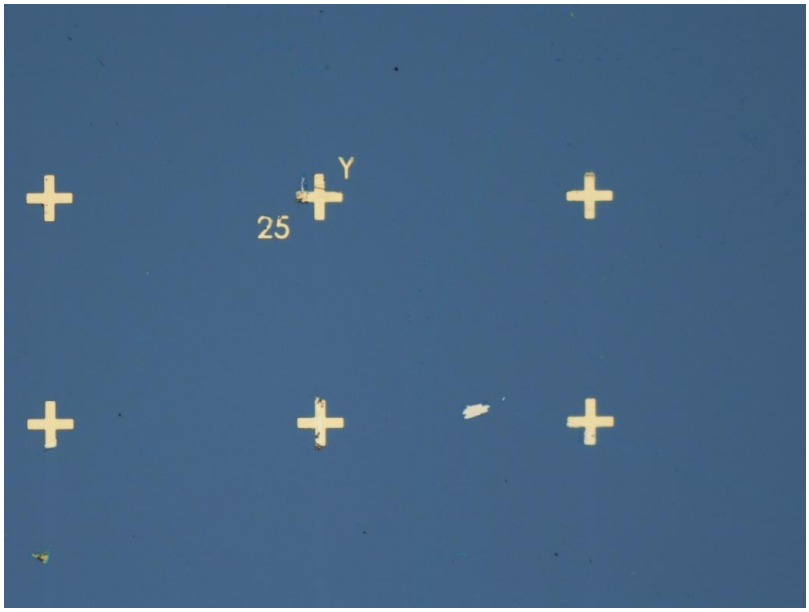
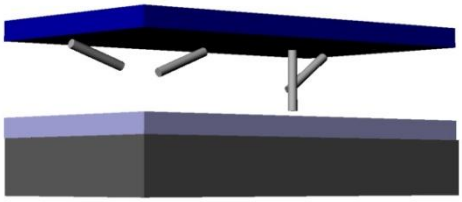


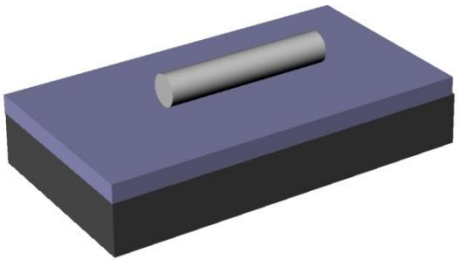
Figure 3.5: Optical image of SiO_2/Si wafer with pre-patterned marker.

3.4 Device Fabrication

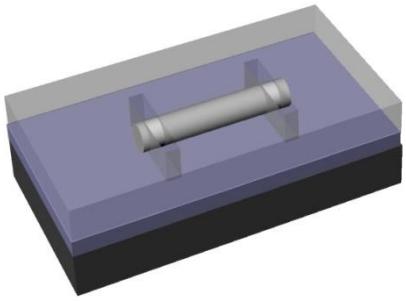
Now we are ready to transfer the nanowires to wafer chip. Before transferring



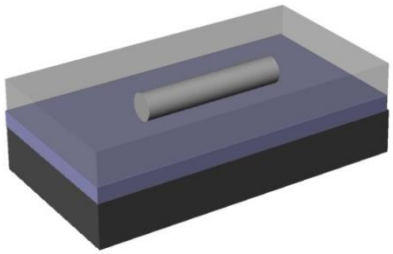
(a)



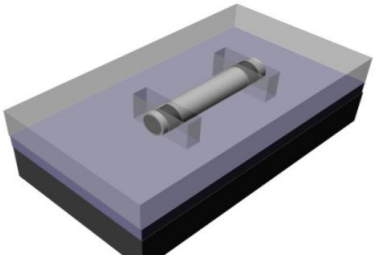
(b)



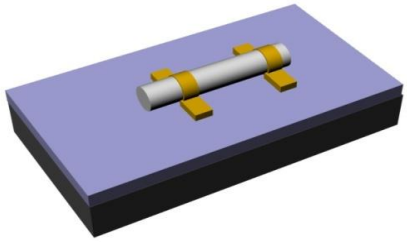
(c)



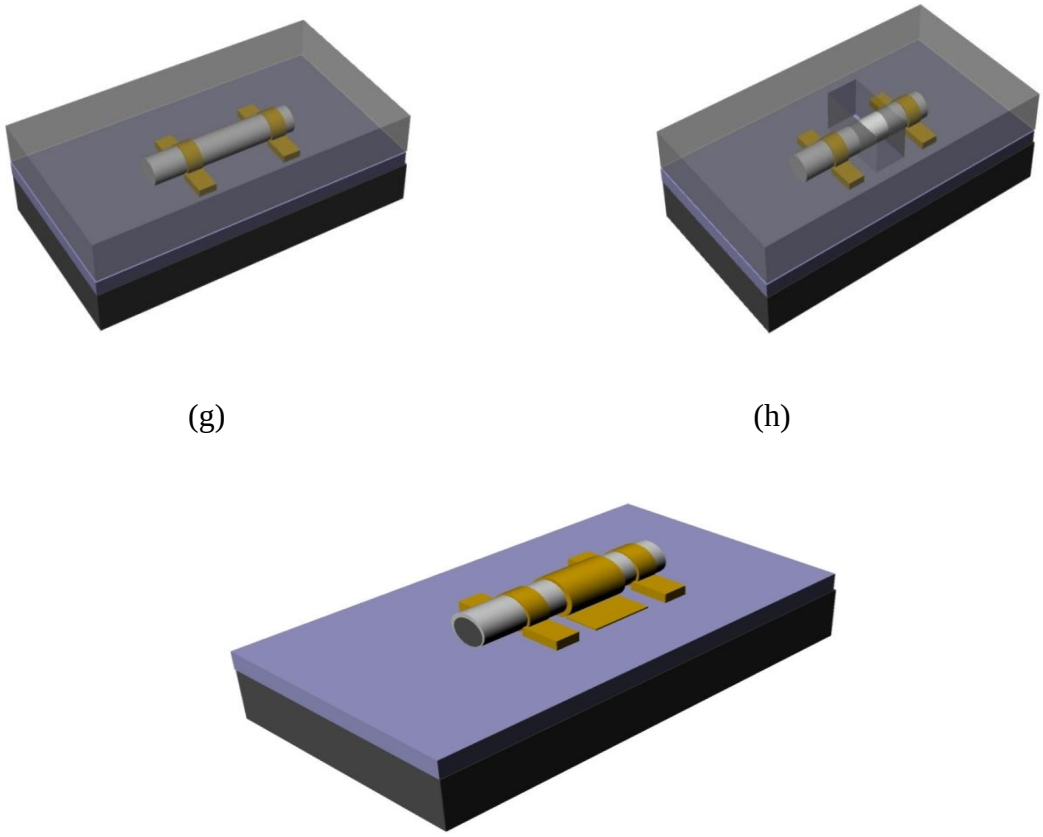
(d)



(e)



(f)



(g) (h)

(i)

Figure 3.6: Process flow for fabricating top gated Si NW FET. **(**a) Mechanical transfer from the growth chip to device chip (b) Nanowire is indentified through SEM or dark field optical microscopy c) layers of MMA (methyl methacryllate) and PMMA (poly methyl methacryllate) are spun on the substrate. d) First Electron Beam Lithography to open source and drain contact (e) 10 s of Buffer Oxide Etch is done to remove shell oxide (critical step to obtain good electrical contact) 70 nm of Ni is evaporated followed by 50 nm of Au in Electron beam evaporated in 10^{-6} Torr base pressure right after BOE etch g) Another layer of MMA and PMMA are spun on the substrate for second EBL for gate opening (h) Second aligned EBL is done for top gate i) 70 nm of Ti evaporated followed by 50 nm of Au in Ebeam evaporator for final Dual gate Si NW FET.nanowire ,the device chip is thoroughly cleaned by acetone, iso-propyl alcohol (IPA) and finally with DI water to remove any dust or organics particle from the chip.Then nanowire growth wafer is gently rubbed to the device wafer with tweezers .Some of the nanowires got transferred by this and they are identified under dark field microscopy which looks like the figure 3.7 (a).After the right nanowires are selected based on their length and shape, their position is marked as we have a substrate which has coordinate

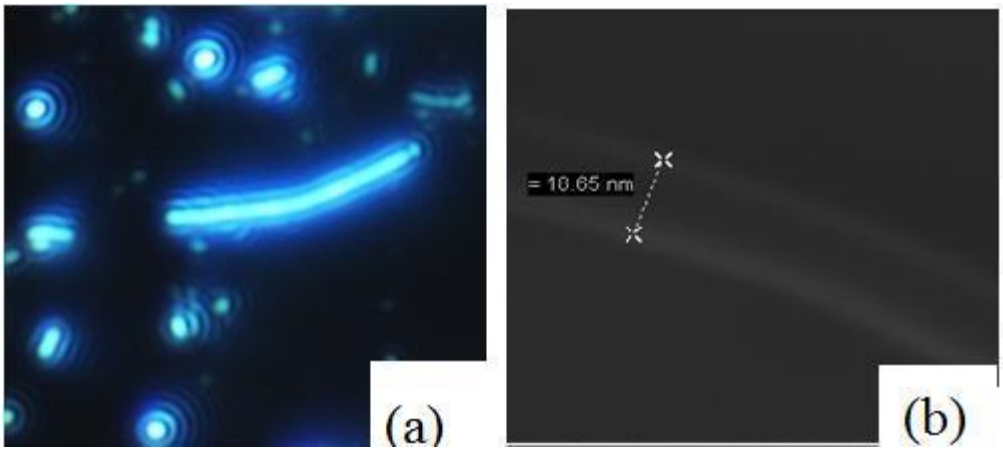


Figure 3.7: (a) Optical dark field image of a single nanowire (b) SEM image of a single nanowire

marker. The next step is small refined marker around each selected nanowire. For this we use Electron Beam Lithography (EBL) which allows us to make opening in the ebeam resist precisely where user wants. Here we use PMMA/MMA bilayer of resist. PMMA (poly methyl methacryllate) and MMA (methyl methacryllate) are positive ebeam resists consisting of long polymer chain of carbon atoms which are available in various molecular weights. The standard molecular weights of PMMA which we use here is 950K. The standard use for MMA/PMMA bi-layers in EBL gives us good lift-off of metallic structures. For good lift-off we need an undercut resist profile to avoid coating the sidewall of the resist when we evaporate metal. The PMMA/MMA bi-layer gives a larger undercut profile than PMMA/PMMA as shown below.

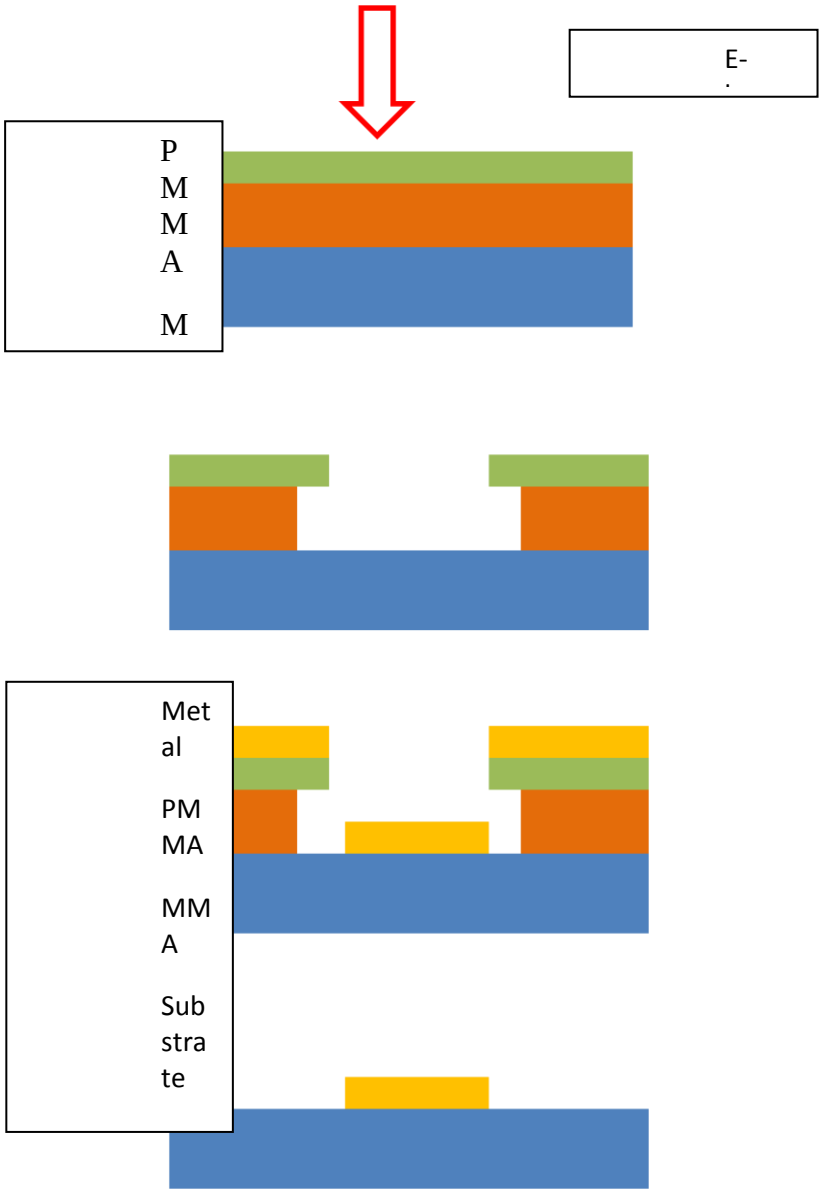


Figure 3.8: Schematic of EBL basic using PMMA/MMA resist.

First the substrate containing nanowires are spin coated with MMA in 3200 rpm for 40 seconds which gives around 200 nm of thick resist followed by 15 minutes baking at 180°C.Then PMMA A2 (Microchem Inc.) is spin coated at 3200 rpm for 40 seconds to

have 80 nm of resist on top of MMA. Then it is baked again for 10 minutes at 180°C and ready to load into Leo Supra Electron Beam Lithography. At this point our target is to put a small marker shown in figure 3.9 which will help us later to put aligned source, drain and top gate contact. For this marker, 0.5 μC line dose is used by EBL. This marker is placed quite accurately in terms of position as we already know the position of the nanowire from the optical microscope image. After the exposure we develop the wafer in

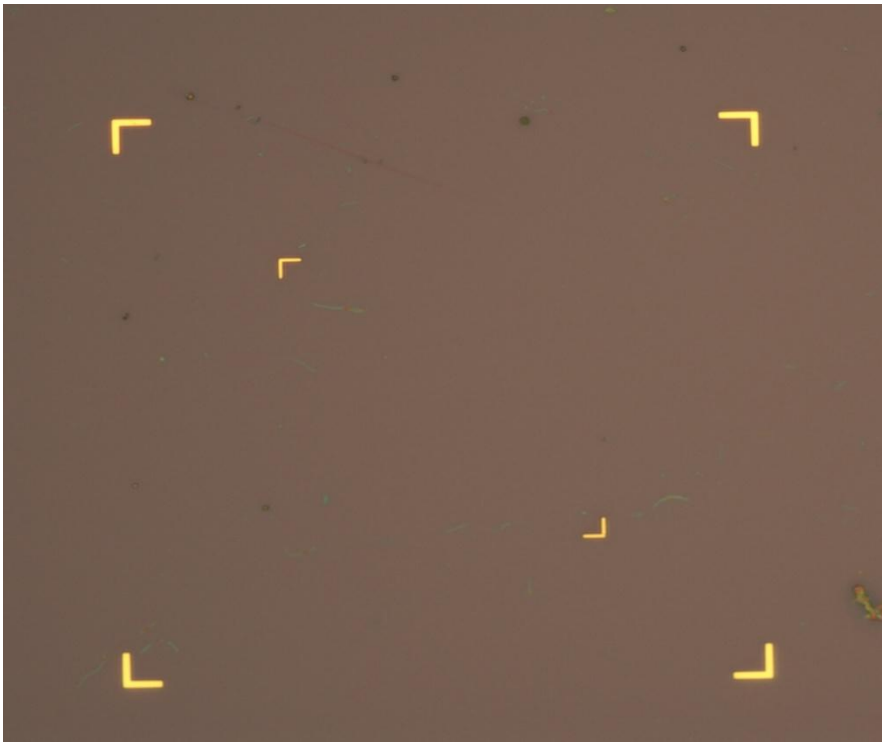


Figure 3.9: Small marker around nanowire for alignment.

1:3 MIBK (methyl isobutyl ketone):IPA solution for 65 seconds followed by 60 seconds dip in IPA and a rinse with DI water.At this point the sample is ready to load into electron beam evaporator where 10 nm of Ti is deposited followed by 50 nm of Au at a

base pressure of $8x10^{-6}$ Torr. The deposition rate is maintained lower than 0.2 nm per second. After the deposition the sample is taken out from the E-beam evaporator chamber and dipped in acetone for 5/6 hours to do the lift-off and finally we are left with the small marker shown in figure 3.9.

Now we do the above same procedure for drain and source contacts. The previously patterned small marker serves as alignment marker for this step. This time after resist development the sample is immersed in buffer oxide etchant (BOE) for 10 seconds to remove the shell oxide from the nanowire from the region where source and drain contacts would be made. Right after the BOE dip the sample is loaded into the e-beam evaporator chamber without any delay to prevent oxide re-growth on silicon from ambient. This step is crucial for good electrical contact. For contact we choose 70 nm of Ni followed by 50 nm of Au as .Ni is chosen as it make low barrier Schottky contact with p-silicon.

After the Ni/Au deposition for source and drain contact, the sample is annealed at 400°C in N_2 ambient for 4 minutes in rapid thermal annealer.This annealing makes Ni to nickel silicide (NiSi) which forms low resistive contact with nanowire.In this case silicide extends to exposed NW section also and about 500 nm of exposed SiNW turns to nickel silicide. This silicide formation is unlike to planar device and shown in the figure 3.10.It clearly shows annealing effect as the silicided part is brighter and un-silicided part is darker. It also turns the NW unipolar to ambipolar conductor which will be discussed later chapter

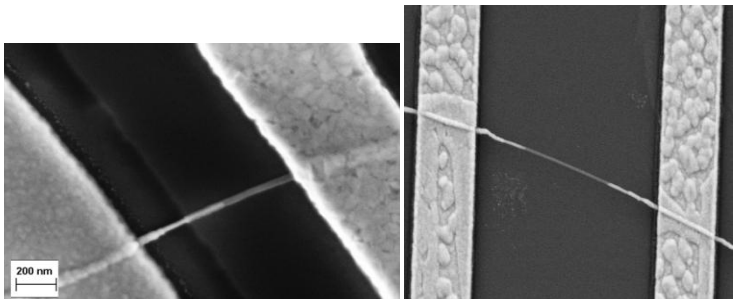


Figure 3.10: SEM image of NW showing NiSi after annealing.

Next step is to fabricate top gate. It follows exactly same steps for source and drain contact formation except the part this time BOE etchant is avoided as the shell oxide serves as gate oxide. Another deviation for this step is we use 70 nm Ti and 50 nm Au instead of Ni. After all this long procedure are completed the final structure is shown in the figure 3.11 and the schematic of the final structure is shown above in the figure 3.6 (i).

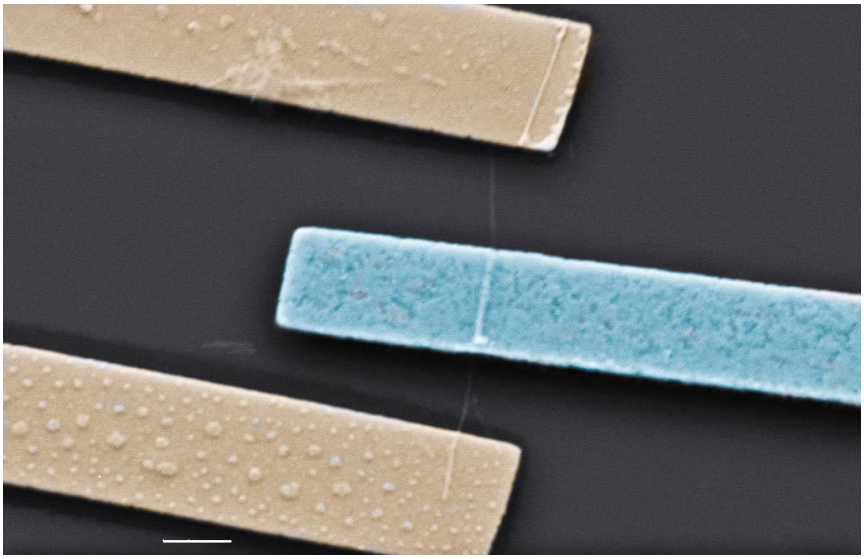


Figure 3.11: SEM image of top gated Si NW. False colors are used to show source, drain (golden) and top gate (blue).Scale bar is1 μm.

3.5 Fabrication Issues

The some several critical fabrication issues which could potentially fail the device. One of them is shadowing effect in metal evaporation. The metal in the e-beam evaporator evaporates in conformal way that means from the metal target source metal evaporates in normal direction. Since our nanowire is cylindrical shape there is a chance that metal will not go under the NW close to substrate. This situation is illustrated in the figure 3.12.The maximum thickness of the deposited metal depends on the thickness of the resist. For good lift-off the thickness of the metal should not be more than 1/3 of the the thickness of the resist. Here in our case total thickness of the resist is around 300 nm. Hence our metal thickness should be around 100 nm. But if the diameter of the NW is above 50 nm then the shadowing effect takes place and eventually there would be no electrical contact to NW. In this case to avoid shadowing effect , two steps of evaporation is necessary.First the sample is kept at 45° angle with a holder then metal is evaporated so that metal goes underneath the NW close to the substrate where NW is creating shadow previously.Then the sample is taken out and the other side is kept upfront with 45° angle to evaporate metal once again. The whole steps are shown in the figure 3.12.

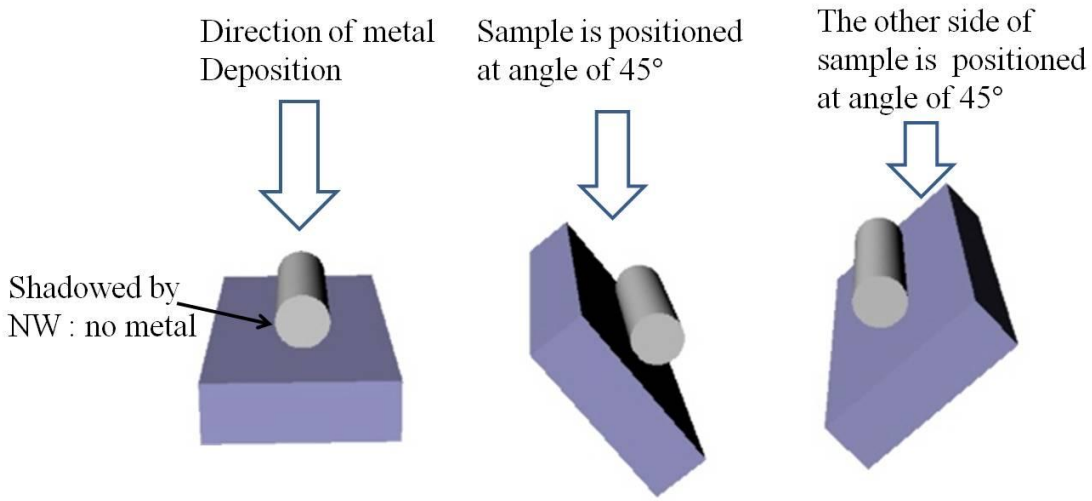


Figure 3.12: Schematic of the shadowing effect.

The outcome of the shadowing effect where there is no metal contact with the NW is shown in the figure 3.13.

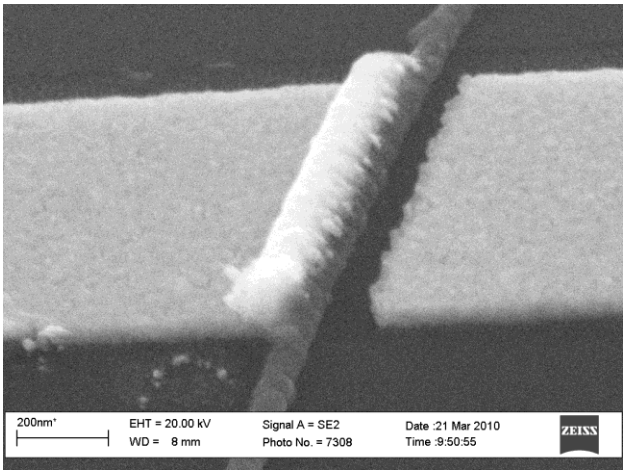


Figure 3.13: SEM image of a NW contact shows the shadowing effect.

Chapter 4

Electrical Characterization of Silicon Nanowires

4.1 Introduction

Semiconductor nanowires (NWs) are very attractive and versatile building blocks for future electronic systems because of the unique possibilities they offer for rational control of fundamental properties such as dimension, composition, and doping during growth. A wide range of NW based devices and systems, including transistors and circuits light emitters and sensors have been explored. NW field-effect transistors (NWFETs) have been of particular interest recently both as vehicles for investigation of basic carrier transport behavior and as potential future high-performance electronic devices. NWFETs fabricated from silicon and group IV, III-V and II-VI semiconductors and conductive oxide have demonstrated promising FET characteristics in top-gate back-gate and surround-gate FET geometries. Silicon in particular is an attractive candidate for NW-based electronic devices because of its potential opportunity to integrate in current CMOS technology. In this chapter, I will discuss about electrical characterization of silicon nanowire and methods of data extraction and analysis in detail.

4.2 Instruments for Characterization

We use Agilent B1500A semiconductor parametric analyzer to monitor current-voltage relationship in different configuration. This parametric has four medium power source monitor units (SMU), each of which can supply upto 100 V with maximum current of 100 mA with a current resolution of 1 fA. If proper care is taken care such that the device under test (DUT) and all the cable are kept in a dark and noise free environment, we can measure down to 10 fA of current. Of course for this type of sensitive and low current measurement we need to use tri-axial cable which has capability to compensate the charging of cable.

The next very important thing for measurement is probe station. We have Signatone probe station with four probes which are capable of handling tri-axial cable. The chuck of the probe station is feed with a heater to provide the capability of temperature dependent measurement. All the setup is enclosed by a shielded box that gives an isolation from the outside acoustic noise, light and all other kind of disturbance while measuring.

For a top gated and back gated device, we need four SMUs which gives us ultimate freedom to vary any of the voltage/current independently. The schematic of such arrangement is shown in below figure 4.1.

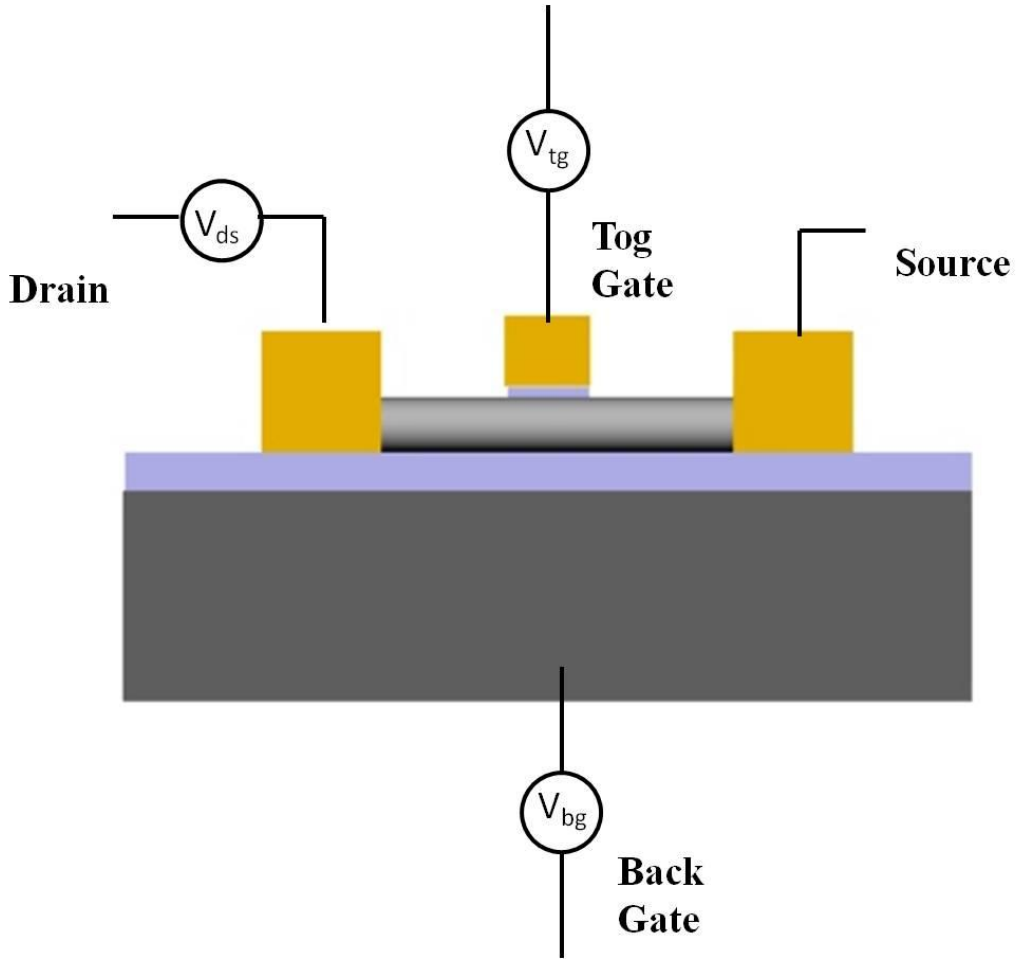


Figure 4.1: Schematic of electrical characterization of a FET device. Four SMUs are used, one for back gate, one for top gate and other two for source and drain contact.

4.3 Effect of Silicidation

As mentioned earlier, we anneal our device at 400°C for 4 minutes which makes NiSi silicide.The silicidation does not only confined under the metal but takes place in the exposed region of the nanowire also and thus reduce the effective length of the nanowire.

The EDS spectra on the NW confirms that the presence of Ni in the NW segment. The spectra is shown below in the figure 4.2.

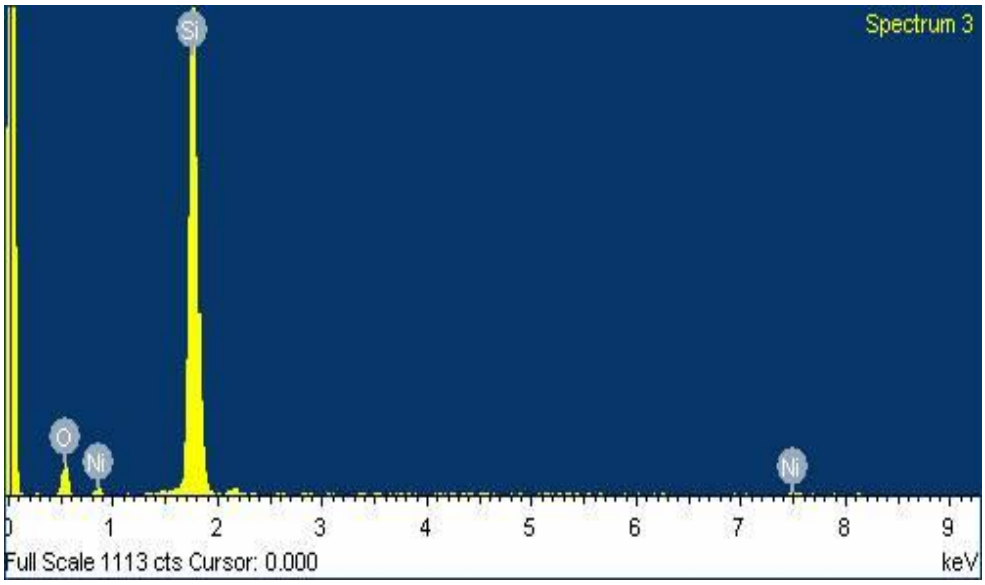


Figure 4.2: EDS spectra on NW near the source/drain contact showing presence of Ni in NW.

and make low resistance contact to the nanowire. It has also significant effect on electrical characteristics of NW. Before annealing the NW shows unipolar behavior and only hole can conducts. But after silicidation, the NW turns to ambipolar which can also conduct electrons. It also improves the quality of contact for hole. Now, the magnitude of the hole currents also improves.

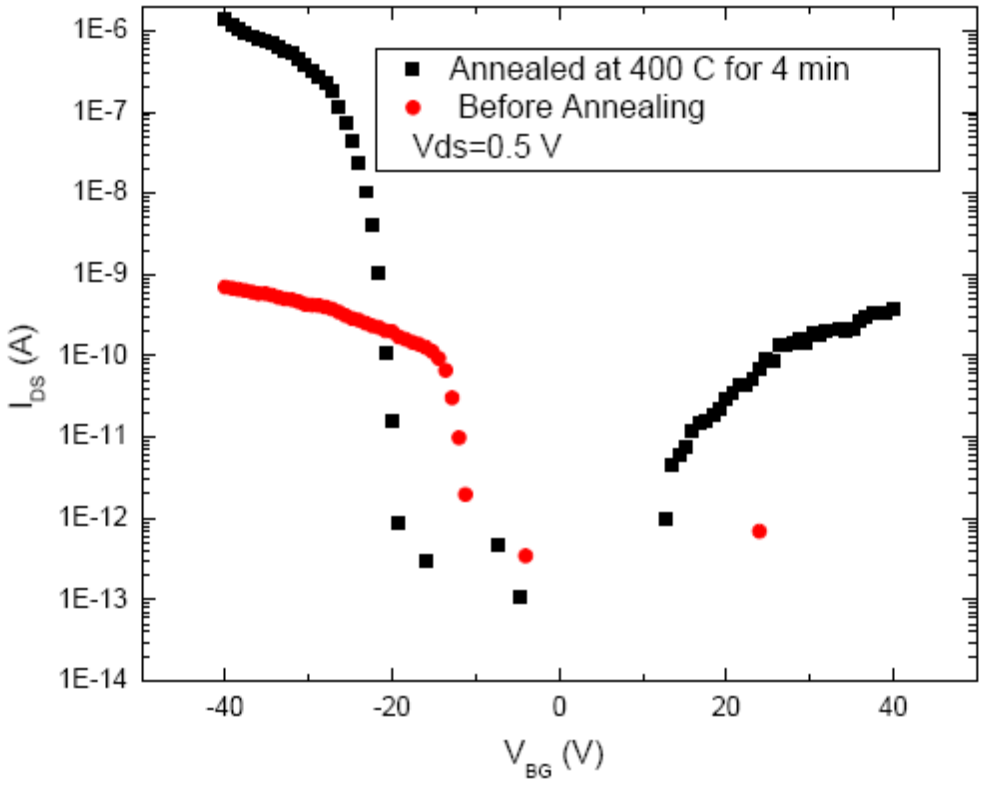


Figure 4.3: I_{ds}- V_{gs} curve for Silicon nanowire before and after annealing.

4.4 Back Gated Silicon Nanowire Measurement

We first start with a device which has source, drain and back gate only that means there is no top gate at this point. This configuration gives us idea about devices contact and transport behavior. A typical back gated NW SEM is shown below in the figure 4.4.

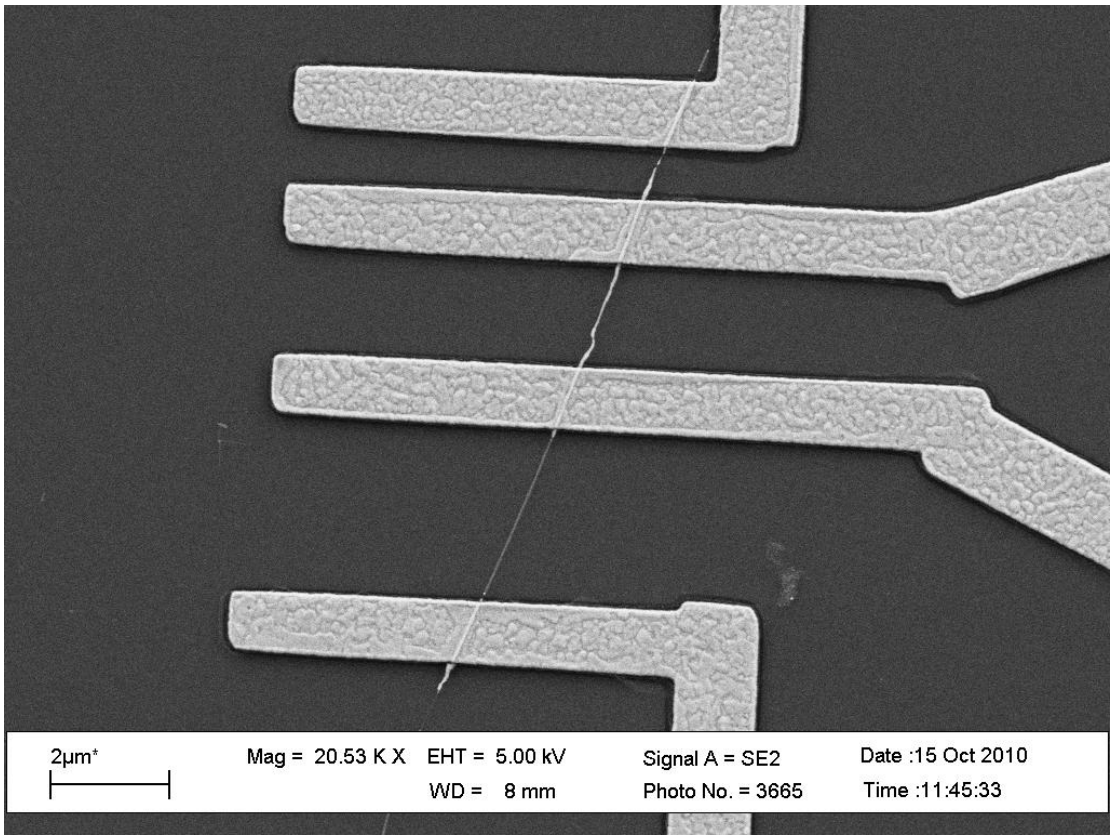


Figure 4.4: SEM image of back gated NW. The four contacts are shown.

For back gated measurement, first the back gate (V_{bg})is varied from -60 V to +60 V while keeping the drain to source voltage (V_{ds}) constant at +1 V and next -1 V. This measurement produce the curves shown in figure 4.5 and 4.6. The reason for using such as high back gate bias is that our back gate oxide thickness is 300 nm which is quite high in compare to typical gate oxide of MOSFET. This curves are found from a NW which is 1.75 µm long and 50 nm of diameter of which 10 nm is shell oxide. The NW shows ambipolar conduction since they are undoped and any type of carrier (electron/hole) can

be induced in the channel. The interesting observation from this curve is for +1 V and -1 V drain-source voltage, they are not symmetrical possibly different schottky barrier in the contact region due to image force .

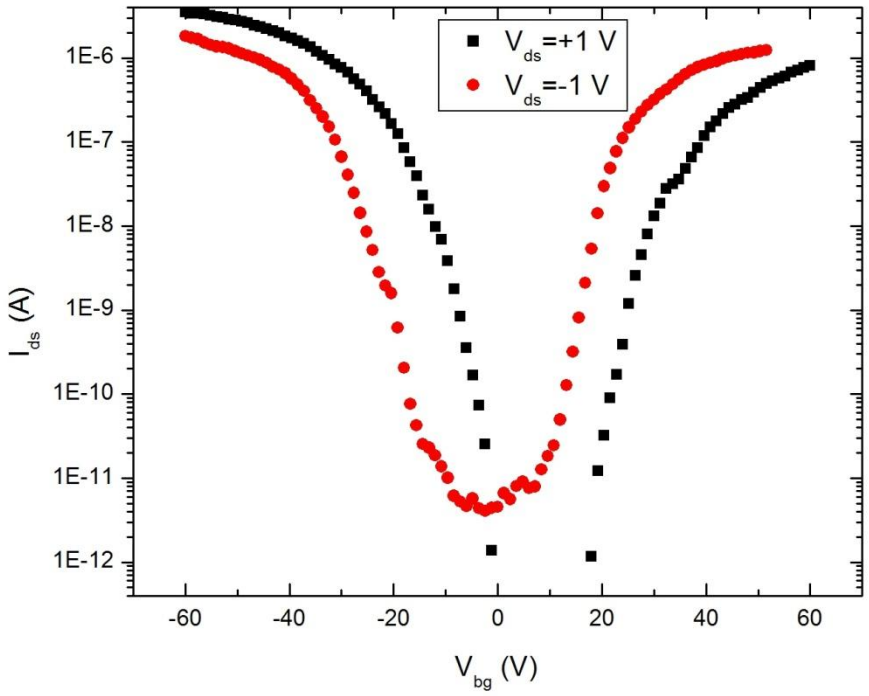


Figure 4.5: I_{ds}- V_{gs} curve for 1.75 µm long silicon nanowire.Vds is at +1V and -1 V.

Another important observation is that the hole conduction which is induced by negative voltage at back gate is higher than that of electron owing to the fact these are all schottky contact type FET. That means there is a energy barrier from the silicide contact to the conduction band and the valence band. For hole to NiSi the energy barrier is around 0.35-0.45 eV while for electron the barrier is around 0.65 -0.75 eV. This explains that holes

are more favorable to jump into the NW valence band (hole) rather than electron to jump into the conduction band and give rise to current flow.

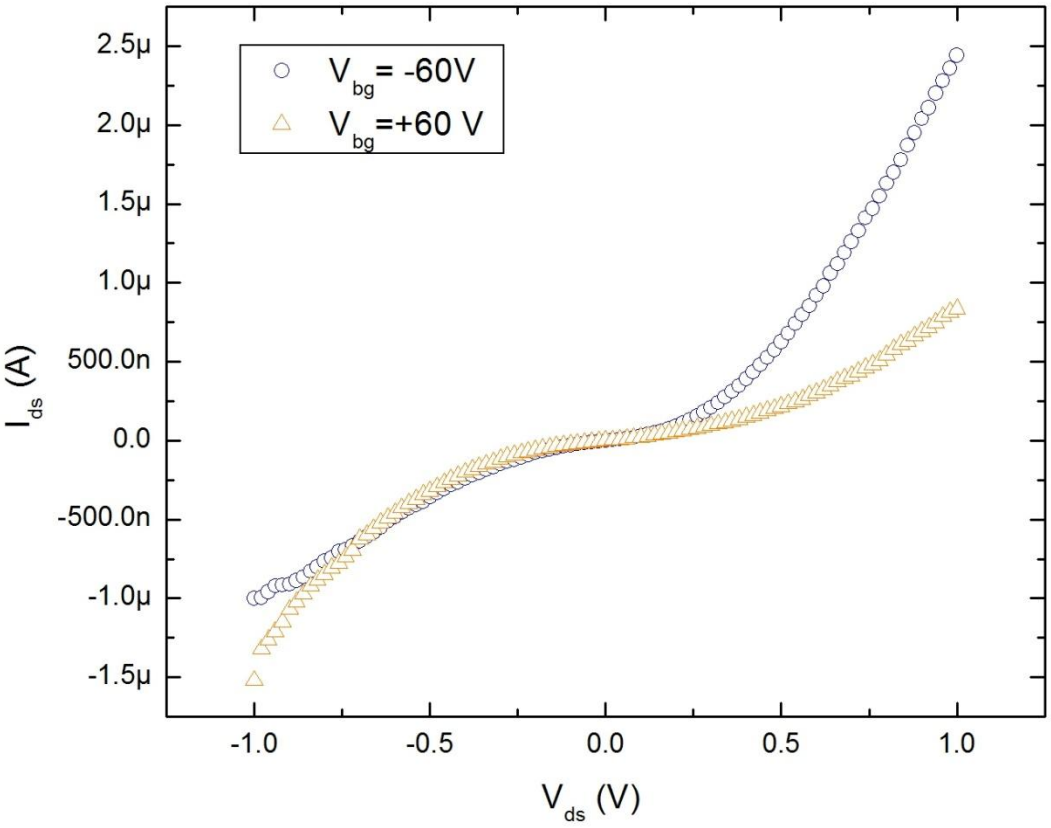


Figure 4.6: I_{ds}- V_{ds} curve for 1.75 µm long silicon nanowire. Vgs is at +60 V and -60 V.

In figure 4.2, the Ids-Vds relationship is shown for electron and hole. For +1 V the hole current is higher than electron due to small Schottky Barrier Height (SBH). But for -1 V electron current is higher possibly due to image force the SBH for electron reduced while it increased for holes.

4.4 Dual Gated Silicon Nanowire Measurements

Dual-gate FET geometries fabricated with our process (with a top-gate electrode on the NW and the substrate used as bottom gate) allow a more extensive electrical

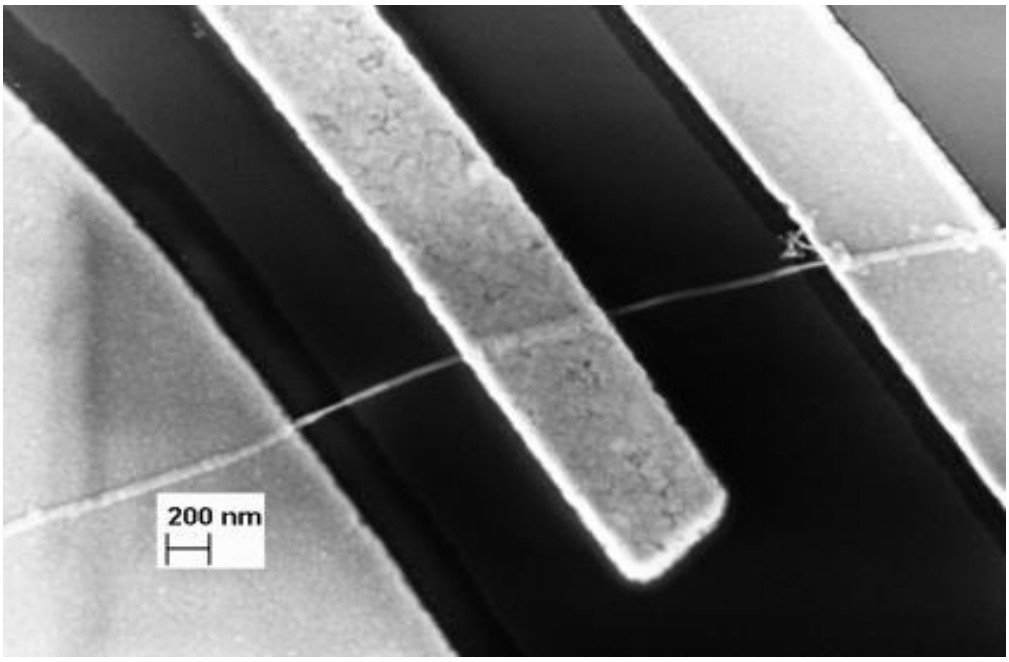


Figure 4.7: SEM image of dual-gate Silicon NW device.

characterization due to the various combinations offered by the interplay of the gate potentials. Figure 4.8 plots transfer curves (drain current I_D, as a function of gate voltage) recorded by sweeping the top-gate voltage (V_{TG}) from -1 V to +1 V, with the back-gate (V_{BG}) kept between at -40V. In this case, the source-drain voltage (V_{DS}) is set to 50 mV. As a convention, we consider the grounded terminal as source and the biased terminal as

drain so that V_{DS} represents the drain potential. Figure 4.7 shows that we can choose a *V*TG to selectively suppress hole conduction, transforming a back-gated ambipolar FET in a unipolar n-type or p-type FET, respectively. The Figure 4.8 schematize the band diagrams corresponding to the ON states for the lowest V_{TG} . The band pinning at the Schottky contacts due to the back-gate sweep is sufficient to inject either holes or electrons (in this case hole) into the NW but if V_{TG} is too high (shown in figure 4.9) a barrier is formed in the center of the NW that hinders the transmission of holes.

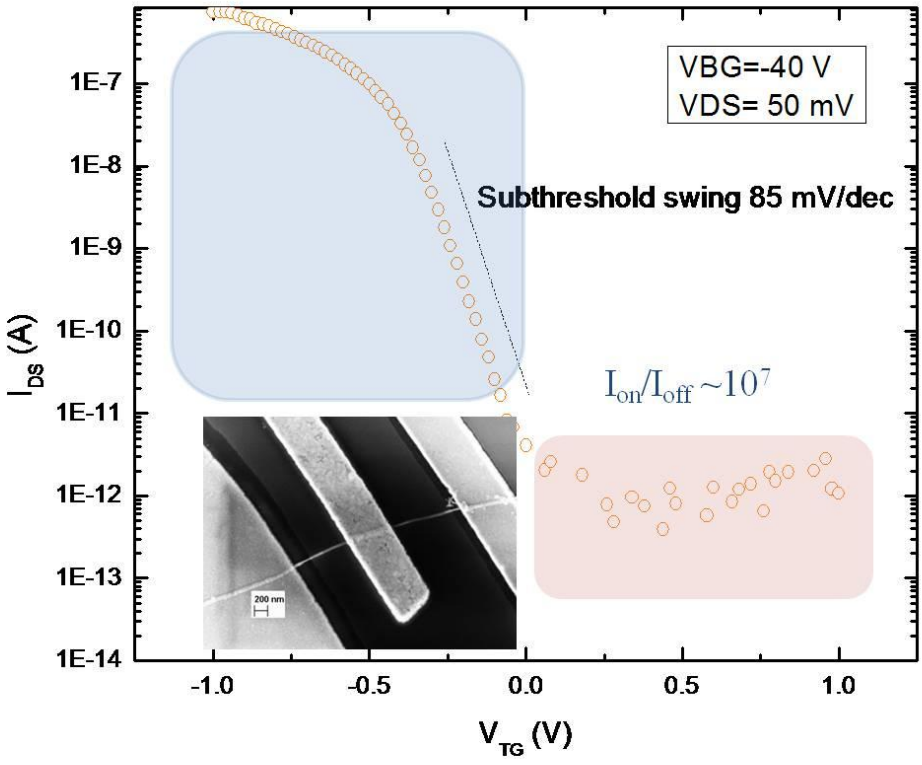


Figure 4.8: I_{ds}- V_{tg} curve for the silicon nanowire with -40 V at the back gate.

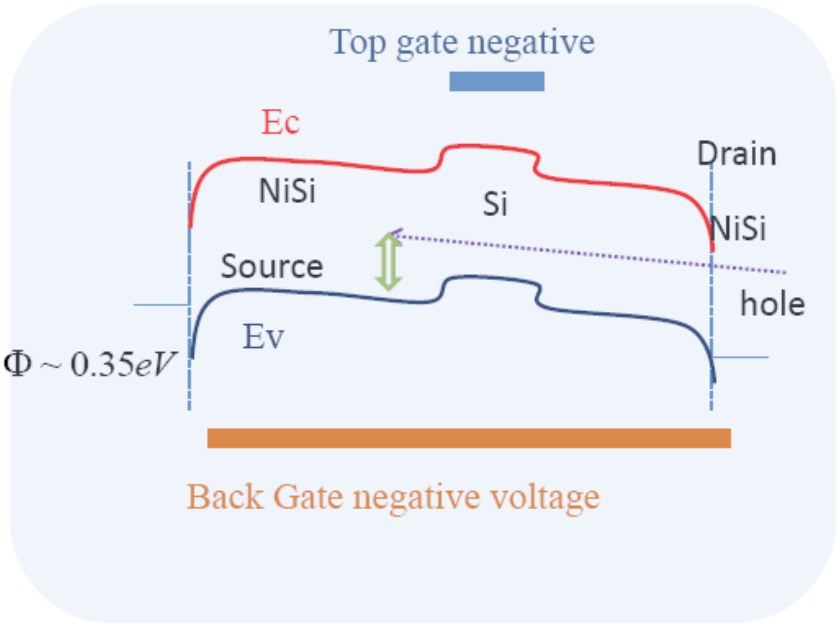


Figure 4.9: Schematic of the band diagram for On state for h-regime.

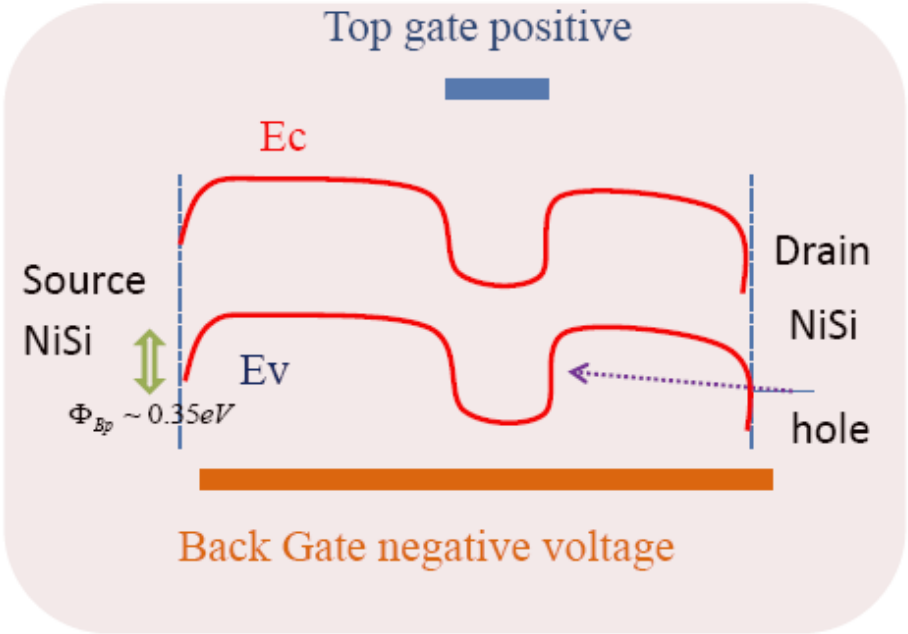


Figure 4.10: Schematic of the band diagram for OFF state for h-regime.

Similarly Figure 4.11 plots transfer curves (drain current *I*D, as a function of gate voltage) recorded by sweeping the top-gate voltage (*V*TG) from -1 V to +3 V, with the back-gate (*V*BG) kept between at +40V. In this case, the source-drain voltage (*V*DS) is set to 50 mV. As a convention, we consider the grounded terminal as source and the biased terminal as drain so that *V*DS represents the drain potential. Figure 4.7 shows that we can choose a *V*TG to selectively suppress electron conduction, transforming a back-gated ambipolar FET in a unipolar n-type or p-type FET, respectively. The Figure 4.12 schematize the band diagrams corresponding to the ON states for the high *V*TG . The band pinning at the Schottky contacts due to the back-gate sweep is sufficient to inject either holes or electrons into the NW but if *V*TG is too low (shown in figure 4.13) a barrier is formed in the center of the NW that hinders the transmission of electrons.

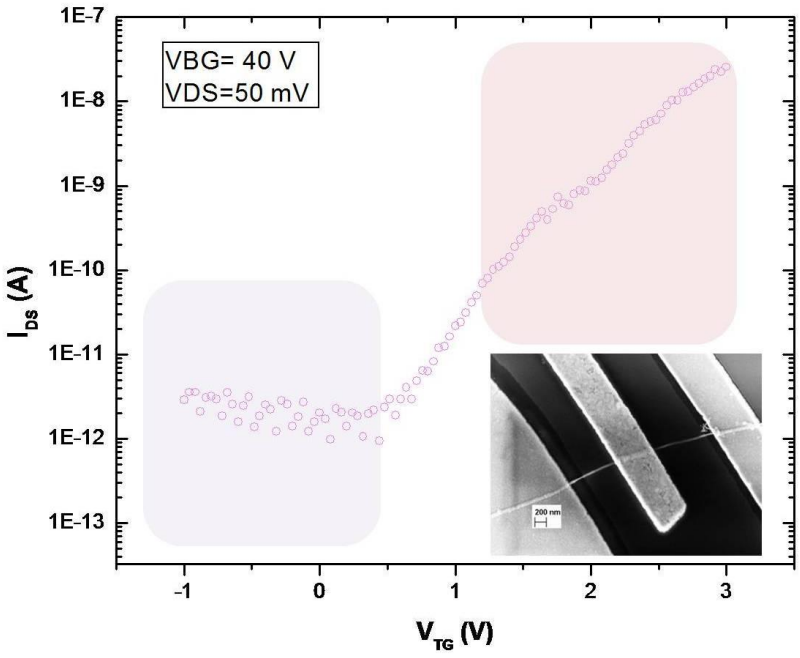


Figure 4.11: I_{ds}- Vtg curve for silicon nanowire with +40 V at the back gate.

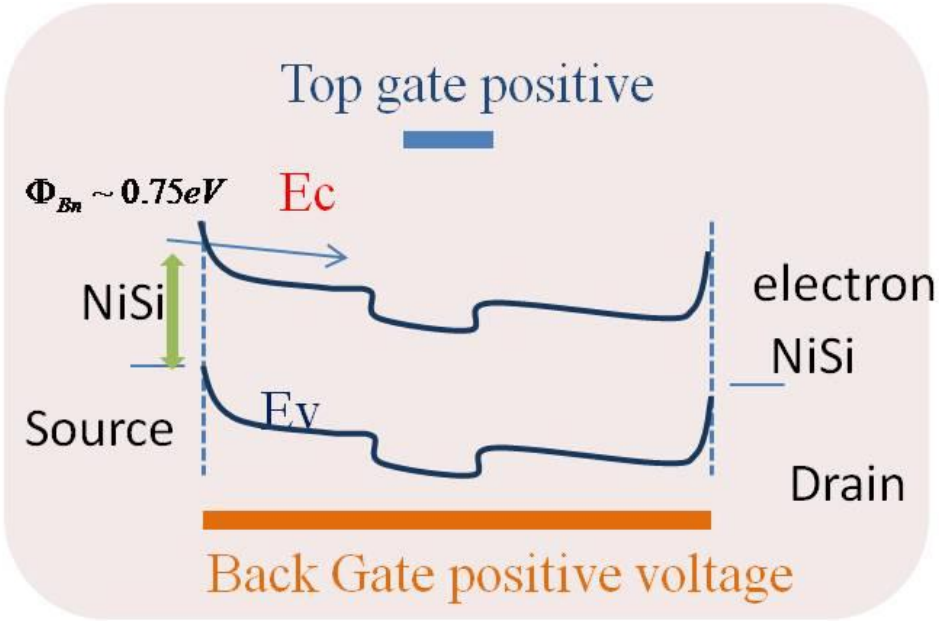


Figure 4.12: Schematic of the band diagram for ON state for e-regime.

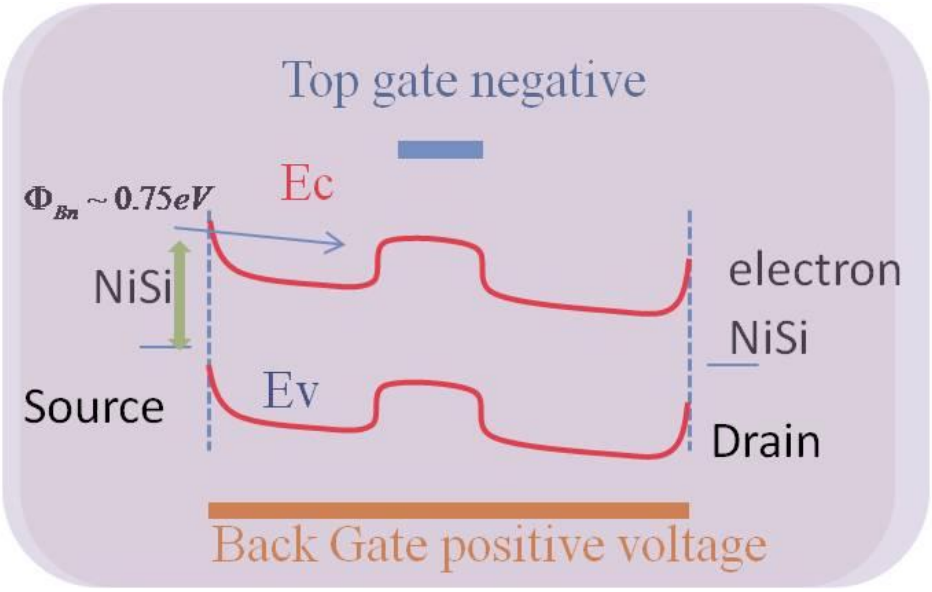


Figure 4.13: Schematic of the band diagram for OFF state for e-regime.

It is more desirable during operation to switch the FET using the top-gate, as the better coupling ensures lower threshold voltages and steeper subthreshold slopes. In this configuration it is also important to emphasize small differences in electrical behavior due to device scaling. Figure 4.11 and 4.8 plot transfer curves (*I*D *vs* gate voltage) recorded by sweeping *V*TG, while *V*BG is kept at +40 V and -40 V, respectively. In all cases, *V*DS is set to 50 mV. For long-channels, the corresponding inverse subthreshold slopes [d*V*TG/d(Log *I*D)] for hole and electron accumulation are 85 and 430 mV/dec, respectively. These are comparable to the best top-gated NW FETs to date.

4.5 Effect of the Back Gate on Silicon Nanowires

The back gate voltage has profound effect on the contact barrier.First of all it thins down the SB width that facilitate tunneling of hole (electeon). Second due to image force effect, the barrier height is reduced by the amount of $\Delta\Phi = \sqrt{\frac{qE_m}{4\pi\varepsilon_s}}$ .This also helps to holes and electrons to penetrate more into the NW from the contact.The effect of this back gate is shown in figure 4.14 and 4.15 show that for holes the schottky contacts turns to almost ohmic contact if higher voltage is applied to back gate.

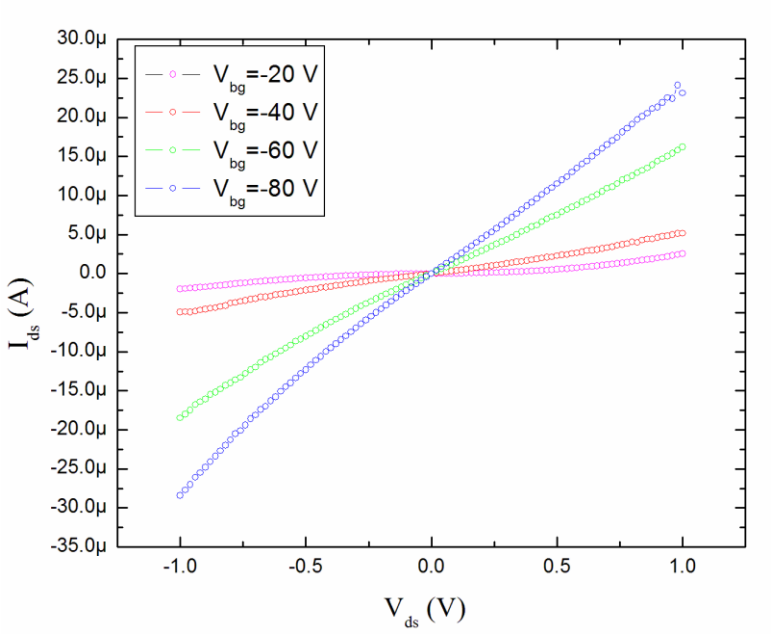


Figure 4.14: I_{ds}-V_{ds} curves at different back gate voltage.

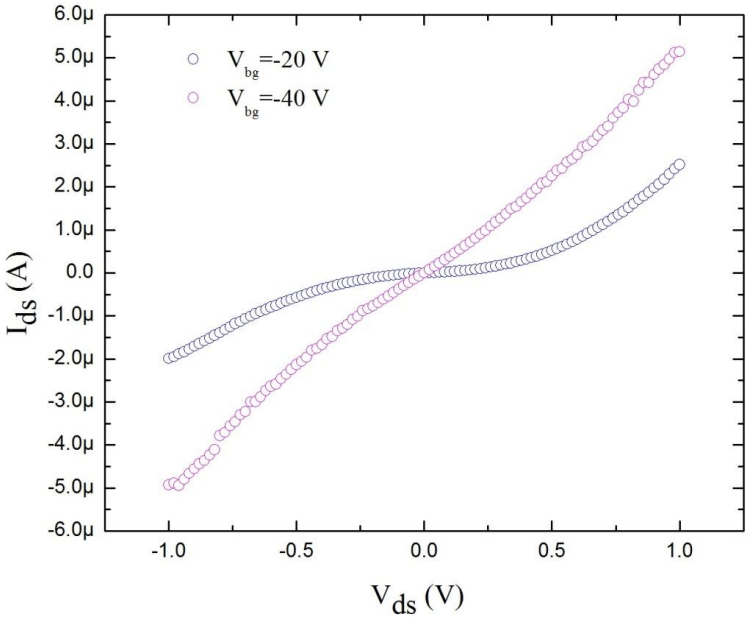


Figure 4.15: I_{ds}-Vd_s curves at different back gate voltage showing schottky contact turns to ohmic contact for holes for sufficient back gate voltage.

4.6 Effect of Temperature on Silicon Nanowire Transport

We have investigated the effect of temperature on the carrier transport in NW.As the temperature is increased we expect that conductivity will decrease due to increased phonon scattering. But since we have SB FET the injection of carrier first increases as thermionic emission goes up for hole as we increase the temperature from ambient to 50 °C. Even the carrier scattering is increases in the NW but the total number of carrier increases and thus conductivity increase. But after the phonon scattering dominates and current reduces. In the figure 4.14 the effect of temperature on conductivity shown.

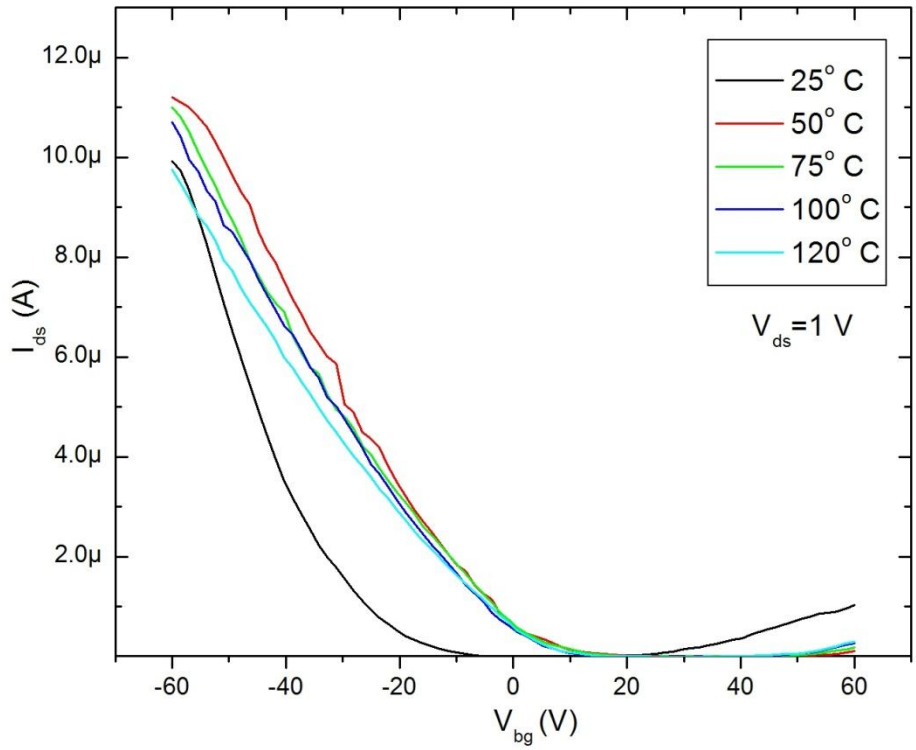


Figure 4.16: I_{ds}-V_{gs} curve at back gate V_{ds}=1 V. Temperature varied from RT to 120 °C.

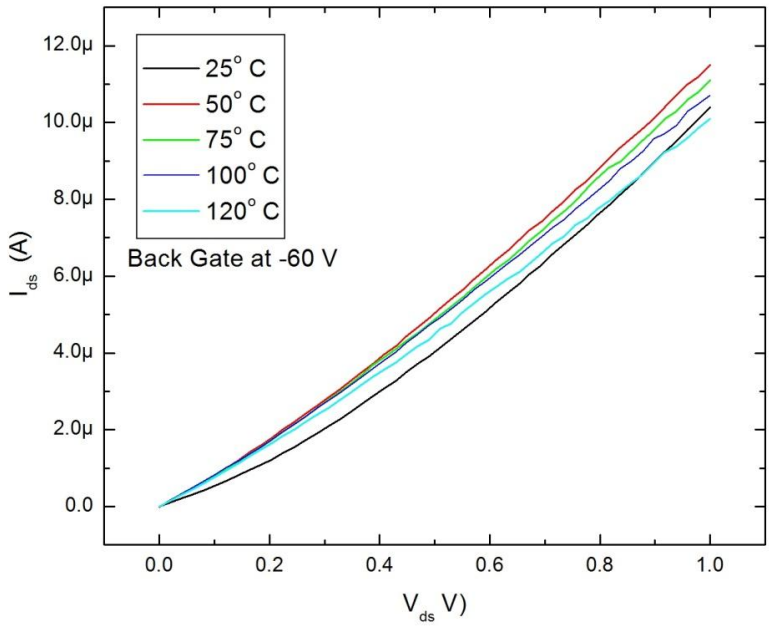


Figure 4.17: Ids-Vds curve at back gate -60 V. Temperature varied from RT to 120 °C.

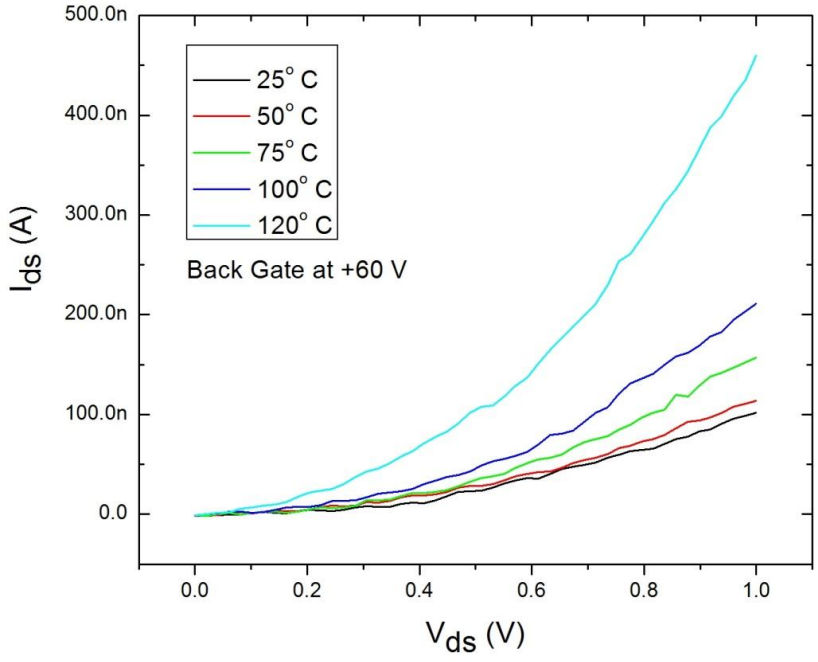


Figure 4.18: I_{ds}-V_{ds} curve at back gate +60 V. Temperature varied from RT to 120 °C.

The figure 4.14 shows the hole transport varying the temperature. The back gate is kept at -60 V to inject holes from the contact. As hole has lower SB height conduction is almost ohmic. But there is non-linearity due to thermionic emission. For hole the current show an increment from RT to 50°C as thermionic emission increases the hole injection even though the mobility is reduced by phonon scattering. After that we see decrease in current due to phonon scattering.

The figure 4.15 shows the I_{ds}-V_{ds} for electron transport at various temperature. Since SBH is higher for electron the current monotonically increases as temperature is increased owing to more and more thermionic emission of electron.

4.7 The Gate Oxide Quality

In Figure 4.16 and 4.17 we investigate the breakdown strength of our SiO_2 dielectric by measuring the leakage current between a gate terminal and a contact (Figure 4.16). In such a configuration, our circuit can be seen as a series of three resistors: the oxide gate barrier (R_{OX}), the NW itself (R_W) and the NW-contact junction (R_C). To ensure the whole potential drops across *R*OX, we switch ON the NW channel by applying a large voltage (-50 V) to the bottom-gate. This ensures that $R_W+R_C << R_{OX}$, no matter if conduction is via holes or electrons. Devices initially show a higher resistance but reach breakdown when a critical voltage (5 V) is exceeded. We, thus, see that, in our operational range

(-1 V < V_{TG} <3 V), no gate breakdown occurs and the leakage current always remains below 10 pA.

The good electrical properties shown in Figures 4.15 and 4.16 indicate the feasibility of using our self-formed SiO_2 shell as the gate oxide, avoiding the necessity for oxide fabrication by conventional methods yet achieving comparable dielectric performances. We also note that, for a shell thickness of 5 nm, a 5 V breakdown voltage corresponds to a field of 10^7 V/cm [5]. This is similar to the standard breakdown field reported for SiO2 (10^7 V/cm), indicating the high-quality of our intrinsic oxide shell.

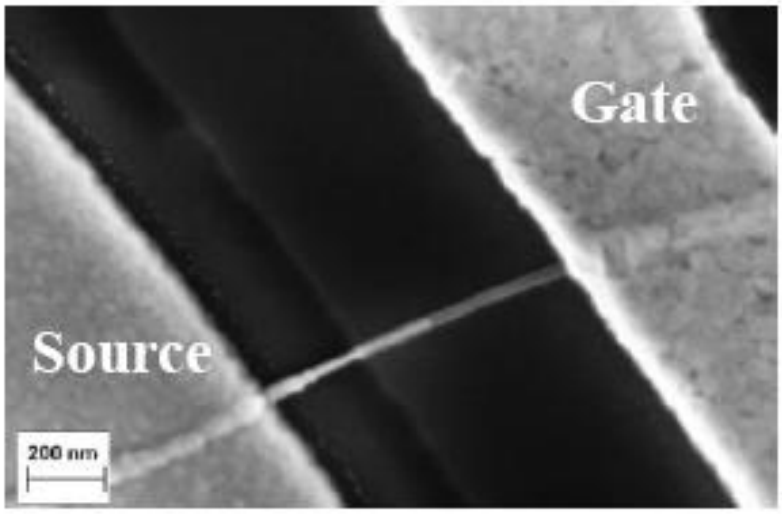


Figure 4.19: SEM image of the NW top gate region.

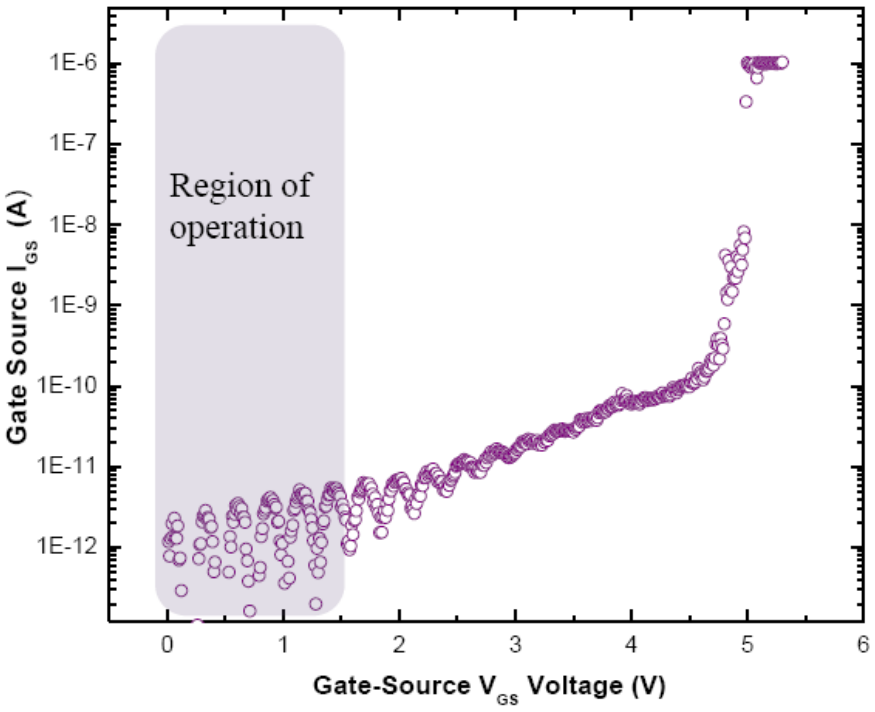


Figure 4.20: Gate to contact voltage.

4.8 Capacitance Extraction of NW

To estimate the field effect mobility, TCAD simulation was done by Synopsis Sentauras. This can estimate the capacitance more accurately than any analytical formula. Here poisson equation was solved together with drift diffusion equation to solve the electrostatic profile.

For the correct simulation, the diameter and the gate thickness was determined from the SEM of cross section of the nanowire done by Focus Ion Beam. Figure 4.17 (left) shows the cross section of the NW the circle is 15 nm that the diameter of the NW in this

case with 5 nm of SiO2 wrapping around it and Figure 4.17 (inset) is the electrostatic potential profile for this structure. Figure 4.18 gives the estimate of the simulated C-V profile for the top gated Si NW.

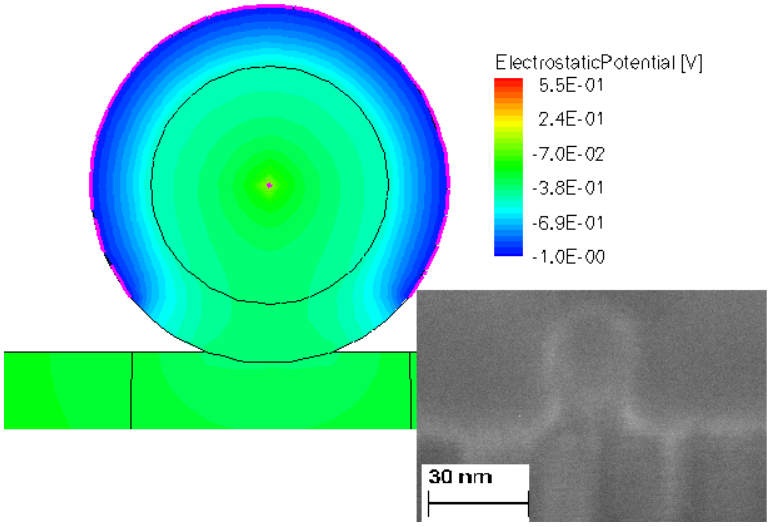


Figure 4.21: SEM iamge of X-section of SiNW under the top gate (inset).Electrostatic profile of simulated NW under the top gate.

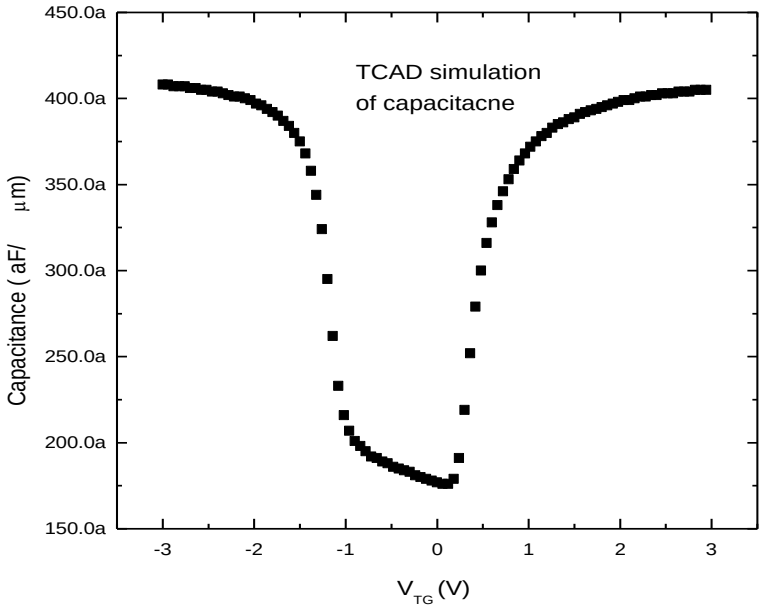


Figure 4.22: Simulated C-V characteristics of top gated SiNW.Top gate is varied from -3 to +3 V while back gate is kept at -40 V.

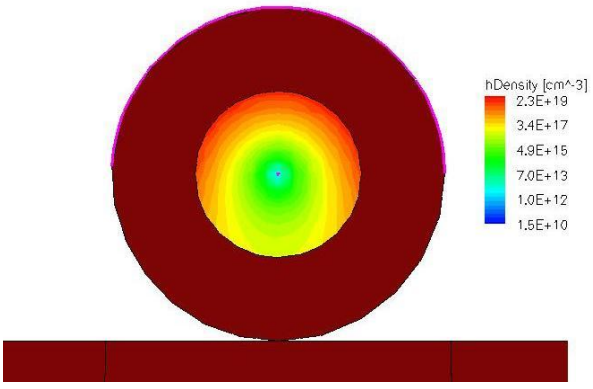


Figure 4.23: Simulated hole dendity characteristics of top gated SiNW.Top gate is at -1 to while back gate is kept at -40 V.

We did a comparative analysis why TCAD simulation for NW capacitance extraction method is better than the analytical formula based extraction..Even tough analytical for capacitance of formula for cylindrical shape object quite accurate result, but our top gate does not cover the NW cylindrically rather 80% of the circumference of the NW is covered .Thus analytical formula below gives incorrect estimation of capacitance.

$$C = \frac{2\pi\varepsilon_0\varepsilon_r L}{\cosh^{-1}\left(1+\frac{2t_{ox}}{d_{nw}}\right)} \qquad (4.1)$$

The comparison between analytical formula and TCAD based estimation is shown in the figure 4.19

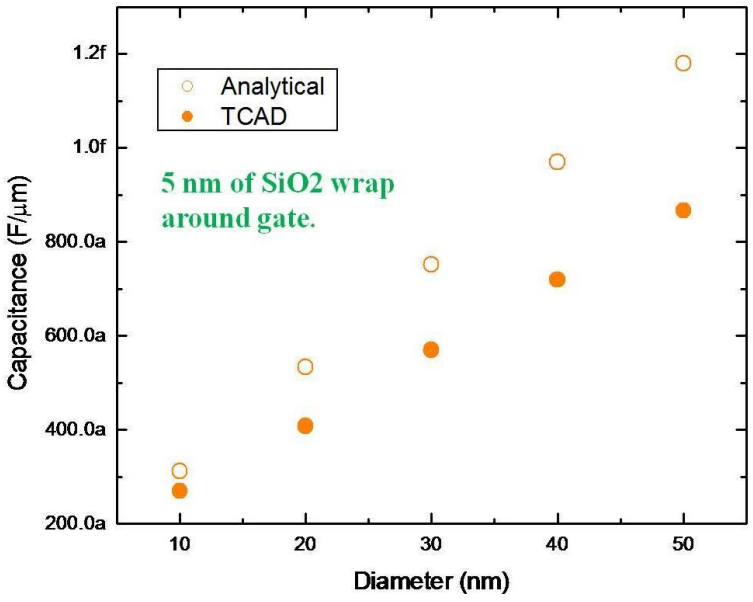


Figure 4.24: Capacitance estimation of NW by analytical formula and TCAD modeling.

4.9 Mobility Extraction of NW

Now we assess the field effect mobility for hole. We restrict our mobility extraction to hole since hole has small SB height than that of electrons and gives reasonable transconductance value. The transconductance can be written $g_m = dIds/dVgs\ |_{Vds}$ where Vds is low bias (In this case V_{ds}=50 mV).The analytical expression for mobility is

$$\mu_p = g_m \ \frac{L^2}{C_{ox}} \frac{1}{V_{ds}} \tag{4.2}$$

Figure 4.20 shows μ_p as a function of top gate Vgs. The peak mobility was found around 260 cm^2/Vs.The mobility increases first with the increment (decrement) of top gate voltage due to reduce coulomb scattering then it starts to decrease which is typical for planar MOSFET.As at higher gate voltage carriers are attracted more close to surface, mobility is effected by surface roughness, traps etc.

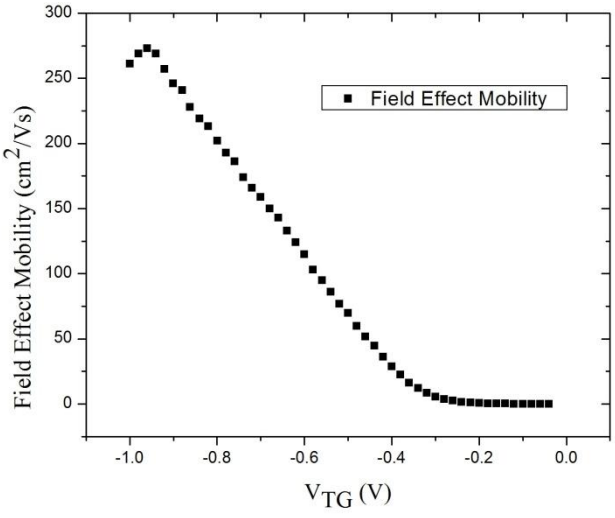


Figure 4.25: Field effect mobility (hole) as a function of top gate V_{tg}.

It should be mentioned that the electron mobility reported in this work is the so-called "field-effect" mobility, different from the effective mobility and the Hall mobility. The Hall mobility describes the bulk carrier transport where no major contributions from the surface and quantization effects whereas both the field-effect and effective mobilities represent to characterize the carrier transport in the surface inversion layer of the MOSFETs. The field-effect and effective mobility are, however, deduced from the *I-V* characteristics by using different analytical models. Specifically, the effective mobility is deduced from the drain conductance and described by 4.3 and 4.4 respectively.

$$g_D = \frac{\delta I_{DS}}{\delta V_{DS}} \tag{4.3}$$

$$\mu_p = g_D \times \frac{L^2}{C_{ox}} \times \frac{1}{(V_{GS} - V_t)} \tag{4.4}$$

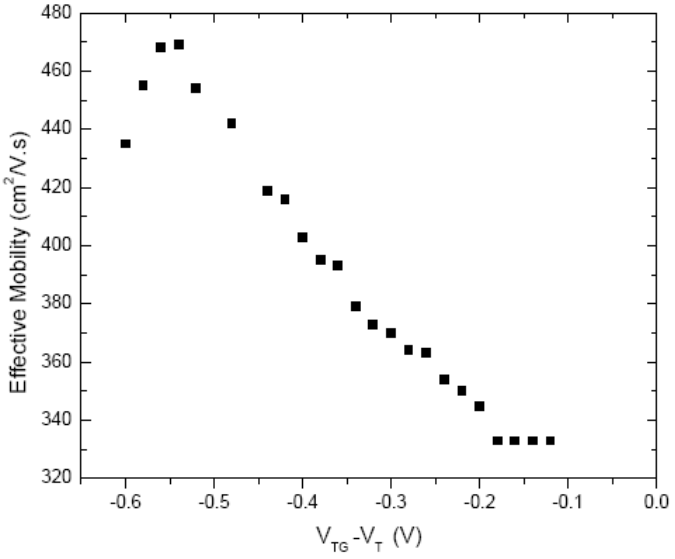


Figure 4.26: Effective mobility (hole) as a function of top gate V_{gs}.

The figure 4.22 shows the channel resistance at different top gate voltage.

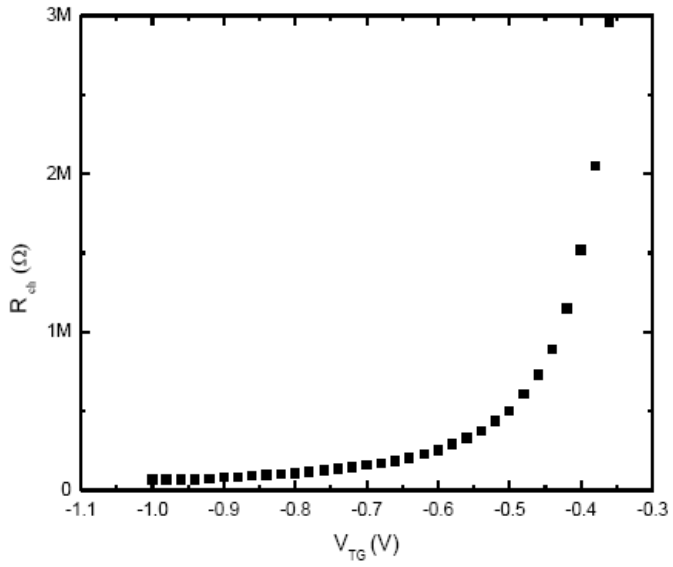


Figure 4.27: Channel resistance as function of gate voltage.

On the other hand, as described above, the field-effect mobility is deduced from the transconductance, *g*m. Therefore, the main difference between the field-effect an effective mobility is the neglect of the gate electric-field dependence in the field-effect mobility expression. For the device modeling, effective mobility is often used to predict the current and switching speeds.

4.10 Summary of the NW properties

In summary, we want to claim that our dual gated NW is superior by many properties in compare other silicon NW fabricated by other people. Here in Table 4.1 I list some very important properties which are crucial for many electronic application specially for digital application. We have achieved I_{on}/I_{off} ration of 10^7 which is on the highest side so far together with small subthreshold swing of 85 mV/decade. Our NW shows very good ON current given that diameter is only 18 nm. And hence showing small ON resistance. Even though the mobility is on higher side, but people reported even better mobility. But we employed more rigorous method of mobility extraction here.

Table 4.1: Comparison of various NW with current NW.

	This work	Walter et al	Byon	Cui	Appenzeller	Colli	Lu
Ref.		4	13	12	3	11	14
active region	i-Si	i-Si	i-Si	i-Si	i-Si	i-Si	i-Si
Lg (μm)	0.7	0.67	-	0.8-2	0.5	3	1
Diameter (nm)	20	20	20	70	60-90	20-30	20
Ron [Ω]	66 K	625 K	15 M	1.1 G	-	10 M	2.7 M
Ion/Ioff	10^7	10^7	-	-	-	10^6	
SS swing (mV/dec)	85	-	-	-	140	135	-

Table 4.2: Properties of silicon NW.

Length	**700 nm**
Diameter	**18 nm**
Threshold Voltage	**-400 mV**
Inverse Subthreshold Swing	**85- 90 mV/dec**
Ion	**1 uA**
I_{on}/I_{off}	**~10^7**
R_{on}	**66 kΩ**
Peak Field Effect Mobility (hole)	**265 $cm^2/V.s$**
Peak Effective Mobility (hole)	**470 $cm^2/V.s$**
Contact	**NiSi**
Contact Behavior	**Schottky**
Gate Delay	**19.2 ps**

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Chapter 5
Conclusions

This dissertation aims at studying transport properties of silicon nanowire as well as to investigate some of their intrinsic properties since silicon NW is a potential candidate to replace current planar MOSFET technology as it is coming down to end of the road of scaling. Even if the CMOS industry need some top-down approach to make large array of orderly device to make functional chip, it is beneficial to study single bottom-up based grown nanowire as it could shed light on transport physics , electronic , thermal and mechanical properties.

In this work, I fabricated dual gated silicon nanowire which has both global back gate and top gate. Two gates gives us more room to play with its electronic properties. NW devices of various length, diameter are fabricated on degenerately doped silicon substrate with 300 nm of silicon dioxide on it serving as global back gate oxide. Electron beam lithography is extensively used to make pattern of drain, source and gate contact.

I have demonstrated superior Ion/Ioff ratio of 10^7 which so far one of the best reported for silicon NW devices. I also showed very good subthreshold swing of 85-90 mV/decade with 5 nm of silicon dioxide gate oxide thickness which is also at the best end. The devices show very low ON resistance of 66 K ohm.

Another important issue in this dissertation is mobility extraction method. I have employed TCAD based simulation for estimating capacitance of NW instead of using any analytical formula. It is very difficult to measure the capacitance of NW since they are in fF range. Hence people use analytical formula to estimate the capacitance which gives incorrect estimation for top gated NW device. So I modeled the NW in TCAD sentaurus software which is finite element based solver that can solve Poisson , Boltzman and many other equation simulatenously. With this TCAD modeling I have estimated capacitance of NW more accurately which give more accurate mobility calculation.. I have estimated peak field effect mobility for hole around 260 $cm^2/V.s$ .People have reported a wide range of mobility for silicon NW. But here I implemented rigorous method to extract mobility.

I have also simulated NW device in TCAD to shed light on the transport physics. Since I used 2D modeler but real NW has 3D structure, it was not possible to match the result exactly but we have the same pattern for transfer curves that can be compared qualitatively.