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**NUCLEAR
INSTRUMENTS
& METHODS
IN PHYSICS
RESEARCH**
Section A

Architecture of the BABAR Electronics System

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Abstract

An overview of the Electronics System for the BABAR Experiment, emphasizing architectural issues and development of new components, is presented. © 1998 Published by Elsevier Science B.V. All rights reserved.

The BABAR Experiment will study CP violation at the SLAC B-Factor. Its detector consists of five major systems: a silicon vertex tracker [1], a cylindrical drift chamber with dE/dx capability [2], a particle identification system (DIRC) based on imaging of Cherenkov rings [3], a cesium-iodide crystal calorimeter [4], and a muon identification system (IFR) based on resistive plate chambers [5]. The specialized requirements of each detector system are addressed by front-end electronics customized to the detector technology but integrated into a uniform data acquisition architecture.

1. Overview of architecture

BABAR has adopted a two-level trigger and data acquisition architecture. At Level 1, the trigger is optimized for simplicity and speed. It is based on a reduced set of detector data from the drift chamber and calorimeter. It consists of a pipelined, hardware processor and is nearly without deadtime. Its latency is 12 μ s, and it is designed to provide an output trigger rate of less than 2 kHz. During the level 1 latency, the full detector data sample is held

in circular buffers. At the final level, which is referred to as Level 3, the data acquisition system assembles events over a commercial network into the memory of a farm of level 3 processors. The level 3 output rate is expected to be about 100 Hz. The level 3 trigger, or Online Event Processor, performs final event selection in commercial CPUs working with the complete set of detector data. The level 3 trigger is followed by on-line prompt reconstruction in the same farm. The architecture is designed to accommodate an optional Level 2, if unexpected background conditions demand higher performance.

Although BABAR's architecture greatly resembles that designed for high-rate hadron colliders such as the LHC, it includes some unusual characteristics. The 12 μ s level 1 latency is relatively long, but can be accommodated because all level 1 latency buffers are digital. Long latency simplifies and reduces the cost of the level 1 trigger. A minimum level 1 trigger spacing of 2.2 μ s is enforced. This spacing simplifies logic design of the readout ICs, because each datum in the silicon tracker and drift chamber is then associated with a single level 1 accept, whereas it introduces minimal deadtime,

0.4%. BABAR has no fast counters for triggering purposes, and bunch crossings are nearly continuous at 4 ns. Hence, the timing of the trigger must be derived from the chamber, as part of track segment reconstruction, and from the calorimeter, as part of waveform processing. The resolving time of the trigger is about 150 ns worst case. A window of data covering several times this value plus the detector resolving time is read out for each detector. For instance, this window is about 500 ns wide for the silicon vertex tracker and 4–16 μ s wide for the calorimeter. The event time is determined off-line from this data.

2. Detector-specific electronics subsystems

All detector-specific, or front-end, electronics subsystems of BABAR share a common architecture. Each front-end chain consists of an amplifier, digitization (discriminator or flash ADC), a circular buffer (to store data during level 1 latency), and a derandomizing buffer (to store data between level 1 accept and transfer to a Readout Module). Analog signal processing, digitization, and data readout occur simultaneously. All front-end subsystems except the IFR provide data sparsification. All level 1 latency buffers are digital; hence, it is possible to store data longer than analog buffers would allow. The buffers of all front-end systems are managed by a common protocol. All level 1 latency buffers function as pipelines of fixed length, and all derandomizing buffers function as FIFOs which are capable of storing a fixed number of events, regardless of the actual implementation of the buffers. Each detector-specific subsystem also shares standard BABAR interfaces to the detector-spanning, or common, electronics subsystems. In all cases, the front-end electronics is mounted directly on the detector for performance reasons. This solution also substantially reduces required cable plant. The design of each detector-specific subsystem balances its individual and common requirements in order to achieve a cost-effective, robust, and easy to maintain implementation. Custom-integrated circuit solutions have been adopted for most subsystems.

The Silicon Vertex Tracker (SVT) Electronics must record hits with coarse (\sim 4-bit) pulse height

resolution for 150 000 silicon strips. A readout IC [6,7], in radiation-hard 0.8 μ m Honeywell CMOS, integrates all functionality between the strip and 60 Mbps serial readout links. It provides low-noise amplification and shaping, with programmable time constants to adjust shaping to detector capacitance and hit rates. It records pulse height using a time-over-threshold technique. It also provides level 1 buffering, sparsification, derandomizing buffer, and readout control logic.

The Drift Chamber Electronics must measure drift time and dE/dx for 7104 small drift cells. Drift time resolution of 2 ns and pulse height measurement with dynamic range of 6 bits are required. In addition, prompt hit cell information must be provided for the level 1 trigger. The electronics is mounted on the chamber endplate opposite the center-of-mass boost. A four-channel amplifier IC [8] in Maxim CPi semi-custom bipolar provides analog and discriminated outputs. An eight-channel digitizer IC [9–11] in Hewlett Packard triple-metal 0.8 μ m CMOS provides a TDC with 1 ns bins and a 15 MHz, bilinear, 6-bit flash ADC for each channel. The digitizer IC also provides level 1 buffering, derandomizing buffer, and sparsification.

The Particle ID (DIRC) Electronics must measure single photoelectrons from Cherenkov light sensed by 10 752 photomultiplier tubes. Time precision of at least 1 ns is required in order to reject background. Amplitude resolution of 6 bits is required for gain calibration. Photomultiplier signals are received by Front-end Boards in crates mounted inside magnetic shielding for the PMTs. Eight-channel analog ICs [12] in AMS 1.2 μ m CMOS provide zero-crossing discriminators for timing and a multiplexed analog output for pulse height measurement on a sampling basis. Digital ICs [13] in ES2 double-metal 0.8 μ m CMOS contain TDCs, buffers, and sparsification for 16 channels.

The Calorimeter Electronics must measure pulse height with very low noise (\sim 500e) and large dynamic range (18 bits) for 13 320 photodiodes on 6 660 CsI crystals. In addition, it must tag the time of event data and provide prompt energy sums to the level 1 trigger. Redundant low-noise, charge-sensitive amplifiers are mounted on the

crystals. The amplifier is based on a single-channel Amplifier IC in AMS 1.2 μm BiCMOS with split-range output. The two outputs of each amplifier are fed to a four-crystal calorimeter auto-ranging and encoding (CARE) IC [14] in AMS 1.2 μm BiCMOS which provides large dynamic range via four amplitude scales multiplexed to a 10-bit flash ADC.

The Instrumented Flux Return (IFR) Electronics [15] must record hit strips for 50 000 channels of resistive plate chambers (RPCs) and associate the hits with the level 1 trigger. RPC strips are read out via 16-channel Front-End Cards (FECs) which discriminate and delay the signals during the level 1 latency. FECs are read out in groups of 64 by FIFO Boards, which are located in crates mounted on the flux return iron. TDC Boards provide precise timing information on groups of RPC strips.

3. Data acquisition

All elements of BABAR front-end electronics are controlled via BABAR-standard protocols on BABAR-standard serial links. 60 Mbps control streams are time-division multiplexed in groups of 16 by Readout Modules onto 1 Gbps fiber control links which transport the control stream to transition cards on the detector. The transition cards derive the 60 MHz system clock, demultiplex the 60 Mbps control data, and distribute these signals to the front-end electronics along point-to-point crate backplanes to the DIRC and IFR and via direct connections to the SVT, drift chamber, and calorimeter. This path transports both timing and slow control. The standard data path from detector-mounted electronics to Readout Modules is parallel to the control path. Groups of 16 serial data streams, up to 60 Mbps, are multiplexed by the transition cards onto 1 Gbps fiber data links. Data streams are demultiplexed and buffered on the Readout Modules. The standard readout protocol allows for both fixed and variable length records. This path is used for both event data and read back of registers. The calorimeter uses a separate set of Gbps links for its large data volume.

A single Readout Module (ROM) design, with two Personality Card types, serves all detectors. It

provides the standard interfaces, deep event buffers, and a processor (300 MHz PowerPC604e or higher). Its implementation consists of a commercial single-board VME computer with PCI mezzanine slots plus two custom boards. Together these two boards provide a DMA interface between the standard BABAR data and control links and PCI, via a PCI/i960-bus bridge. The Controller Card provides a fast control and timing interface and manages front-end buffers. The Personality Card multiplexes and demultiplexes the control and data streams, provides the electro-optical interface, and provides intermediate storage of events. Two types of Personality Card exist. The standard (triggered) Personality Card receives data from detector-mounted electronics in response to a level 1 trigger accept. It is used by all subsystems for control and by all but the calorimeter for event data. An untriggered Personality Card interfaces to the untriggered Gbps data streams of the calorimeter and provides a triggering mechanism such that calorimeter data is presented in the same way as other detector data to the CPU. The commercial CPU and the two custom boards assemble into a single-slot $9\text{U} \times 400\text{ mm}$ VME card. The ROM runs a real-time operating system, VxWorks, and provides a well-supported coding environment.

Segments of event data are read out from ROMs over VME by a crate-level processor. This processor, a ROM without links to front-end electronics, assembles segments into larger event *fragments*. From the crates, fragments are assembled into *events* over a commercial switching network. Studies have established that FDDI can provide adequate bandwidth for BABAR's modest (~ 50 Mbps) bandwidth. Fast Ethernet and ATM are now being investigated as more suitable, and enduring, networks. The BABAR data acquisition system consists of 128 ROMs in 22 VME crates. The DAQ system is partitionable at the crate level such that any combination of subsystems or crates can run independently and autonomously with any combination of triggers.

4. Summary

BABAR has designed a pipelined, and nearly deadtime free, trigger and data acquisition

architecture. The design is highly standardized across detector-specific subsystems, providing standards for buffer architecture, links and protocols for readout and control, Readout Module, and interfaces to timing, DAQ, and controls. Seven custom ICs have been developed to realize the full performance of detector systems. Prototypes of all components presently exist and demonstrate requisite performance. BABAR installation will occur in mid-1998, and data taking will commence in early 1999.

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