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$YBa_2Cu_3O_{7-\delta}$-CeO_2-$YBa_2Cu_3O_{7-\delta}$ Multilayers Grown by Reactive Co-Evaporation on Sapphire Wafers

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***Abstract*—High-T_C superconductor thin film heterostructures were deposited using reactive co-evaporation for dual layer electronic applications. The epitaxial structure consisted of 35-nm $YBa_2Cu_3O_{7-\delta}$(YBCO), 75-nm CeO_2, 150-nm YBCO, and 20-nm CeO_2 on *r*-plane sapphire wafers. The critical temperature was measured to be 83.6 K and 84.8 K for the bottom and top YBCO layers, respectively. Atomic force microscopy reveals smooth surfaces with RMS roughness of the top YBCO layer to be 4.7 nm. The CeO_2 insulating layer exhibited hopping conduction that freezes out at low temperature, making these structures suitable for electrical circuits with isolated ground planes.**

***Index Terms*—Multilayer, heterostructures, YBCO, CeO_2, reactive co-evaporation.**

I. Introduction

HIGH-TEMPERATURE superconductors (HTS) are promising candidates for superconducting electronics operating at elevated temperatures. Improvements in the ability to grow, pattern and interconnect multiple HTS layers are needed, in particular at the commercial wafer scale level. Several applications would greatly benefit.

HTS SQUID magnetometers can achieve high sensitivity through integration with multi-turn flux transformers which require vias and crossovers between layers [1]. This allows the primary and secondary coils to cross over one another to maintain a continuous superconducting loop. Ground planes are needed for high frequency RF electronic applications and those that require low sheet inductance, such as single flux quantum (SFQ) logic circuits [2].

For optimizing SFQ circuits, inductance is especially important because the product of inductance and the Josephson junction critical current (I_C) must be of the order of the flux quantum (Φ_0). This is essential so that only a single flux quantum can be stored or processed per each SFQ cell. At the temperatures where HTS SFQ operate, I_C must be higher than that used in low temperature SFQ to suppress thermal noise, which is necessary for maintaining a low bit-error-rate. Larger values of I_C increase the need for small HTS sheet inductance. In prior work, comparing multilayer devices prepared by pulsed laser deposition, Terai *et al.* showed that the inductance can be lowered by almost three times through the inclusion of a superconducting ground plane [3].

Several other previous studies have also been performed on HTS multilayers grown by PLD using both $SrTiO_3$ [4], [5], and CeO_2 [6] as the insulating layer. These works clearly demonstrated the potential of multilayer stacks, however there is still a need for a larger scale commercial process.

Controllable high quality multilayer structures could lead to the realization of more complex multilevel circuits such as those fabricated using Nb-Al_2O_x-Nb Josephson junctions [7], [8]. However, there are still many challenges that need to be overcome to bring this to fruition, such as large area growth of HTS epitaxial thin films with small surface roughness, high critical current density (J_C) and high-transition temperature (T_C). Furthermore, there is a need for isolation of multiple layers with no leakage. These properties are intertwined and are important to be optimized simultaneously. For example, if surface roughness is not minimized, pinhole shorts will occur through the insulating layer. Therefore, it is important to investigate and examine the properties of a thin electronics grade HTS layer with an isolated ground plane grown with a commercial deposition process.

Commercial production of very high quality films has been available for decades using reactive coevaporation (RCE) [9]. In the RCE process, metallic elements such as yttrium, barium, and copper, (in the case of YBCO) are thermally evaporated from resistive sources onto a substrate attached to a rotating plate that revolves at 5 Hz, cycling the wafers between the evaporation vacuum chamber at 7.5×10^{-6} torr (1 mPa) and a higher

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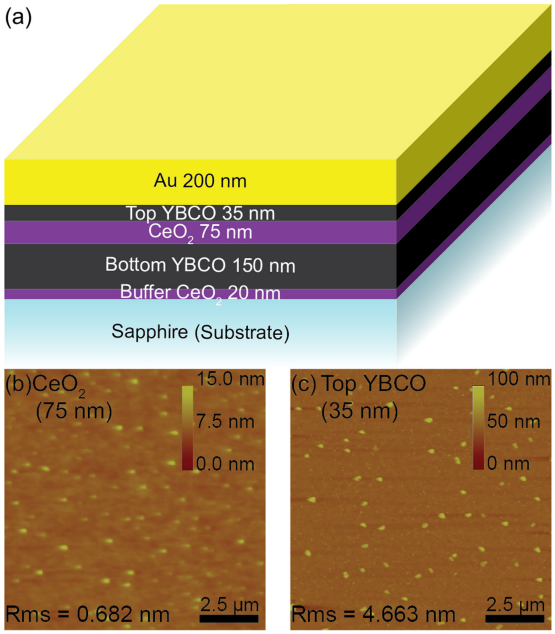

Fig. 1. (a) Schematic illustration of the multilayer structure consisted with 200-nm Au, 35-nm top YBCO, 75-nm CeO_2, 150-nm bottom YBCO and 20-nm CeO_2 buffer layer on sapphire substrate. (b) 75-nm CeO_2 surface topography scanned by AFM. (c) Top 35-nm YBCO surface topography scanned by AFM.

pressure oxygen "pocket" blackbody heater at 7.5×10^{-4} torr (0.1 Pa) [9]. The evaporation rate of the metal sources are monitored using quartz crystal micro balances with collimators to keep the accuracy within 1%. Moreover, the growing temperature at 650 °C is about 150 degrees lower in temperature than other techniques. Lower temperature decreases the possibility of the film cracking upon cool down [10], [11]. It also minimizes the formation of inter-metallic phases such as $BaCeO_3$.

RCE HTS coated substrates have been routinely produced in large numbers for commercial purposes. When the films stoichiometry is precisely tuned very smooth ultra thin films with thickness of the order of a few tens of nanometer can be produced for electronics grade material. Another key advantage to RCE is that the deposition area can be very large and the nature of the rotating pocket heater facilitates deposition of many wafers simultaneously or very large wafer sizes [9].

In this work, we grow and investigate the properties of a thin electronics grade HTS layer with an isolated ground plane grown with RCE for multilayer wafer production.

II. Experiments and Results

A multilayer heterostructure consisting of 35-nm YBCO, 75-nm CeO_2, 150-nm YBCO and 20-nm CeO_2 (top to bottom) on *r*-plane sapphire was grown at Ceraco GmbH using RCE as shown in Fig. 1(a). In our hetreostructures, the layer thicknesses were chosen to be optimized for Josephson devices with junctions fabricated using the focused helium ion beam process (FHB) [12] in the top layer. Using FHB, high quality nanoscale devices can be created, but they require very smooth and thin films (35 nm) [13], [14].

The thickness of the bottom YBCO ground plane layer was chosen to be of the same order of the penetration depth of YBCO to ensure that the ground plane can shield effectively. For the insulating CeO_2 layer, the thickness is maximized while keeping the total multilayer thickness under 300 nm to prevent cracking of which is common in films grown on sapphire.

For our multilayer structure, five 2" r-plane sapphire wafers were placed at the center of the plate(n) for deposition. First a 20-nm buffer CeO_2 layer was grown followed by a 150-nm thick YBCO film to serve as the bottom ground plane. In order to make the film as smooth as possible, to prevent pinhole shorts through the subsequent layers, the copper content was reduced. This eliminates copperoxide precipitates on the surface at the expense of a reduced T_C and J_C. Second, a 75-nm CeO_2 layer was deposited, and the T_C and J_C of the bottom YBCO were measured to be 83.6 K and 1.0 MA/cm^2 respectively using an inductive Cryoscan.

The wafers were returned to the vaccum chamber along with an additional CeO_2 buffered sapphire test substrate and a 35-nm thick YBCO layer was grown followed by a 200 nm gold contact layer. For this deposition the copper content was increased to obtain better electrical properties. Following this second deposition T_C and J_C were measured to be 84.8 K and 2.3 MA/cm^2 using a cryoscan of the test substrate. A third cryoscan of the hetero structure exhibited a J_C of 1.2 MA/cm^2 for the two layers combined. Assuming a J_C of 1.0 MA/cm^2 for the bottom layer and 2.3 MA/cm^2 for the top layer, one would expect for the double layer a J_C of (1.0 MA/cm^2 $\times$ 150 nm + 2.3 MA/cm^2 $\times$ 35 nm)/185 nm = 1.25 MA/cm^2, consistent with the measured value 1.2 MA/cm^2 of the stack. This suggests that the quality of the 35-nm YBCO on top of the CeO_2/YBCO is similar to the film on the test substrate.

To characterize the surface morphology, atomic force microscopy (AFM) was used to inspect the surfaces. To scan the top YBCO surface, the gold capping layer is removed with KI-I^+ gold etch. The insulating 75-nm CeO_2 surface topography is acquired from the samples removed from the chamber after the 75-nm CeO_2 deposition. The YBCO top layer and CeO_2 surfaces were both smooth with the exception of a small number of particles on the top YBCO surface as shown in 1(b) and (c). Large scale defects were not observed. Surface roughness was determined to be 0.7 nm and 4.7 nm for the CeO_2 and top YBCO respectively.

Resistivity as a function of temperature was measured for each layer using a 4-point Van der Pauw geometry and lock-in amplifier. The results are shown in Fig. 2. To access only the bottom layer for this measurement, the top YBCO layer is fully removed with phosphoric acid and the insulating CeO_2 layer is scribed through to make contact with bottom YBCO layer.

Both layers exhibit sharp transitions with residual resistivities of 22 $\mu\Omega$-cm and 35 $\mu\Omega$-cm for the top and bottom layers respectively which suggest that there is low temperature independent defect scattering. We remark that the top YBCO shows an apparent room temperature resistivity of 500 $\mu\Omega$-cm that is much larger than the ground plane layer resitivity of 275 $\mu\Omega$-cm. We interpret this result to be due to an overestimate of the electrical thickness of the top layer. Process damage, surface roughness

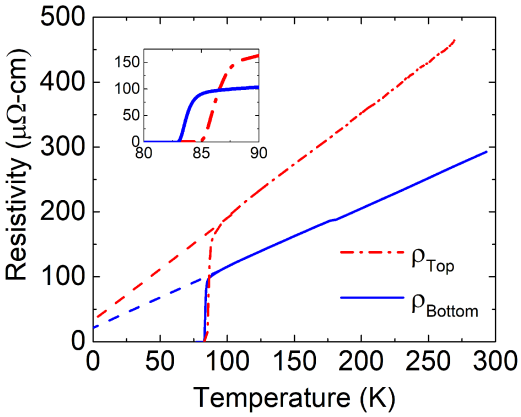

Fig. 2. Resistivity-Temperature of top YBCO layer (red dash dot line) and bottom YBCO layer (blue solid line), and the red and blue dash lines are extrapolations for residual resistivity of 22 $\mu\Omega$-cm and 35 $\mu\Omega$-cm of top and bottom YBCO layer respectively. The curves are zoomed in around transition in the inset.

and a possible dead layer at the CeO_2 interface likely contribute to a reduction of the electrical thickness. Assuming that the actual resistivity of the two layers is the same yields a reasonable electrical thickness of 20 nm for the top layer.

To characterize the electrical properties of the CeO_2 insulating layer to test for the presence of pinhole shorts we prepared the samples for a four-point resistance measurement. In order to make contact with the buried YBCO, a 3 mm diameter circle was printed on top of the sample using photolithography. The pattern was transferred into both gold and the top YBCO layer by chemical etching with KI-I^+ and 0.1% phosphoric acid respectively. The CeO_2 layer was etched using a 500 V argon ion mill. To ensure proper milling down to the bottom YBCO layer, electrical continuity was tested between the bottom contacts and the etch step height of the stack was measured to be 320 nm with a KLA Tencor P-7 profilometer in the inset of Fig. 3.

Four electrical contacts were attached to the sample for a four-point measurement. Two contacts were attached to the top Au electrode and the other two were attached to the bottom YBCO layer with silver paint. Current as a function of voltage ($I-V$) was measured by using a function generator to drive the sample and a series resistor at 1 Hz. Low noise preamplifiers were used to measure the voltage across the CeO_2 (V) and the series resistor (I). Curves were continuously recorded and the sample was cooled to low temperature. Selected curves are shown in Fig. 3(a) for a series of different temperatures. At room temperature, the insulating layer appeared ohmic with a resistance of 351 Ω. However as temperature was reduced below 200 K non-linearity was observed (Fig. 3(a)).

To investigate the temperature dependence further we calculate the resistivity assuming a uniform current density through the patterned area from the resistance obtained from data in Fig. 3(a) and the result is plotted for several voltages in Fig. 3(b). We observe a strong dependence of the resistivity on both temperature and voltage that is reminiscent with variable range hopping transport. We note that the appearance of our data to approach an asymptotic value at low temperature is likely an artifact from using a measurement voltage much greater than the

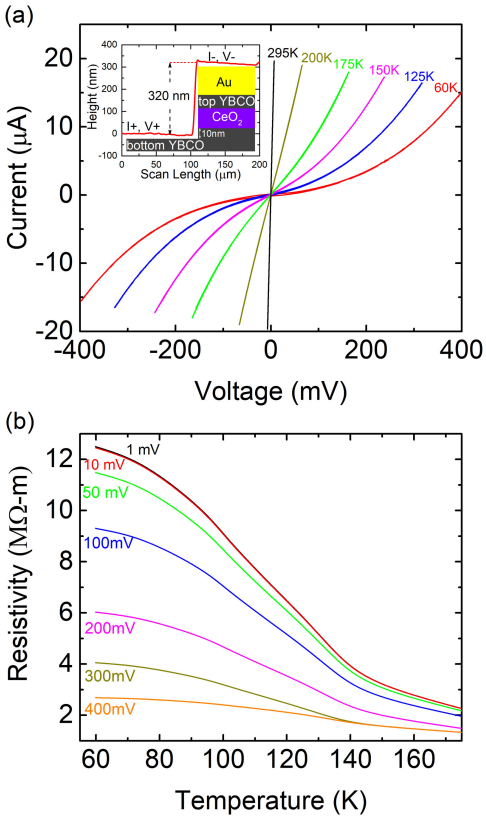

Fig. 3. (a) Current-Voltage across 75-nm CeO_2 insulating layer measured at different temperatures. The inset is the step height obtained by the profilometer to ensure etching was through the layers. (b) Resistivity-Temperature of 75-nm CeO_2 insulating layer obtained from (a) for different constant voltage ranges.

thermal energy k_BT. From these large area measurements we conclude that there are no pinhole shorts through the dielectric and that the transport mechanism is thermally activated variable range hopping.

III. Conclusion

In conclusion we have investigated superconducting YBCO-CeO_2-YBCO thin films in multilayer heterostructures grown by reactive co-evaporation. Both the top 35-nm and the bottom 150-nm YBCO layers have high transition temperatures at 83.6 K and 84.8 K and large critical current densitys with moderate surface roughness. The CeO_2 insulator exhibited activated transport but provides substantial insulation with resistivty of 11.5 MΩ-m at 77 K. While additional structural characterization such as XRD and transmission electron microscopy could yield more insight into the quality of these structures electrically these films look very suitable for thin film electronics. This is another step forward towards a large scale commercial multilayer RCE process for HTS electronics. In the future, we envision the incorporation of vias and crossovers for more complex integrated YBCO circuits.

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