Title

High-efficiency and Ultra-fast Photodetectors in the Visible and Near-infrared for Optical Communication, Sensing, and Imaging Applications

Author

Mayet, Ahmed

Publication Date

2023

Peer reviewed|Thesis/dissertation

High-efficiency and Ultra-fast Photodetectors in the Visible and Near-infrared for Optical Communication, Sensing, and Imaging Applications

By

AHMED S. MAYET

DISSERTATION

Submitted in partial satisfaction of the requirements for the degree of

DOCTOR OF PHILOSOPHY

in

Electrical and Computer Engineering

in the

OFFICE OF GRADUATE STUDIES

of the

UNIVERSITY OF CALIFORNIA

DAVIS

Approved:

_____

M. Saif Islam, Chair

_____

Jerry Woodall

_____

Erkin Seker

Committee in Charge

2023

Abstract

Over the last five decades, there has been continuous development in the field of optical communication and sensing applications. Timely development of cost-effective, power and absorption efficient, low-noise and ultra-fast optical interconnects/sensors is crucial to meet the high demand for data transfer in the era of the Internet of Things (IoT), augmented reality (AR), virtual reality (VR), light detection and ranging (LIDAR), quantum communication, biomedical imaging and emerging applications that are expected to connect billions of devices/sensors with different functionalities. Datacenters are envisioned to scale up to meet the high connectivity demand as big data and cloud computing continues to grow exponentially. Intra- and inter-datacenter communications require optical links for reach gap (500 m–2 km), long-reach (~10 km), and extended-reach communications (up to 40 km), which requires optical transceivers/PDs that work in a wide range of the optical spectrum. In a surface-illuminated PD, high speed and high efficiency are often a tradeoff since a high-speed device needs a thin absorption layer to reduce the carrier transit time. In contrast, a high-efficiency device needs a thick absorption layer to compensate for the low absorption coefficient of some semiconductors such as Si Germanium (Ge), GaAs, and InGaAs at wavelengths near the bandgap.

This thesis presents the recent development in enhancing the photon–material interactions by utilizing photon-trapping (PT) nanostructures that can control light for more interaction with the photoabsorbing materials, slow down the propagation group velocity and reduce surface reflection. Since ultra-fast PDs suffer from low optical absorption, photon-trapping nanostructures can be utilized to enhance their efficiency. We demonstrated that a perpendicular light beam could be bent to allow guiding parallel to the surface of the PDs, greatly enhancing the interaction of light with the absorption material, which allows for improving broadband absorption by photon manipulation. Consequently, the speed of carrier collection can be increased by designing a thin absorbing layer with a reduced transient time without losing the sensitivity of the PD. Another

advantage of developing PT nano-designs is to reduce the junction capacitance by decreasing the junction area. That helps reduce RC time, which is one factor limiting a photodetector's speed. The capacitance reduction in designed PT PDs results in faster response compared to its counterpart without PT PDs. Additionally, thinner absorbing material with integrated PT nano-designs could also help to reduce the bulk dark current, which is one of the noise components in the PDs. Different passivation methods were applied to improve the surface damages/traps to achieve low leakage of less than 1 nA. Moreover, photon-trapping designs add another parameter to guide the light to a specific preferential depth to maximize the gain bandwidth and absorption efficiency in PDs.

This thesis presents the modeling, fabrication, and characterization of various photon-trapping designs in Si, Ge, III-V, and quantum-well PDs. Si photon-trapping PDs enable the development of efficient ultra-fast PDs suitable for monolithic integration with CMOS electronics for the short-reach (850 nm) multimode optical data links used in datacom and computer networks. Such an all-Si optical receiver offers great potential to reduce the cost of short reach, <300 m optical data links in data centers. Additionally, Ge-on-Si PT PDs have the potential to be monolithically integrated with CMOS/ BiCMOS ASICs. Si and Ge-on-Si photon-trapping per pixel designs are presented, which show high absorption efficiency and enable high-performance CMOS image sensors. The unique response of the Si photon-trapping PDs paves the way for computational imaging development and spectroscopy on chips utilized for biomedical applications. In addition, highly sensitive photon-trapping Avalanche Photodetectors (APDs) and Single Photon Avalanche Photodetectors (SPADs) are designed with low noise, high gain, and ultra-fast characteristics. The monolithic integration of Si and Ge-on-Si offers low-cost packaging solutions and allows low parasitics, resulting in high-performance on-chip detection. Ge-on-Si, InGaAs, III-V quantum-well PT PDs can be utilized for short- and long-reach communication at intra- and inter-datacenters, passive optical networks, LIDAR, and quantum communication systems, as well as enhancing the capacity of long-haul DWDM systems beyond the L band. III-V PT PD modeling is presented

to enhance their bandwidth to meet future THz optical detection and communication demand in the C and L bands and other emerging applications.

Acknowledgments

First and foremost, I am thankful to Allah (GOD) for giving me the strength, knowledge, ability, and opportunity to complete this research study. I want to thank all the people, colleagues, and institutions for making this research possible. I want to express my deepest gratitude to my advisor Prof. Saif Islam for his inspiration, patience, valuable time, and continuous support during my Ph.D. study and research. His advice and encouragement to seek innovative ideas inspired me to continue this adventure. He taught me important scientific principles, but more importantly, he showed me how to approach research effectively and the value of using science and technology for the good of society. I will carry these teachings with me throughout my career. I want to express my sincere gratitude to the academics and researchers whose passion for science motivated me to elevate the quality of my work and offered wise advice, valuable feedback, scientific analysis, and direction. I would like to take this opportunity to express my sincere gratitude and appreciation to Prof. Jerry Woodall for his support, which has greatly influenced me, and I am grateful for his kind guidance and suggestions. My interaction with him was an enriching learning experience for me. I am thankful to Prof. Erkin Seker, who taught me important concepts of nanofabrication, Micro- and Nano-technology in Life Sciences, and advised me on my research projects. He also gave me academic advice, and I am grateful for that. I am also thankful to the professor who was part of my qualifying exam, Prof. Laura Marcu from the Biomedical Engineering department, who was an important part of this work and allowed me to explore biophotonics and bioimaging research areas. I would like to thank Prof. Diego Yankelevich for his support, analysis, and guidance. The concepts I have learned from all of the committees and instructors who taught me during my Ph.D. program have been critical for developing this research and my professional career. I thank all of you for challenging me and supporting me with your valuable feedback. Your valuable comments and suggestions gave me a better understanding of my Ph.D. research area. I am very grateful to all of you.

Special thanks to the outstanding scientists at W&Wsens, Prof. Shih-Yuan Wang, Prof. Aly F. Elrefaie, Prof. Toshishige Yamada, and Prof. Ekaterina Ponizovskaya Devine for their support, analysis, and their suggestions related to optical receivers, their applications, and challenges. I want to thank my friends and colleagues of the Integrated Nanodevices and Nanosystems Research (Inano Lab), from whom I learned essential research skills, who gave me technical advice, and who provided me with stimulating discussions and analysis. In no particular order: Dr. Soroush Ghandipharsi, Dr. Cesar Bartolo-Perez, Prof. Ahmed Kaya, Dr. Wayesh Qarony, Dr. Amita Rawat, Ahasan Ahamad, Dr. Hilal Cansizoglu, Dr. Yang Gao, Dr. Busra Ergul, Lisa Mcphillips, Howard Mao, Xuzhi He, Dr. Daniel M. Dryden, Dr. Kazim Gurkan Polat, Sicong Yu,

Mauricio Tavares, Dr. Jun Gou, Dr. Hossein Rabiee Golgir, Dr. Badriyah Alhalaili. I am honored to have such successful scientists assess and colleagues in my research work. I would like to recognize the staff members of the UC Berkeley and UC Davis Nanofabrication facilities for their assistance during the fabrication of devices. Special thanks to the UC Davis Nanofabrication staff for all their help and support. I am grateful to the Institute for Innovation and Entrepreneurship at the Graduate School of Management (GSM) for letting me be part of the business development Fellowship Program. I would like to thank all the instructors who taught me valuable concepts during the program. My Ph.D. studies and research would not have been possible without the scholarship support from the Saudi government. I am incredibly grateful with special and many thanks for all their unconditional support, help, and cooperation. Special thanks to the Saudi educational institutions and Taibah university for all their ultimate help and support. I am forever indebted to my family, who always supported me in pursuing my passion for research. Special thanks and deepest gratitude to my beloved parents, siblings, wife, child, and all my family for their unlimited support, encouragement, patience, and care, this work is dedicated to you all. I want to thank all my friends and colleagues for their encouragement and support. Also, thanks to all the awesome staff at the Department of Electrical and Computer Engineering at UC Davis, who helped me during my studies. I enjoyed being a member of a bigger family in our research lab at UC Davis. Finally, a special thanks to the University of California, including the engineering college, and graduate studies, for all their support, encouragement, and help during my research and graduate program.

Contents

List of Figures

List of Tables

Chapter 1 Introduction

The growth of distributed computing, cloud storage, social media, device-to-device (D2D) communication, and affordable portable devices currently allow extreme ease of transferring a plethora of data, including videos, pictures, and texts, over the globe. We are only at the beginning of a new era that promises unprecedented quality of life in a healthier, more secure, highly connected, and efficient way. Autonomous vehicles, smart houses with smart appliances, smart sensors, device-to-device (D2D) communication, and intelligent infrastructures will be the norms of future living. Networking of these devices, namely, the Internet of Things (IoTs) and D2D communication, will bring along big data that needs to be transmitted, stored, and analyzed more efficiently and securely [1, 2]. Thus, the transformation of the current data centers is inevitable to meet these demands. Building many mini data centers and/or scaling up the existing ones will require technology development for high-capacity network data transmission [Fig. 1][3]. The enormous number of connections with low latency will require receivers with high bandwidth and high efficiency together with minimal power consumption. To keep up with the demand in data traffic, existing copper wire interconnects utilized in data centers need to be fully replaced by ultra-fast and low-cost optical fiber interconnects [1, 4].

1.1 Global IP Traffic Trend and Forecast

Annual IP data traffic worldwide is growing exponentially, increasing the reliance on data centers. According to Statista, the actual and the forecasted amount of global data created is estimated to reach a data volume of 2142 ZB per year ($2142X10^{21}\ Byte/year$) by 2035 [Fig. 1.1][3]. The considerable traffic growth is due to the next generation of wireless networks, such as the emergence of new cloud-computing systems, Internet of Things (IoT), smart sensors, smart homes, worldwide online multimedia streaming services, augmented reality (AR), virtual reality (VR), machine to machine communication (M2M), autonomous vehicles, 5G/6G applications, business, and education digitization. Data centers are expanding rapidly to handle the explosive

internet traffic load with new architectures handling higher traffic volumes relative to the high IP Internet traffic requirements.

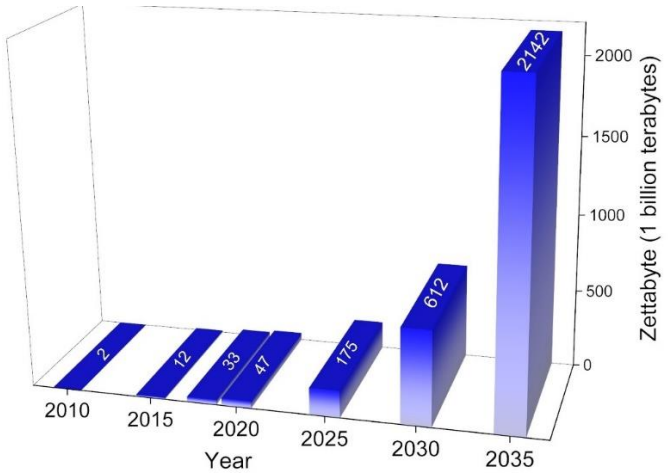


Fig. 1.1. Actual (2010-2019) and forecasted (2020-2035) data creation globally

Datacenters and their networks have become the enablers for several internet-based applications. Nowadays, most of the internet applications, such as online search, online interactive maps, social networks applications, video streaming, the Internet of Things (IoT), and emerging applications, are running in data centers[5]. The number of devices (IoT) connected to IP networks is forecasted by Statista to almost triple from 9.7 billion devices in 2020 to more than 29 billion devices in 2030, as can be seen in Fig. 1.2. by 2023.

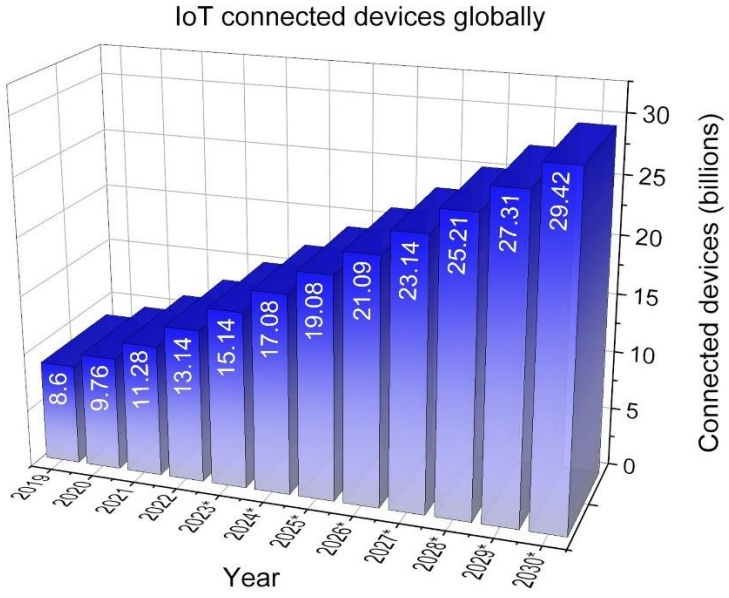


Fig. 1.2. Actual IoT-connected devices globally from (2019-2022) and forecast from (2023 to 2030) [6].

1.2 Optical Communication in Data Centers

1.2.1 Short reach communication

The bandwidth limitations and microwave losses of copper cables and transmission lines are causing a data traffic bottleneck in data centers since they are not as reliable and do not support high speed. Therefore, current data centers widely use low-cost, energy-efficient optical interconnects, which are expected to continue in the future. Nowadays, low-cost, broadband, and energy-efficient optical interconnect based on vertical cavity surface emitting lasers (VCSELs), multimode fiber (MMF), and III-V material-based photodiodes (PDs) are commonly deployed technologies in the high-speed optical short-reach links (<300 m) in data centers. In data centers, short-reach (<300 m) multimode data communications utilize wavelengths of 840–860 nm and also at a new short wavelength division multiplexing (SWDM) band of 850–950 nm that is being proposed for data centers communications[7].

Silicon (Si), due to its high reliability, low-cost mature fabrication process, and volume manufacturability, is the best candidate to produce low-cost, high-speed optical PDs. Using the CMOS fabrication standards, Si PD, silicon-transimpedance amplifiers (TIA), and clock data recovery circuits (CDR) can be monolithically integrated on the same chip. Optical transceiver cost per Gb/s is an essential issue in data centers. Currently, the average cost per Gb/s is in order of tens of dollars, which needs to be decreased to a few dollars [8, 9].

This thesis presents a photon-trapping approach to designing and fabricating an all-silicon photodiode with broad spectral responses from 800 to 1100 nm, >50% EQE and ultrafast time response characteristics of ~30 picoseconds (ps) full width at half maximum (FWHM), and 16 ps deconvolved time response, and a data rate of more than 20 Gb/s. The experimental demonstration of photoabsorption enhancement by more than 20× in silicon effectively exceeds the intrinsic absorption limit of GaAs for a broad wavelength spectrum between 800 to 905 nm

with the potential to exhibit similar enhancement for an even wider range of wavelengths. Intriguingly, simulated performances for ultrathin silicon photodetectors with even thinner absorption regions, such as 30 and 100-nm thin films, exhibit similarly enhanced photosensitivity. Additionally, Si photon-trapping structures help reduce photodetectors' capacitance compared to the planar counterpart, enabling faster response. Finally, the results show that highly efficient future Si-based PDs have the potential to be operational up to 50 Gb/s.

Next, to handle a higher data rate per second in short-reach communication, we utilized the photon-trapping approach in modeling GaAs PT PDs. Optical simulations show that the PT GaAs PIN photodetectors, with only 0.5 μm thin i-layer, can absorb more than 55% of the incident light at λ = 850 nm. On the other hand, as the photon trapping structure filling ratio increases while the junction capacitance decreases and hence the PD bandwidth increases. GaAs photodetectors with 0.5 μm thin i-layer of diameter 25 μm, 8 μm, and 5 μm with 70% surface area covered with nanohole arrays can be operated at a speed of ~70GHz, ~100GHz, and ~135GHz.

1.2.2 Intra- and inter-datacenter communications

Datacenters are envisioned to scale up to meet the high demand for connectivity. Intra- and inter-datacenter communications require optical links for reach gap (500 m–2 km), long-reach (~10 km), and extended reach communications (up to 40 km), which need optical transceivers operating at wavelengths of 1310 nm. At the same time, passive optical networks (PONs), which provide low-cost solutions for the demand for high data rate access to users, require optical transceivers operating at a wavelength of 1550 nm[10]. Data centers support massive traffic coming and going from data centers to end-users. The cloud IP traffic is projected to dominate the global data center traffic ultimately. As a result, the share of global data transferred between data centers to users is projected to increase, while the share of global data transferred within data centers is projected to decrease, as seen in Fig. 1.3.

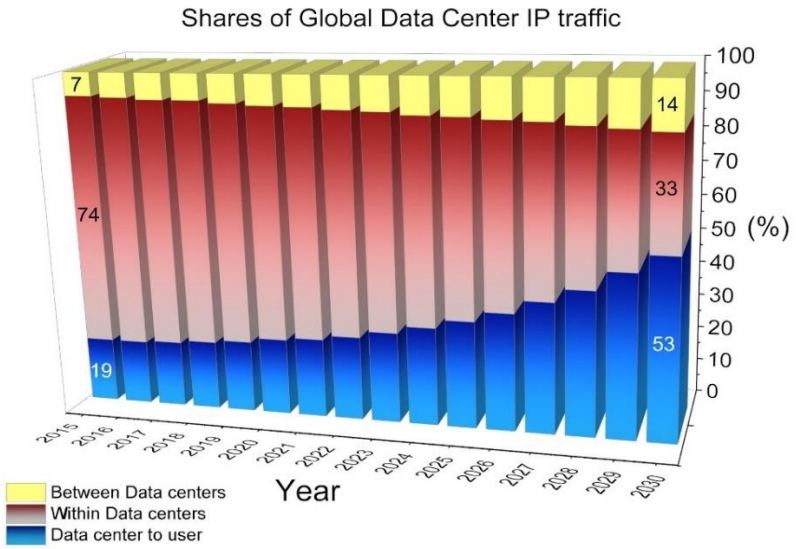


Fig. 1.3. Global share of the data center traffic[11].

The data rate can be increased in such systems by utilizing dense wavelength division multiplexing (DWDM). However, the demand for data traffic is increasing beyond the current capacity of single-mode fiber operating at the C band (1530–1560 nm) and the L band (1560–1620 nm) for DWDM in long-haul communication links. One of the promising solutions to overcome the capacity crunch is to extend existing single-mode fiber bandwidth beyond the L and XL bands. Achievements for fiber amplifiers [12, 13] that can operate in the new band of 1620–1700 nm pave the way to realize data transmission beyond the L band. Furthermore, the new development of hollow-core photonic-bandgap fibers [14, 15] has also provided a new option to extend fiber bandwidth up to 2000 nm with these new optical amplifiers. In addition, applications such as quantum communications [16], eye-safe lidar systems [17], and photonic biosensors [18], require detectors operated at the near-infrared, particularly at 1310 or 1550 nm, taking advantage of the low-loss windows of optical fibers and low scattering of light at those wavelengths in the atmosphere and tissue, respectively.

Ge-on-Si photodetectors provide a possible solution for these high-speed applications, as BiCMOS SiGe technology has already been proven in CMOS foundries [19]. In addition, low-field transport is much faster in Ge than in Si, and high-field transport is similar between both materials.

Thus, using Ge for the i-layer in a pin PD is highly advantageous in improving speed [20]. Although bulk Ge has a very broad absorption spectrum, the direct bandgap of Ge is only 0.8 eV, which results in weak absorption at and beyond 1500 nm.

The optical efficiency of Ge can be significantly enhanced beyond 1500 nm by integrating photon-trapping nanoholes without sacrificing the speed performance. This thesis discusses the demonstration of surface-illuminated Ge-on-Si pin PD with high EQE (>80% at 850 nm, >87% at 1310 nm, and 77% at 1550 nm) for 10 Gb/s operation for short-reach and long-haul optical data communication links. The EQEs of photon trapping (PT) holes PDs have enhanced to >120% at short reach communication 850 nm compared to the control PDs (without holes). In addition, the EQEs of PT PDs enhanced by >400% up to 1700 nm compared to the control PDs, which is promising to realize optical receivers for data transmission beyond the L band, such as U/XL optical band window. The results show that highly efficient future Ge-on-Si-based PDs with only 0.5 µm have the potential to be operational up to 80 Gb/s.

Additionally, this thesis discusses $In_{0.53}Ga_{0.47}As$ photodetector integrated with photon-trapping structures, utilized with a narrow depletion region. The photodetectors with a thin depletion region enable faster photocarriers to drift across the reverse-biased junction, resulting in high bandwidth. The results show that the EQE is enhanced by ~ 3x with PT holes with only 700 nm $In_{0.53}Ga_{0.47}As$ active layer compared to the conventional InGaAs photodetectors. Additionally, bandwidth can be enhanced to meet future THz optical detection and communication demand in the C and L bands and other emerging applications. Based on the PT approach, $In_{0.53}Ga_{0.47}As$ PT PDs have the potential to be operational with >250 Gbps data transmission rate and around 70% detection efficiency.

1.3 Low light level detection

An extremely low number of photons detectors operating at ultra-fast speed and high bandwidth are crucial for optical communications and emerging new technologies and applications.

Emerging technologies require extremely sensitive, low-power, mass-manufacturable photodetectors such as Light Imaging and Ranging (LiDAR), Quantum Communications, computational imaging, biophotonics, medical imaging systems, and other emerging applications. Recently, Avalanche Photodetectors (APDs) and Single Photon Avalanche Photodetectors (SPADs) detectors can meet those requirements. However, their bandwidth, sensitivity, and noise limitation must be overcome[21-23].

The conventional solution for low-light-level detection in many applications uses APDs and SPADs. Avalanche Photodetectors (APDs) are highly sensitive photodetectors (PDs) with an internal gain mechanism generated by the impact ionization of their carriers. This mechanism provides higher signal-to-noise ratios and higher optical sensitivities. The gain depends on the internal electric field and the applied reverse bias. In APDs, the output photocurrent is linearly proportional to the input optical power when APDs work at lower than their breakdown voltage. While Single Photon Avalanche Photodetectors (SPADs) are also designed as avalanche PD that operate at higher reverse bias voltage (above the breakdown voltage), and this operation mode is known as Geiger mode operation.

Si APDs and SPADs with photon-trapping (PT) holes can be monolithically integrated with CMOS/BiCMOS application-specific integrated circuits (ASICs) and could offer a promising solution for waveguide photodetectors required for Photonic Integrated Circuits (PICs). Such APDs and SPADs are designed with the implementation of proper doping profiles for high amplification, thin Si layer for high speed (short transient-time), low dark current, high gain, and optimized design of micro/nanoholes for highly sensitive and ultrafast optical receivers/sensors.

1.4 Computational imaging

Optical spectrometers are widely used scientific equipment with many applications involving material characterization, chemical analysis, disease diagnostics, surveillance, etc. Emerging applications in biomedical and communication fields have boosted research in the miniaturization

of spectrometers[24]. Recently, reconstruction-based spectrometers have gained popularity for their compact size, easy maneuverability, and versatile utility[25]. These devices exploit the superior computational capabilities of recent computers to reconstruct hyperspectral images using detectors with distinct responsivity to different wavelengths. In this thesis, we present CMOS-compatible reconstruction-based on-chip spectrometer pixels capable of spectrally resolving the visible spectrum with 1 nm spectral resolution maintaining high accuracy (>95 %) and low footprint (8 μm × 8 μm), all without the use of any additional filters. To achieve distinct responsivity, we utilize optimized photon-trapping nanostructures photodiodes with different dimensions and profiles that modify light coupling at different wavelengths, which can reflect a unique response footprint. This also reduces the spectrometer pixel footprint (comparable to conventional camera pixels), thus improving spatial resolution. This miniaturized spectrometer can be utilized as spectroscopy-on-chip for real-time in-situ biomedical applications such as Fluorescence Lifetime Imaging Microscopy (FLIM), pulse oximetry, disease diagnostics, and surgical guidance.

1.5 CMOS image sensors

The interest in complementary metal-oxide-semiconductor (CMOS) image sensors is increasing due to the growing demand for mobile imaging, digital cameras, surveillance, monitoring, and biometrics. Image sensors have been adopted in a significant number of products [26-28] and have a multitude of applications. One such application is night-time surveillance and monitoring, which demands high sensitivity and improved resolution in the near-infrared wavelength spectrum. As a result, several manufacturing companies compete to bring a higher resolution imager to the market. This constant drive to increase the pixel density has resulted in a 2.5-fold reduction in the pixel pitch from 2.2 μm (Micron-2006) to even 0.8 μm (Sony-2019) over the past decade [29]. The trade-off for such improvement came in the form of a loss in optical sensitivity due to the reduction of the absorption area. This can be resolved by using a thicker absorbing

layer. However, the thicker absorber layer reduces the speed of operation, thus affecting the bandwidth of the imager. To mitigate this trade-off between resolution-efficiency-speed, we investigate the use of microholes to enhance the optical efficiency of the imagers in the near-infrared wavelength region [30]. As a result, we observe an enhanced optical efficiency in the near-infrared spectrum compared to the same structure without the microholes. CMOS image sensors generally have pixel sizes of 2 μm × 2 μm or even smaller dimensions [31]. CMOS sensors having such small pixel sizes contribute to a significant challenge in suppressing the parasitic charge exchanges between neighboring pixels (crosstalk). Although the insertion of microhole arrays increases the crosstalk between pixels, it was reduced using deep trench isolation (DTI).

1.6 Surface passivation of silicon photonic devices integrated with nanostructures.

A high-speed and high-efficiency silicon photodiode (PD) is demonstrated by enabling photon-trapping nanoholes. While attractive for light manipulation, these high surface-to-volume-ratio nanostructures, which are created by top-down dry etching processes, can also bring other challenges, such as creating silicon surface damage and crystalline defects. To reduce the dark current level and minimize surface recombination for better detection, successful passivation is a vital step to achieving the ultimate performance of the silicon PD based on photon-trapping structures. In this thesis, multiple surface passivation schemes, including HF treatment, PECVD, thermal oxidation, and LIEE, are utilized to suppress the dark current level of the photon-trapping micro/nanohole-enabled Si *pin* PDs and ultimately achieve desirable external quantum efficiency (EQE). More than 3 or 4 orders of magnitude of dark current reduction have been observed by all the passivation techniques. Unlike most PV applications, our Si *pin* PDs have highly doped n^+ and p^+ layers for high-speed operation. Thus, the quality of each passivation scheme is assessed based on the EQE of the PDs to reflect the overall effect on the PDs. The results in this

paper are CMOS compatible and can also be applied to many other photonic device applications[32, 33].

1.7 Dissertation Outline

In this thesis, we present photon-trapping nanostructure designs in various photodetectors that utilize different semiconductors to cover a broad optical spectrum [Fig. 1.4] for optical communication, imaging, and sensing applications.

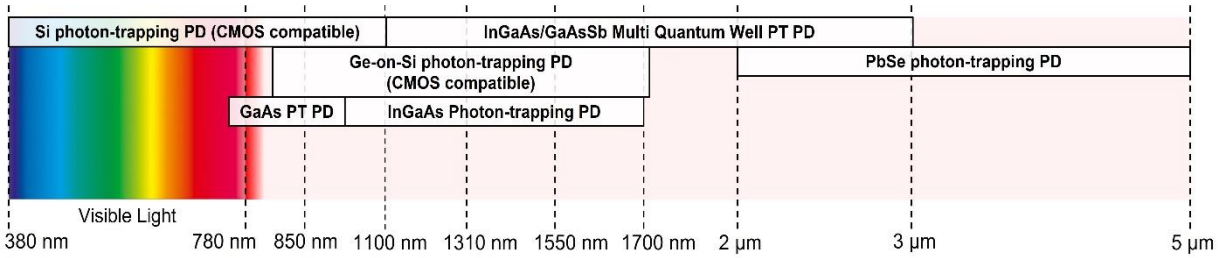


Fig. 1.4. Operational spectral range of devices and photon-trapping (PT) nano designs incorporated in various semiconductors PDs.

This dissertation is structured as follows: Chapter 1 introduces the motivation, this work contribution, and a summary of the accomplishments [Fig. 1.5]. Chapter 2 presents an overview of enhancing photodetectors' efficiencies and photon-trapping theory. Chapter 3 presents the passivation techniques of silicon photonics devices with high surface-to-volume ratio nanostructures that are CMOS compatible. Chapter 4 introduces the implementation of photon-trapping nanostructures in Si photodetectors, and designs optimization enabled ultra-fast and high-efficiency Si CMOS-compatible PDs. Chapter 5 presents low-cost Si photovoltaic integrated with surface light-trapping nanostructures for indoor and outdoor self-standing IoT sensors. Chapter 6 presents highly sensitive Si avalanche PD (APD) and single-photon avalanche (SPAD) enabled by photon-trapping designs. Engineering optical depth and gain are discussed subsequently. Finally, computational imaging and the unique response of the fabricated Si photon-trapping APD are presented. Chapter 7 presents achieving higher photoabsorption than group III-V semiconductors in thin Si using photon-trapping nanostructures. Next, we optimized

photon-trapping designs to enhance optical efficiency in Si and Ge-on Si CMOS image sensors as single nano-/micro holes per pixel. Expanding the optical detections to longer wavelengths, Chapter 9 presents ultra-fast, and high-efficiency Germanium on Silicon (Ge-on-Si) integrated with optimized photon-trapping designs. Next, in Chapter 10, thin III-V (GaAs and InGaAs) semiconductors are modeled, discussed with photon-trapping designs, and utilized for ultra-high-speed operation. Additionally, we exploit multi-quantum-wells (MQWs) phenomena to engineer a detection ability to cover 1-3 µm wavelength and introduce photon-trapping designs to enhance their detection and operational speed efficiencies in Chapter 11. Subsequently, we studied photon-trapping designs on mid- and long-wavelength infrared (IR) detectors and exploited the PT approach to model PbSe and HgCdTe for high-performance IR detection in Chapter 12. Finally, Chapter 13 presents the CMOS integration of Si PT PDs, new photon-trapping designs, future opportunities, and emerging applications.

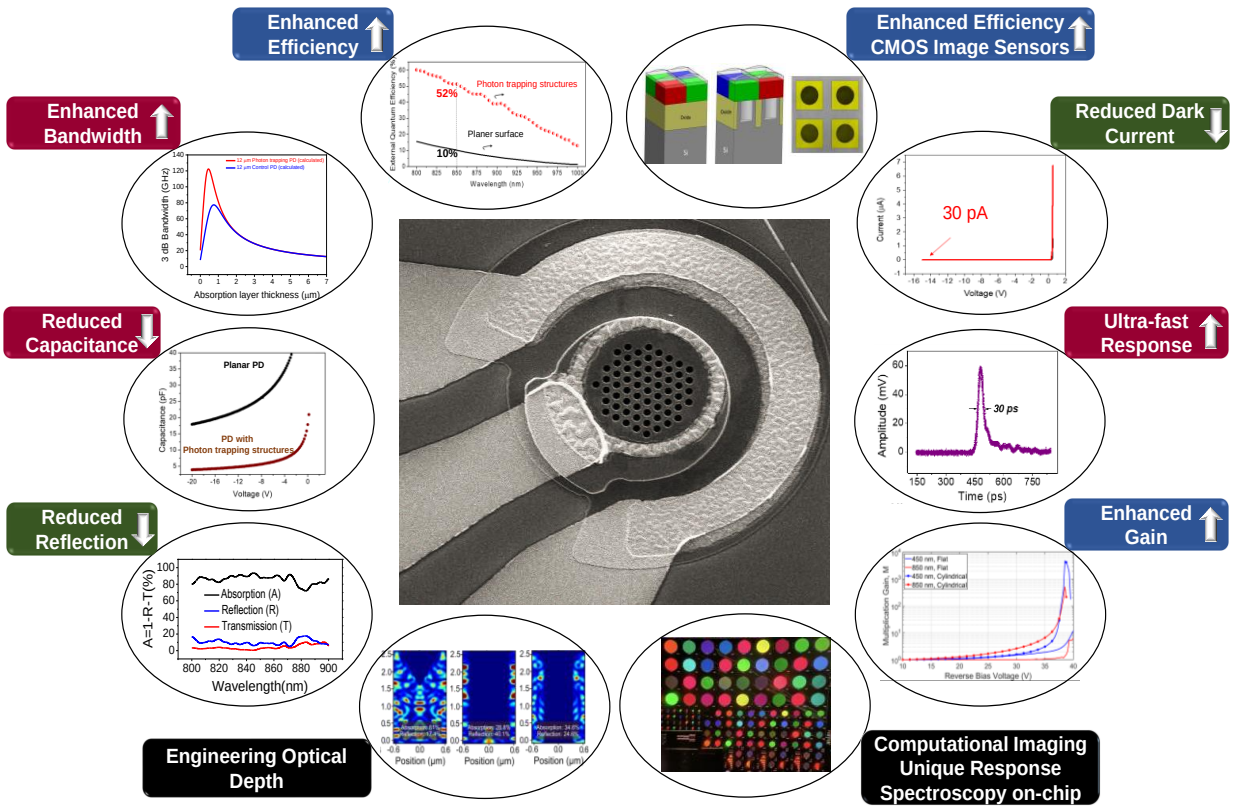


Fig. 1.5. Photon-trapping designs in PDs enabled the achievement of numerous objectives for highly-efficient photodetectors that could be utilized in optical communication, imaging, and sensing applications.

References

[1] H. Cansizoglu *et al.*, "A new paradigm in high-speed and high-efficiency silicon photodiodes for communication—Part II: device and VLSI integration challenges for low-dimensional structures," *IEEE Transactions on Electron Devices,* vol. 65, no. 2, pp. 382-391, 2017.

[2] O. Vermesan and P. Friess, *Internet of things: converging technologies for smart environments and integrated ecosystems*. River publishers, 2013.

[3] Armstrong, "Global Data Creation is About to Explode [Digital image]," ed, 2019, pp. https://www.statista.com/chart/17727/global-data-creation-forecasts/.

[4] C. Kachris, K. Kanonakis, and I. Tomkos, "Optical interconnection networks in data centers: recent trends and future challenges," *IEEE Communications Magazine,* vol. 51, no. 9, pp. 39-45, 2013.

[5] Cisco, "Cisco Annual Internet Report (2018–2023) White Paper."

[6] T. Insights, "Number of Internet of Things (IoT) connected devices worldwide from 2019 to 2021, with forecasts from 2022 to 2030 (in billions), In Statista. Retrieved January 15, 2023," ed. Transforma Insights, July, 2022, p. .

[7] J. A. Tatum *et al.*, "VCSEL-based interconnects for current and future data centers," *Journal of Lightwave Technology,* vol. 33, no. 4, pp. 727-732, 2015.

[8] R. Kirchain and L. Kimerling, "A roadmap for nanophotonics," *Nature Photonics,* vol. 1, no. 6, pp. 303-305, 2007.

[9] S. Ghandiparsi *et al.*, "High-speed high-efficiency photon-trapping broadband silicon PIN photodiodes for short-reach optical interconnects in data centers," *Journal of Lightwave Technology,* vol. 37, no. 23, pp. 5748-5755, 2019.

[10] V. Houtsma, D. van Veen, and E. Harstead, "Recent progress on standardization of next-generation 25, 50, and 100G EPON," *Journal of Lightwave Technology,* vol. 35, no. 6, pp. 1228-1234, 2016.

[11] H. J. Walnum and A. S. Andrae, "The internet: Explaining ICT service demand in light of cloud computing technologies," in *Rethinking Climate and Energy Policies*: Springer, 2016, pp. 227-241.

[12] S. V. Firstov *et al.*, "A 23-dB bismuth-doped optical fiber amplifier for a 1700-nm band," *Scientific reports,* vol. 6, no. 1, pp. 1-6, 2016.

[13] Z. Li *et al.*, "Extreme short wavelength operation (1.65–1.7 μm) of silica-based thulium-doped fiber amplifier," in *Optical Fiber Communication Conference*, 2015: Optica Publishing Group, p. Tu2C. 1.

[14] H. Zhang *et al.*, "81 Gb/s WDM transmission at 2μm over 1.15 km of low-loss hollow core photonic bandgap fiber," in *2014 The European Conference on Optical Communication (ECOC)*, 2014: IEEE, pp. 1-3.

[15] T. Morioka, Y. Awaji, R. Ryf, P. Winzer, D. Richardson, and F. Poletti, "Enhancing optical communications with brand new fibers," *IEEE Communications Magazine,* vol. 50, no. 2, pp. s31-s42, 2012.

[16] P. Jouguet, S. Kunz-Jacques, A. Leverrier, P. Grangier, and E. Diamanti, "Experimental demonstration of long-distance continuous-variable quantum key distribution," *Nature photonics,* vol. 7, no. 5, pp. 378-381, 2013.

[17] R. Sabatini, M. A. Richardson, H. Jia, and D. Zammit-Mangion, "Airborne laser systems for atmospheric sounding in the near infrared," in *Laser Sources and Applications*, 2012, vol. 8433: SPIE, pp. 288-327.
[18] L. A. Sordillo, Y. Pu, S. Pratavieira, Y. Budansky, and R. R. Alfano, "Deep optical imaging of tissue using the second and third near-infrared spectral windows," *Journal of biomedical optics,* vol. 19, no. 5, p. 056004, 2014.
[19] J. S. Dunn *et al.*, "Foundation of RF CMOS and SiGe BiCMOS technologies," *IBM Journal of Research and Development,* vol. 47, no. 2.3, pp. 101-138, 2003.
[20] S. M. Sze, Y. Li, and K. K. Ng, *Physics of semiconductor devices*. John wiley & sons, 2021.
[21] R. H. Hadfield, "Single-photon detectors for optical quantum information applications," *Nature photonics,* vol. 3, no. 12, pp. 696-705, 2009.
[22] R. E. Warburton *et al.*, "Ge-on-Si single-photon avalanche diode detectors: design, modeling, fabrication, and characterization at wavelengths 1310 and 1550 nm," *IEEE Transactions on Electron Devices,* vol. 60, no. 11, pp. 3807-3813, 2013.
[23] P. Vines *et al.*, "High performance planar germanium-on-silicon single-photon avalanche diode detectors," *Nature communications,* vol. 10, no. 1, pp. 1-9, 2019.
[24] Z. Yang, T. Albrow-Owen, W. Cai, and T. Hasan, "Miniaturization of optical spectrometers," *Science,* vol. 371, no. 6528, p. eabe0722, 2021.
[25] J. Malinen *et al.*, "Advances in miniature spectrometer and sensor development," in *Next-Generation Spectroscopic Technologies VII*, 2014, vol. 9101: SPIE, pp. 83-97.
[26] C.-F. Han, J.-M. Chiou, and J.-F. Lin, "Deep trench isolation and inverted pyramid array structures used to enhance optical efficiency of photodiode in CMOS image sensor via simulations," *Sensors,* vol. 20, no. 11, p. 3062, 2020.
[27] I. Oshiyama *et al.*, "Near-infrared sensitivity enhancement of a back-illuminated complementary metal oxide semiconductor image sensor with a pyramid surface for diffraction structure," in *2017 IEEE International Electron Devices Meeting (IEDM)*, 2017: IEEE, pp. 16.4. 1-16.4. 4.
[28] S. Yokogawa *et al.*, "IR sensitivity enhancement of CMOS Image Sensor with diffractive light trapping pixels," *Scientific reports,* vol. 7, no. 1, pp. 1-9, 2017.
[29] R. Fontaine, "The state-of-the-art of mainstream CMOS image sensors," in *Proceedings of the International Image Sensors Workshop*, 2015, pp. 6-12.
[30] Y. Gao *et al.*, "Photon-trapping microstructures enable high-speed high-efficiency silicon photodiodes," *Nature Photonics,* vol. 11, no. 5, pp. 301-308, 2017.
[31] J. Ahn *et al.*, "Advanced image sensor technology for pixel scaling down toward 1.0 µm," in *2008 IEEE International Electron Devices Meeting*, 2008: IEEE, pp. 1-4.
[32] A. S. Mayet *et al.*, "Surface passivation of silicon photonic devices with high surface-to-volume-ratio nanostructures," *JOSA B,* vol. 35, no. 5, pp. 1059-1065, 2018.
[33] A. S. Mayet *et al.*, "Inhibiting device degradation induced by surface damages during top-down fabrication of semiconductor devices with micro/nano-scale pillars and holes," in *Low-Dimensional Materials and Devices 2016*, 2016, vol. 9924: SPIE, pp. 36-42.

Chapter 2 Research prospective and theory

Semiconductor photodetectors consider the technology of many choices for applications requiring durability, high sensitivity, fast response times, and low cost. Available photodetectors offer high detection efficiency at wavelengths from the UV/visible spectrum to the near-infrared (NIR). The standard photodetectors are the PIN diode, metal semiconductor metal (MSM), also considered as a type of PIN detector, and avalanche photodiode. Normally, the photodetector is characterized by three core performance metrics: (i) responsivity (how effectively electrons and holes are generated), (ii) dark current density, and (iii) response time (how fast the generated carriers transport). However, once a particular semiconductor material is chosen for a particular cut-off frequency (for instance, silicon), the carrier transport properties remain unchanged—mostly limited by the carrier mobility of the semiconductor. Therefore, one can only explore novel techniques for improving the electron–hole (e–h) pair generation and collection efficiency. The most common device structure in high-speed PDs involves PIN diode (i.e., intrinsic layer, or i-layer, sandwiched between highly doped p and n layers serving as contacts). The photoconductive mode of PIN diodes, which requires a reverse bias of moderate magnitude, is the common configuration in high-speed PDs. The thickness of the i-layer defines the transit time that is required for carriers to reach the contacts. For ultrafast operations, the i-layer must be thin enough to ensure high bandwidth. However, a thin i-layer cannot efficiently absorb the incoming photons, leading to a trade-off between efficiency and speed in the conventional PIN photodetectors.

2.1 The absorption coefficient of selected semiconductors

The optical absorption coefficient (α) defines a semiconductor's ability to absorb the incident light, as seen in Fig. 2.1[1]. These values correspond to the light penetration depth at which all the incident photons get absorbed. Therefore, high optical absorption coefficient semiconductors with

low reflection and low transmission are desired for optical detection applications. However, the absorption coefficient is wavelength dependent; therefore, the absorption values drop sharply closer to their bandgap's edges. Therefore, thicker semiconductors are needed to completely absorb all incident photons, leading to a larger transient time and slower photodetectors.

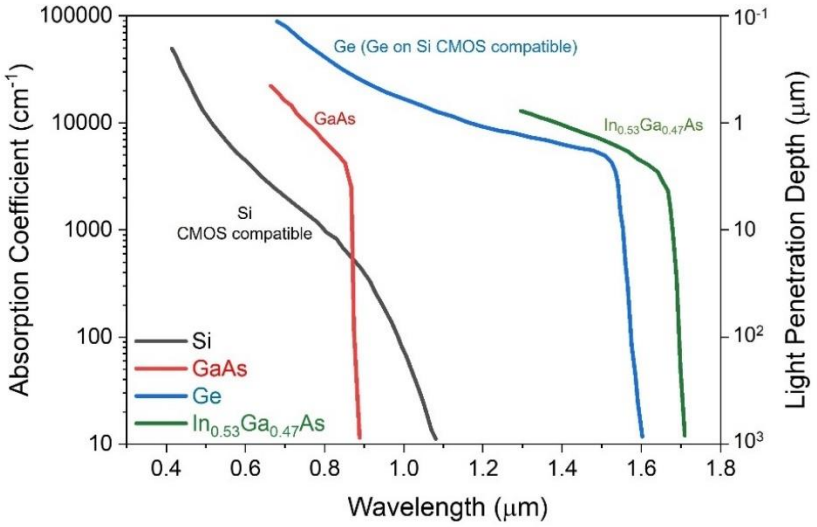


Fig. 2.1. Absorption coefficients (α) of different semiconductors.

Besides the optical absorption coefficients, electrical properties are considered while designing photodetectors. Different semiconductors are studied and developed for detection applications according to their unique physical, optical and electrical properties. Table 2.1 compare some of the bulk properties of Si, Ge, and III-V semiconductors [2, 3]. A semiconductor's bandgap specifies the material's cut-off frequency response, which utilizes them to operate in a specific optical spectrum. Additionally, as seen in table 2.1, Ge and III-V semiconductors have significantly higher electron mobility than Si, enabling them for ultra-fast operation. However, Si and Ge are CMOS-compatible semiconductors, while III-V semiconductors suffer from cost and CMOS compatibility issues in the Si photonics platform.

Property	Si	Ge	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	InSb
Electron Mobility cm^2/(V.s)	1600	3900	9200	13800	40000	77000
Hole Mobility cm^2/(V.s)	430	1900	400	400	500	850
Bandgap (eV)	1.12	0.66	1.424	0.74	0.36	0.17
Dielectric Constant	11.8	16	12.4	13.9	14.8	17.7

Table 2.1. Bulk semiconductors properties of Si, Ge, and III-V.

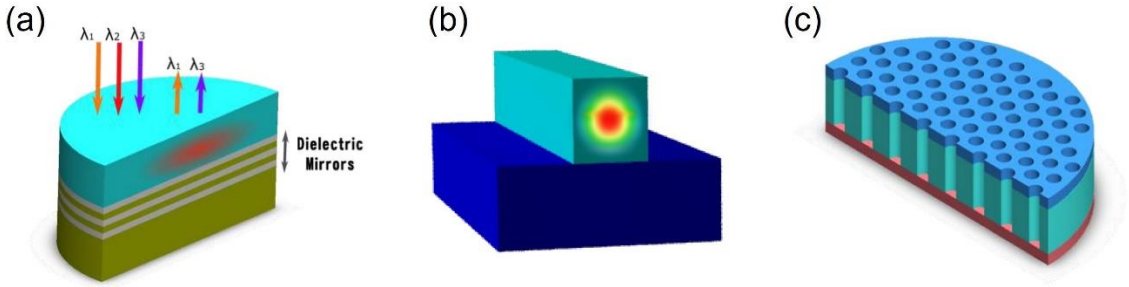
2.2 Motivation

2.2.1 Si and Ge-on-Si CMOS compatible ultra-fast and high-efficiency photodetectors.

III-V semiconductors are the dominant PDs in high-speed optical communication due to their direct band gap and high carrier velocities' physical characteristics. However, III-V photodetectors cannot be monolithically integrated into electronic CMOS circuits. They would incur additional costs for wafer bonding, packaging, yield, thermal management, and III-V growth high-cost. For monolithically CMOS integration and cost-effective purposes, Si and Ge-on-Si could replace III-V photodetectors on chips for optical communication, imaging, and sensing applications. There is a longstanding belief that most common materials used in semiconductor manufacturing, such as Si, cannot be employed in designing a surface-illuminated PD for ultra-fast communication networks due to their low absorption coefficients at near-infrared wavelengths such as 850 nm—a wavelength commonly used for short-reach optical communication. Several absorption enhancement methods without using a thick i-layer have been applied to surface-illuminated Si PDs for high-speed operations. Prior work in high-speed Si PDs mainly involved surface-illuminated resonant cavity enhanced (RCE) PDs and edge-illuminated waveguide PDs, as depicted in Fig. 2.2 (a) and (b), respectively. The optical path is prolonged due to multiple passes of light supported by the cavity. Hence RCE PD exhibits a high external quantum efficiency (EQE); however, the useful optical bandwidth is narrow.

Additionally, any thermal shift of the laser wavelength can result in a decreased sensitivity at the optical receiver, which limits their practical implementation. Waveguide Si PDs [4, 5] can have high EQE and high-speed operation. Long absorption lengths along the waveguide enable high EQE. At the same time, a thin intrinsic layer allows short e–h transit time since the optical wave propagation direction is perpendicular to the electric field. However, waveguide PDs require

precision packaging for efficient coupling of single-mode optical fiber to the optical waveguide, resulting in high packaging costs [6].



Resonant Cavity Enhanced PD	Waveguide PD	Photon-trapping holes integrated PD
Surface-illuminated	Edge-coupled	Surface-illuminated
Narrow optical bandwidth	Broadband	Broadband
Requires careful design/ fabrication of dielectric mirrors	Tight fiber alignment tolerance	CMOS compatible

Fig. 2.2. (a) Resonant cavity-enhanced PD with high bandwidth and wavelength-dependent high quantum efficiency. (b) Waveguide PD confines light in a thin and long absorption region, and the electrical signal is collected in a transmission line as light propagates forward. High-precision alignment of fiber contributes to high packaging costs in such a device. (c) Holes integrated into a PD fabricated via CMOS compatible process for low reflection, broadband absorption, high efficiency, and high bandwidth.

A technology that enables a surface-illuminated PD with an ultrathin absorption layer to absorb most of the incident photons is highly desirable to address the trade-off between efficiency and bandwidth. Unfortunately, there has been a lack of practical high-speed Si PDs until the recent demonstration of a CMOS-compatible, high-efficiency, and high-speed Si PD with integrated photon-trapping nanoholes. Figure 2.2 (c) shows incoming photon beams that are vertically oriented and have a direction of propagation parallel to the axis of the holes; they interact with the holes to produce both vertically and laterally propagating modes, which then allow them to interact with Si for a long time before being effectively absorbed. This method can overcome the poor Si absorption coefficient at datacom wavelengths between 800 and 1100 nm.

As can be seen in Fig. 2.3., the solid lines belong to the Si PDs with holes providing a 50% reduction in junction capacitance, and the dashed lines belong to Si PDs without holes. For example, >50 Gb/s data transmission is attainable with a Si PD with 1 μm i-layer and holes that

reduce the junction capacitance by half. On the other hand, large PDs such as 100 µm in diameter can be designed for 10 Gb/s data transmission lines. Figure 2.3 shows that high-efficiency Si PDs can be designed with nanoholes to reach speeds similar to/or greater than GaAs PDs [7]. The behavior of responsivity of Si PDs vs. i-layer thickness is also strictly dependent on the geometry. The dashed red line shows the theoretical prediction for Si PDs without holes (control) in the case of perfect anti-reflection (AR) coating. Si with nanoholes was anticipated to have 0.5 A/W responsivity (~2 µm i-layer) while supporting sufficient BW for a 25 Gb/s data transmission rate. However, the responsivity of Si PD without holes can only reach 0.1 A/W with 2 µm i-layer and perfect AR coating. Si PDs without holes require a much thicker absorption layer, which reduces BW to ~1 GHz to get similar efficiency of Si PD with nanoholes.

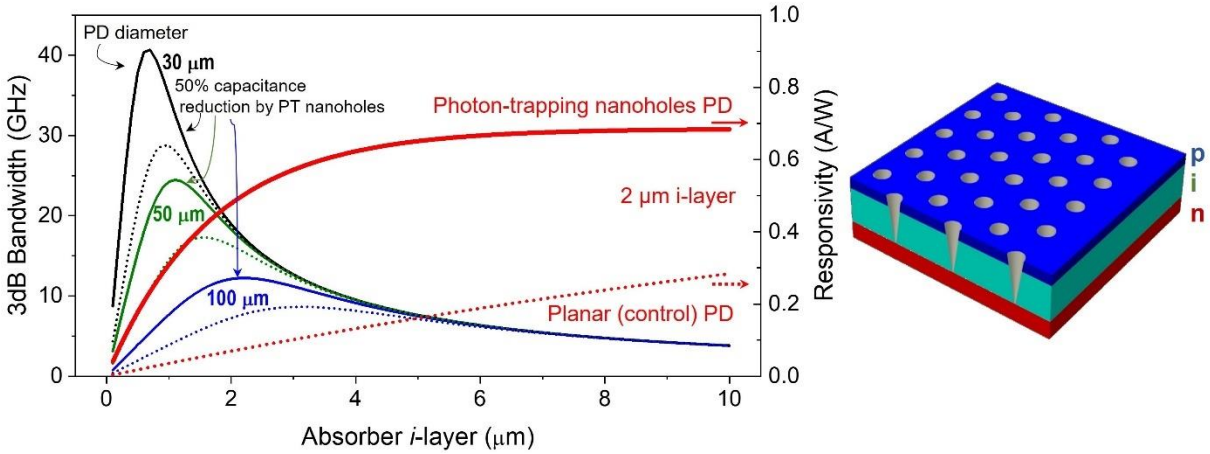


Fig. 2.3. 3dB BW and responsivity estimated for different intrinsic layer thicknesses of Si pin circular photodiode with 30, 50, and 100 µm in diameter for 850 nm wavelength. The solid and dashed lines represent the Si photon-trapping (PT) nanoholes PDs and without holes (control) in the case of 50% capacitance reduction, respectively.

2.2.2 III-V and multi-quantum-wells (MQWs) ultra-fast and high-efficiency photodetectors.

Single-crystalline III-V compound semiconductors, such as GaAs, InGaAs, and MQWs PDs, offer direct and tunable energy bandgap, higher electron mobility, and higher absorption coefficient than Si [8]. However, a thinner i-layer in PIN PDs can reduce the transit time and increase the photoresponse, which leads to a larger 3 dB bandwidth, resulting in an absorption-bandwidth

trade-off that limits the device's performance. Therefore, various designs and approaches were developed to address such limitations.

For instance, PDs integrated with nanowires have been studied extensively during the evolution of nanofabrication techniques [9]. However, one of the great challenges of nanowire devices is the ohmic contact formation due to the characteristics of the metal–nanowire interface [10]. Additionally, plasmonic nanostructures can be a promising alternative technology to achieve light trapping in thin-film PDs [11, 12]. Plasmonic nanostructures enhance light trapping in different mechanisms; metallic nanoparticles, which act as subwavelength scattering centers, can couple the incident light by folding it into the semiconductor [Fig. 2.4 (a)]. In addition, nanoparticles embedded in the film, acting like a sub-wavelength nanoantenna, can cause coherent electromagnetic energy transport along the absorbing material employing strong near-field coupling of plasmon oscillations between nanoparticles [Fig. 2.3(b)][13, 14].

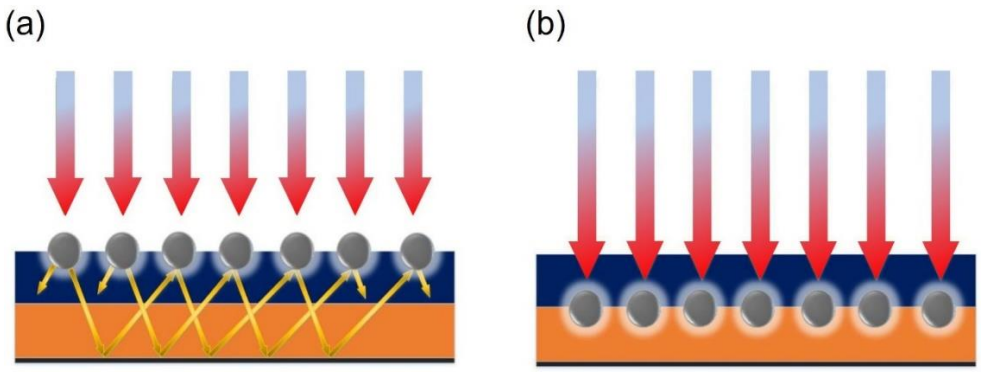


Fig. 2.4. (a) Light trapping by scattering from metal nanoparticles at the surface. (b) Light trapping by exciting plasmon polaritons embedded at the interface of semiconductors.

Our photon-trapping nanostructures approach can address the absorption-bandwidth trade-off by increasing photon-matter interaction, enhancing absorption efficiency, and maintaining ultra-fast operation [7]. Photon-trapping III-V photodetectors provide unprecedented performance enhancements, which suggests the commercialization of photon-trapping structure photodetectors may be profitable. One of the objectives of this thesis is to push the limits of III-V photodetectors (GaAs, InGaAs, and MQWs PDs) and to determine to what degree the performance of currently available commercial photodetectors can be surpassed.

PDs with photon-trapping nanostructures can inhibit broadband reflection and improve broadband absorption by photon manipulation and slow light. Additionally, an ultra-thin absorbing layer (such as 0.5 μm) [Fig. 2.5] can enhance the bandwidth to meet future THz optical detection and communication demand in the C and L bands and other emerging applications with >250 Gbps data transmission rate and >70% detection efficiency.

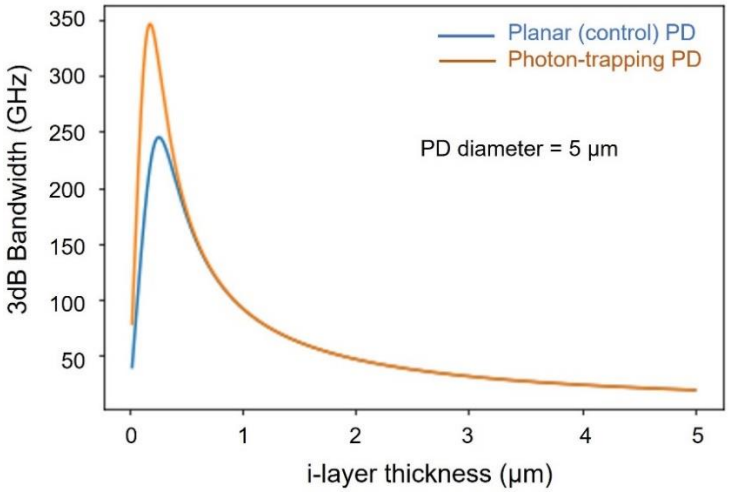


Fig. 2.5. Estimated 3dB operation bandwidth for InGaAs PDs with different absorption layer thicknesses for the 5 μm diameter devices. A photon-trapping PD is assumed to achieve over 300 GHz 3dB operation bandwidth, requiring a thickness of 0.5 μm, with a PD diameter of 5 μm.

2.2.3 Low light level detections, computational imaging, and spectroscopy on chip (SoC)

Currently, exciting new applications are developing in optical sensing communities that require detecting an extremely low number of photons at visible and near-infrared (NIR) spectral regions, potentially reaching the level of single photons. Fast and ultra-sensitive detectors are particularly needed for applications that require precise measurement of sub-nanosecond lifetimes of very weak optical signals [15, 16]. Free space optical communication (FSO), such as light detection and ranging systems (LIDAR), have been highly developed in the recent past due to the interest in implementing these systems in autonomous cars. This application needs to be able to sense and quickly respond to objects at distances over 100 m to avoid car collisions. Atmospheric transmission loss, environmental noise, fog, air turbulence, and the restrictions on maximum laser

power result in only a small number of photons reaching the LIDAR receiver [17]. Big data and information interchanging increase security challenges, especially insecure data transmission; quantum communication are projected to be the most secure technology for data transmission. Since any tapping into the transmission line will destroy the quantum states of entangled photons, immediate detection of a tapped line will be possible in a quantum communication system (QCS). Single-photon detectors are the main component in the receiver of a QCS. In addition, biomedical imaging utilizes the typical fluorescence decay times of biological fluorophores that fall between several nanoseconds and a few hundred of picoseconds [18]. In biomedical applications, detecting intensity, spectral information, and fluorescence lifetime allows us to discriminate between fluorophores with overlapping spectra and to study microenvironments of fluorescent molecules, including local pH, temperature, and ion concentration[19-21]. Miniaturizing image sensors/spectrometers will enable non-invasive diagnostics and pharmaceutical analysis and confer advantages during surgical procedures. Large spectrometers offer a resolution of ~1 nm with wide spectral ranges.

Nevertheless, the fast-growing demand for spectral analysis requires considerably reduced physical dimensions down to sub-millimeter scale footprints to offer abilities for in-situ analysis and develop lab-on-a-chip systems. With the recent surge in computational power and the reduction in microprocessors' size and cost, we can reconstruct spectral images by developing a unique response photodetector. Efficient algorithms and training data can be utilized to develop the unique response PDs to build imaging and sensing system-on-chip (SoC). Our designed and optimized photon-trapping ultra-fast Si avalanche PD (APD) and single photon PD (SPAD) in an array exhibits significantly enhanced wide-spectral sensitivity, enhanced speed, reduced voltage operation, enhanced gain and high dynamic range with improved signal-to-noise ratios (SNR). Photon-trapping nanostructures PDs with various designs presents unique optical response that could be developed and enable artificial intelligence AI-assisted computational imaging on chip (CMOS compatible) for longer wavelength detection applications at 1310 nm, 1550 nm, and

beyond. Photon-trapping designs are implemented in Ge, InGaAs, and MQW PDs and validate their capability to be applied in various thin materials (with different cut-off frequencies) to cover wider optical spectra.

2.3 Photon Trapping Theory

Various signs of progress were developed to enhance optical efficiencies in photodetectors and photovoltaics, such as nanowires [9, 22], plasmonics [23], resonant cavities [24], and photon-trapping nanostructures. The concept of photon-trapping (nanophotonics) strategies was initially inspired by promising aspects of achieving high quantum efficiency in solar cells. From ray optics perspective, light-trapping exploits the effect of total internal reflection inside the semiconductor material and the surrounding medium. The light propagation direction gets randomized inside the material by roughening the semiconductor-air interface. The total internal reflection effect results in a longer propagation distance inside the material and consequently leads to a substantial absorption enhancement [25]. Considering a high-index material such as silicon with n = 3.5 and Germanium n = 4, with a high reflectivity mirror at the bottom (SiO_2 = 1.45) and air at the top, such film supports guided optical modes. The optical absorption of the film (active layer) is weak, as these guided modes typically have a propagation distance along with the film's length being greater than its thickness. Hence a large portion of the incident light reflects or leaks through the thin film without getting absorbed. Light-trapping is achieved by coupling the incident planer waves into a thin film-guided mode with a grating structure with Periodicity L comparable to the incident light wavelength, as seen in Fig. 2.6 (b). The optical absorption spectrum contains multiple peaks corresponding to a guided resonance. As can be seen in Fig. 2.7 (a), each resonance in the frequency range can couple to channels in the parallel wave vector that are equally spaced by 2/L. $|K_{II}|$[25].

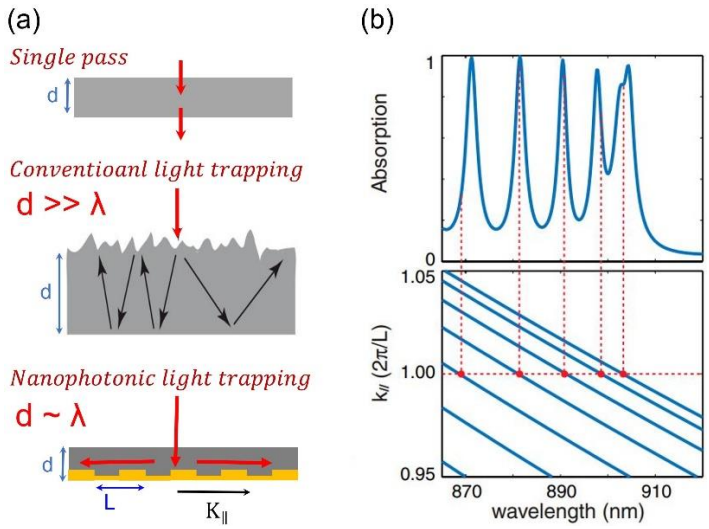


Fig. 2.6. (a) single pass in thin film vs. conventional light-trapping approach (random roughening) and nanophononics light-trapping approach. (b) Resonance in nanophononics light trapping approach [25]. (L is pattern periodicity)

Therefore, for maximizing the absorption, as can be depicted in Fig. 2.7 (b)(red region), the periodicity should be designed to be slightly smaller than the wavelength range of interest (L/λ). Figure 2.7 (c) presents the optical absorption enhancement using the nanophononics (photon-trapping) approach vs. the conventional light-trapping approach. The concept of photon-trapping is utilized to design thinner, high-efficiency, and ultra-fast Si, Ge, III-V, and MQW photodetectors for optical communication, imaging, and sensing applications. Photon-trapping concept is further discussed in sections 4.1, 7.4.6, and 7.4.7.

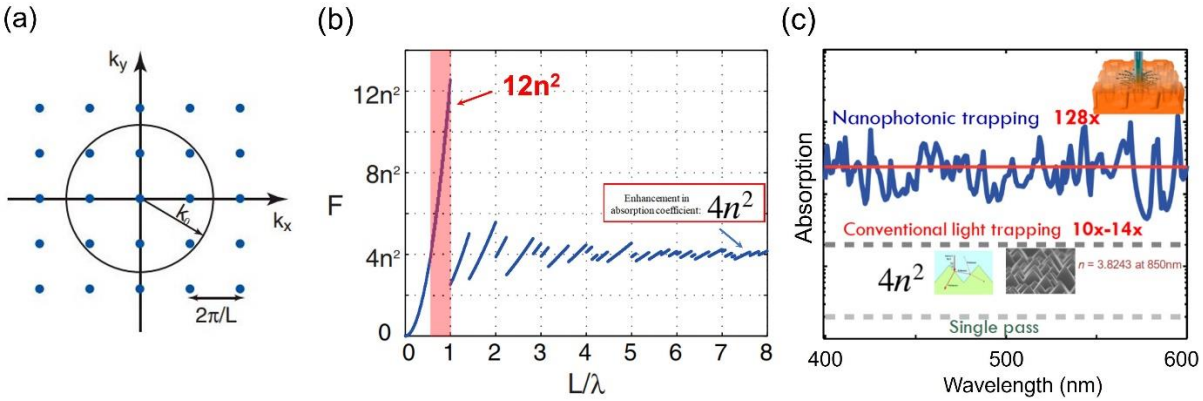


Fig. 2.7. (a) Resonance coupling to channels equally spaced by (2π/L). (b) Resonance mode coupled onto the guiding mode and high optical absorption enhancement at L/λ <1. (c) The nanophononics trapping approach achieves high optical absorption enhancement [25].

References

[1] Z. Huang, *Germanium photodetector integrated with silicon-based optical receivers*. The University of Texas at Austin, 2006.

[2] S. Adachi, *Physical properties of III-V semiconductor compounds*. John Wiley & Sons, 1992.

[3] A. Abedin, "Germanium layer transfer and device fabrication for monolithic 3D integration," KTH Royal Institute of Technology, 2021.

[4] J. J. Ackert, A. S. Karar, J. C. Cartledge, P. E. Jessop, and A. P. Knights, "Monolithic silicon waveguide photodiode utilizing surface-state absorption and operating at 10 Gb/s," *Optics express,* vol. 22, no. 9, pp. 10710-10715, 2014.

[5] L. Alloatti and R. J. Ram, "Resonance-enhanced waveguide-coupled silicon-germanium detector," *Applied Physics Letters,* vol. 108, no. 7, p. 071105, 2016.

[6] P. Karioja, J. Ollila, V.-P. Putila, K. Keranen, J. Hakkila, and H. Kopola, "Comparison of active and passive fiber alignment techniques for multimode laser pigtailing," in *2000 Proceedings. 50th Electronic Components and Technology Conference (Cat. No. 00CH37070)*, 2000: IEEE, pp. 244-249.

[7] Y. Gao *et al.*, "Photon-trapping microstructures enable high-speed high-efficiency silicon photodiodes," *Nature Photonics,* vol. 11, no. 5, pp. 301-308, 2017.

[8] C. L. Tan and H. Mohseni, "Emerging technologies for high performance infrared detectors," *Nanophotonics,* vol. 7, no. 1, pp. 169-197, 2018.

[9] V. Logeeswaran *et al.*, "A perspective on nanowire photodetectors: current status, future challenges, and opportunities," *IEEE Journal of selected topics in quantum electronics,* vol. 17, no. 4, pp. 1002-1032, 2011.

[10] H. Cansizoglu *et al.*, "A new paradigm in high-speed and high-efficiency silicon photodiodes for communication—Part II: device and VLSI integration challenges for low-dimensional structures," *IEEE Transactions on Electron Devices,* vol. 65, no. 2, pp. 382-391, 2018.

[11] F. Wang and N. A. Melosh, "Plasmonic energy collection through hot carrier extraction," *Nano letters,* vol. 11, no. 12, pp. 5426-5430, 2011.

[12] L. Du, A. Furube, K. Hara, R. Katoh, and M. Tachiya, "Ultrafast plasmon induced electron injection mechanism in gold–TiO2 nanoparticle system," *Journal of Photochemistry and Photobiology C: Photochemistry Reviews,* vol. 15, pp. 21-30, 2013.

[13] H. A. Atwater and A. Polman, "Plasmonics for improved photovoltaic devices," *Nature materials,* vol. 9, no. 3, pp. 205-213, 2010.

[14] H. Cansizoglu *et al.*, "A new paradigm in high-speed and high-efficiency silicon photodiodes for communication—Part I: Enhancing photon–material interactions via low-dimensional structures," *IEEE Transactions on Electron Devices,* vol. 65, no. 2, pp. 372-381, 2017.

[15] R. H. Hadfield, "Single-photon detectors for optical quantum information applications," *Nature photonics,* vol. 3, no. 12, pp. 696-705, 2009.

[16] C. Bartolo-Perez *et al.*, "Avalanche photodetectors with photon trapping structures for biomedical imaging applications," *Optics Express,* vol. 29, no. 12, pp. 19024-19033, 2021.

[17] M. Ghioni, A. Gulinatti, I. Rech, F. Zappa, and S. Cova, "Progress in silicon single-photon avalanche diodes," *IEEE Journal of selected topics in quantum electronics,* vol. 13, no. 4, pp. 852-862, 2007.

[18] S. Xie *et al.*, "InGaAs/AlGaAsSb avalanche photodiode with high gain-bandwidth product," *Optics express,* vol. 24, no. 21, pp. 24242-24247, 2016.

[19] T. Kellerer, J. Janusch, C. Freymüller, A. Rühm, R. Sroka, and T. Hellerer, "Comprehensive Investigation of Parameters Influencing Fluorescence Lifetime Imaging Microscopy in Frequency-

and Time-Domain Illustrated by Phasor Plot Analysis," *International Journal of Molecular Sciences,* vol. 23, no. 24, p. 15885, 2022.
[20] W. Jahr, B. Schmid, C. Schmied, F. O. Fahrbach, and J. Huisken, "Hyperspectral light sheet microscopy," *Nature communications,* vol. 6, no. 1, p. 7990, 2015.
[21] Z. Yang, T. Albrow-Owen, W. Cai, and T. Hasan, "Miniaturization of optical spectrometers," *Science,* vol. 371, no. 6528, p. eabe0722, 2021.
[22] S. Mauthe *et al.*, "High-speed III-V nanowire photodetector monolithically integrated on Si," *Nature communications,* vol. 11, no. 1, pp. 1-7, 2020.
[23] J. A. Schuller, E. S. Barnard, W. Cai, Y. C. Jun, J. S. White, and M. L. Brongersma, "Plasmonics for extreme light concentration and manipulation," *Nature materials,* vol. 9, no. 3, pp. 193-204, 2010.
[24] M. Ghioni, G. Armellini, P. Maccagnani, I. Rech, M. K. Emsley, and M. S. Ünlü, "Resonant-cavity-enhanced single photon avalanche diodes on double silicon-on-insulator substrates," *Journal of Modern Optics,* vol. 56, no. 2-3, pp. 309-316, 2009.
[25] Z. Yu, A. Raman, and S. Fan, "Fundamental limit of nanophotonic light trapping in solar cells," *Proceedings of the National Academy of Sciences,* vol. 107, no. 41, pp. 17491-17496, 2010.

Chapter 3 Surface passivation of silicon photonic devices integrated with photon trapping structures

Recently, many high-speed and high-efficiency silicon optoelectronics devices are demonstrated by enabling photon trapping micro/nanostructures. These structures introduce high surface-to-volume ratio micro/nanostructures created by the top-down dry etching process. However, the etching process brings challenges such as creating silicon surface damages, dangling bonds, and crystalline defects [Fig. 3.1 (a)].

3.1 Challenges

Semiconductor surfaces inherently exhibit dangling bonds in their natural unpassivated state [1]. The surface states exist at the dangling bonds on an s − p crossing substrates such as Si and Ge and influence the energy states within the bandgap [2]. Theoretical studies showed that there is a high probability of electrons existing at the edge of atoms [2]. Dangling bonds will form metallic conduction channels, as predicted in [3], and these channels will support undesirable dark current. Dangling bonds support metallic channels, provide surface states, or may cause trap centers, and therefore, they must be eliminated for PD applications. Dangling bonds on Si surfaces can be terminated by hydrogenation, forming Si—H bonds at the surfaces, and thus reducing the conducting paths and trapped charged carriers on the surfaces. This can be achieved by immersing the c-Si in diluted hydrofluoric acid (HF) solution [4, 5]. The HF bath is a standard RCA clean step for CMOS wafers, and this passivation technique can be cost-effective. Other commonly used passivation schemes for Si surfaces can be achieved by adding additional thin dielectric layers using atomic layer deposition (ALD) [6, 7], thermal oxidation [8, 9], or plasma-enhanced chemical vapor deposition (PECVD) [10, 11]. In contrast, low ion energy etching (LIEE) is an alternative process that uses the minimum plasma energy to etch off or remove a shallow layer of the already damaged c-Si surfaces without causing additional damage[12, 13]. In this chapter, multiple surface passivation schemes, including HF treatment, PECVD, thermal

oxidation, and LIEE, are utilized to suppress the dark current level of the photon trapping micro/nanohole-enabled Si PIN PDs and ultimately achieve desirable external quantum efficiency (EQE). More than 3 or 4 orders of magnitude of dark current reduction have been observed by all the passivation techniques. Unlike most PV applications, our Si PIN PDs have highly doped n+ and p+ layers for high-speed operation. Thus, the quality of each passivation scheme is assessed based on the EQE of the PDs to reflect the overall effect on the PDs. The results in this chapter are CMOS compatible and can also be applied to many other photonic device applications.

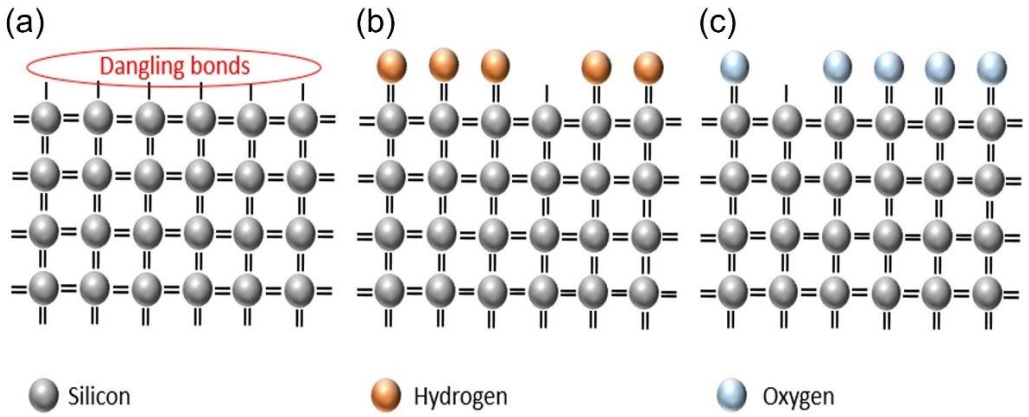


Fig. 3.1. The schematic of c-Si surfaces for different surface compositions. (a) Unpassivated c-Si surfaces. (b) Passivated c-Si surface with hydrogen. (c) passivated c-Si surface with SiO_2.

3.2 Device fabrication

The detailed fabrication processes of the PDs are described in chapter 4. In brief, the PIN Si wafer was pre-cleaned using the RCA standard cleaning procedure to remove organic, oxide, and ionic residues. Deep ultraviolet (DUV) resist was spin-coated and optimized around 1.7 μm on the wafer and patterned with DUV photolithography. After that, reactive ion etch (RIE) and/or deep reactive ion etch (DRIE) were used to create different sizes (630-1500 nm) of the holes on the silicon surface as shown in Fig. 3.2 (b) and (c). Then, the top mesa and bottom mesa were defined by another RIE etch. Both holes and mesa etch involved bombardment of high-energy ions and plasma on the silicon surfaces and sidewalls. This process would create a large number of defects on those surfaces. Different passivation schemes have been applied before the final deposition of ohmic contacts composed of 10 nm Ti, 100 nm Al, and 20 nm Pt as shown in Fig.

3.2 (a) and (c). Compared to most PV applications, the nn and pp type layers in our PDs are more heavily doped to minimize the minority carriers' lifetime and increase the recombination so that the PDs can have a faster response speed. These highly doped layers bring new challenges to the passivation schemes as their qualities would be assessed by the specific PD application.

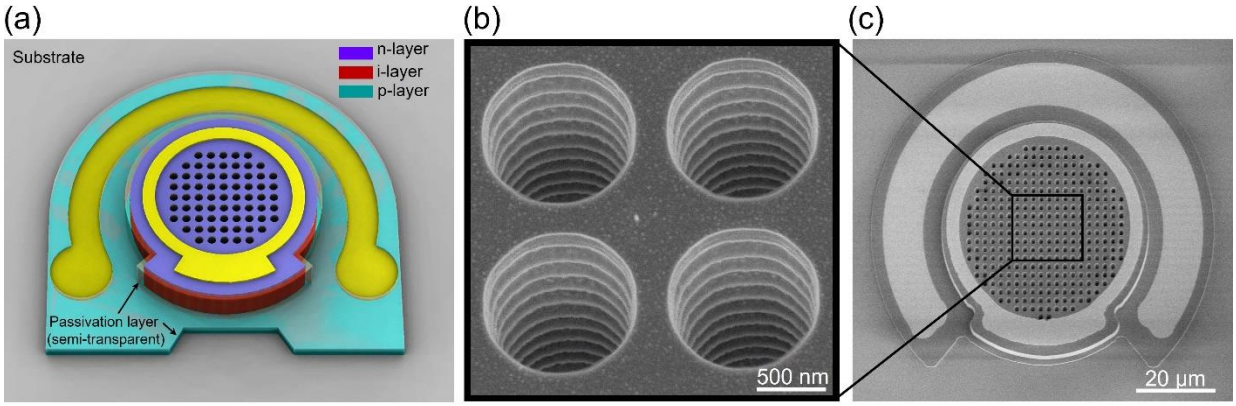


Fig. 3.2. (a) Schematics of photon-trapping nanoholes in a Si PIN PD. Color-coded layers represent: blue, n+ phosphorus doped Si layer (0.25 μm); red Si layer (1.5 μm); turquoise p+ boron doped Si layer (0.5 μm); grey, SOI substrate; yellow, ohmic metals on top and bottom mesas; semi-transparent layers represent passivation layers (b) Enlarged SEM image of the etched holes with a diameter ~ 1 μm. (c) SEM image of complete fabricated PD device.

3.3 EQE and dark current measurement

The I-V characteristics of the PIN Si PD were recorded under both dark and laser illumination conditions. The dark current level of the PD reflects the quality of the passivation.

The ratio of the number of excess electrons to the number of incident photons provides the external quantum efficiency (EQE) of a photodiode/photodetector (PD). The EQE of a PD can be calculated using the following equation (3.1):

$$EQE = \frac{I_{ph}/e}{P/h\omega} \tag{3.1}$$

where I_{ph} is photocurrent, e is one electron charge, P is the incident optical power and $h\omega$ is the energy of a single photon. A supercontinuum laser integrated with a tunable filter was used to conduct EQE measurements for the range of 800-900 nm with 5 nm increment. The light is coupled to the devices by a single-mode fiber probe on a probe station.

3.4 Unpassivated devices

Micro/nanostructures create high surface-to-volume ratio holes which are fabricated by RIE or DRIE. This process induces more defects on the surface. As shown in Fig. 3.3 (a), the dark current is around 11.5 mA for unpassivated PD with holes at -7V, and the dark current is 0. 21 mA for unpassivated PD without holes. The RIE damage-induced surface area of the PD with holes is much larger than the one without holes. The main surface states locate on the sidewall of the mesa for the PD without holes; however, for the PD with holes, they also reside on the hole's sidewall, the bottom of the holes beside the mesa sidewall. For example, for a 100 μm diameter PD device without holes, the damage-related surface area is around 800 μm^2; for a PD device of the same size with holes, it is estimated to be approximately 25,000 μm^2. This is the main cause of the large dark current increase of the PD device with holes compared to the one without holes. The surface states can also be detrimental to the carriers' collection in the PD. For an ideal PD, the photo-response or EQE does not change according to the applied reverse bias. However, as shown in Fig.3.3 (b), the EQEs of the unpassivated PD with holes between 800-900 nm are rather voltage-dependent, the EQEs at -10V are higher than those at -3V for all the wavelengths. In contrast, although the EQEs of unpassivated PD without holes are significantly lower than the ones with holes, they are not as much as voltage dependent (EQE differences are only a couple of percentage at −3 V and −10 V for PDs without holes).

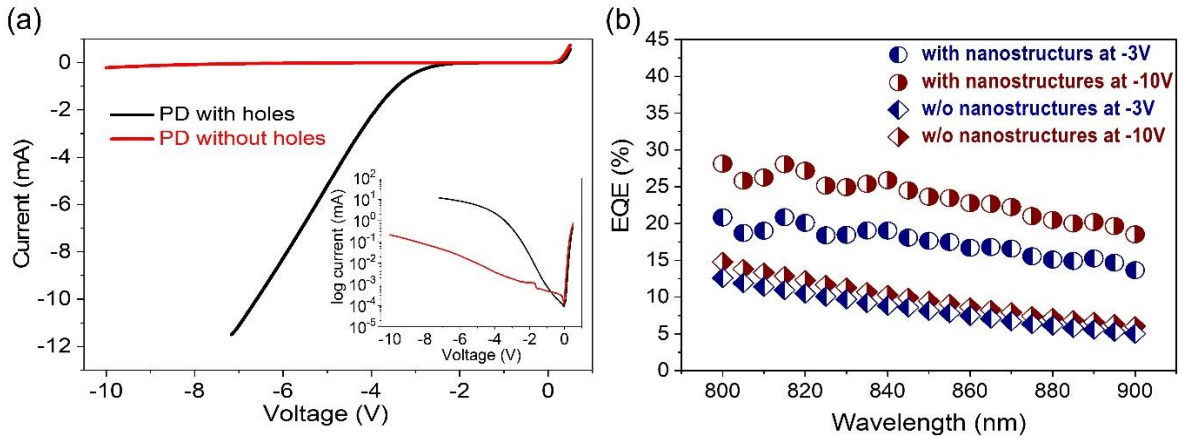


Fig. 3.3. (a) Current-voltage (I-V) characteristics of unpassivated PDs with holes (black solid line) and without holes (red dash line) after RIE and DRIE steps under dark conditions. Inset shows the log-linear

plot. (b) EQE of unpassivated PDs with holes at a reverse bias of -3V and -10V for wavelengths of 800-900 nm.

These phenomena suggest that the micro/nanoholes can effectively increase the EQEs of the PD; however, since they also create more surface area and damaged surfaces due to the dry etching, many photon-generated carriers can be trapped inside these surface states and require a higher voltage to be collected sufficiently [Fig. 3.4]. Although these high aspect ratio micro/nanostructures are very effective for photon-trapping, light-manipulating and are fundamentally important for achieving high quantum efficiency and high speed in PIN Si PDs [14], they would cause high noise levels in the PDs and would require higher operation voltage if left untreated/unpassivated. Besides reliability issues, a low operation voltage of PD is essential for the integration to the CMOS circuit.

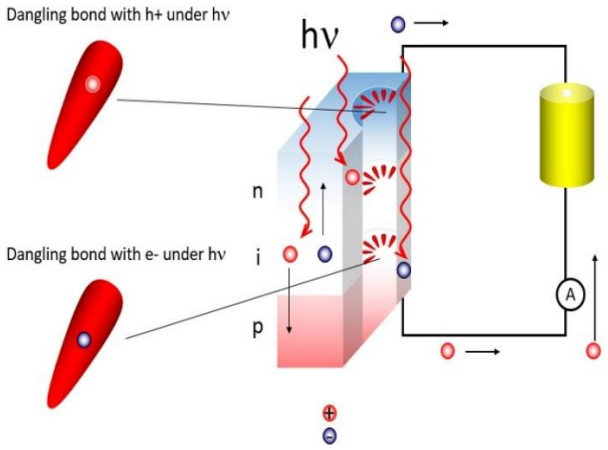


Fig. 3.4. Schematic of a photodetector presenting surface dangling bonds where a portion of the generated carriers are trapped due to the dry holes etching.

3.5 Passivation processes

This chapter includes four types of passivation schemes for the fabricated PDs: (1) alternate PECVD layers of SiO_2 and Si_3N_4; (2) thermal oxidation; (3) LIEE using minimum amount of plasma energy; and (4) hydrogenation by HF treatment.

PECVD passivation was done by depositing one layer of Si_3N_4 sandwiched by two SiO_2 layers at 350^{o} C. For better passivation and parasitic capacitance reduction, multiple PECVD film stacks

are employed in our study instead of one single layer of silicon oxide or silicon nitride film as PIN holes may exist in a single film by low-temperature PECVD process [15, 16]. SiH_4, N_2O, and Ar precursor gases are used to grow SiO_2 dielectric layer. Whereas SiH_4, NH_3, and Ar are used for the Si_3N_4 layer growth.

Thermal oxidation of Si surfaces was done by atmospheric wet thermal oxidation in a thermal furnace at 900^o C to grow a conformal layer of oxide around 120 nm thick. DI water vapor is used for wet oxidation in our process.

LIEE of the damaged Si was done by RIE with an RF forward power of 300 W and a minimum allowable bias power of 3 W. The Si etch gases include HBr and Cl_2, and around 50 nm of the silicon surface is etched off during the 2 min process. Compared to a standard silicon RIE process with a forward power of 300 W and a bias power of 150 W. The etch rate of silicon is greatly reduced to almost 1/10 as the ion energy is greatly reduced by the reduced bias power.

Hydrogenation of the damaged Si surface states was done by simply immersing the Si PIN PD wafers into HF solution (HF: H_2O= 1:10) for 15 seconds after the holes and mesas dry etch.

3.1.1 PECVD stack layers passivation

PECVD dielectric tri-layers film composed of 220 nm SiO_2, 80 nm Si_3N_4, and 220 nm SiO_2 are deposited sequentially on the PIN PD devices after holes and mesa etch for passivation. Figure. 3.5 (a) and (b) show this oxide-nitride-oxide (ONO) passivation layer on the hole's region and mesa sidewalls, respectively. It should be noted that this ONO passivation layer is not conformal on the high-aspect-ratio micro/nanoholes (630-1500 nm in diameter, and around 3 µm in depth): the passivation layer thickness is uniform on the top surface, but the thickness gradually reduces on the sidewall of the holes, and it seems that there is no passivation film at the bottom surface of the holes. However, for large features such as the device mesas (mesa diameters are usually 30-500 µm, and the depth is around 3 µm), the passivation layers tend to have full coverage on both top and bottom surfaces as well as the sidewalls as can be seen in Fig. 3.5 (b). This is

possibly caused by the low-temperature process of PECVD, the precursor gas may not be efficiently delivered inside the high-aspect-ratio features, leading to a relatively poor step coverage, especially on the sidewall and bottom of such nanostructures.

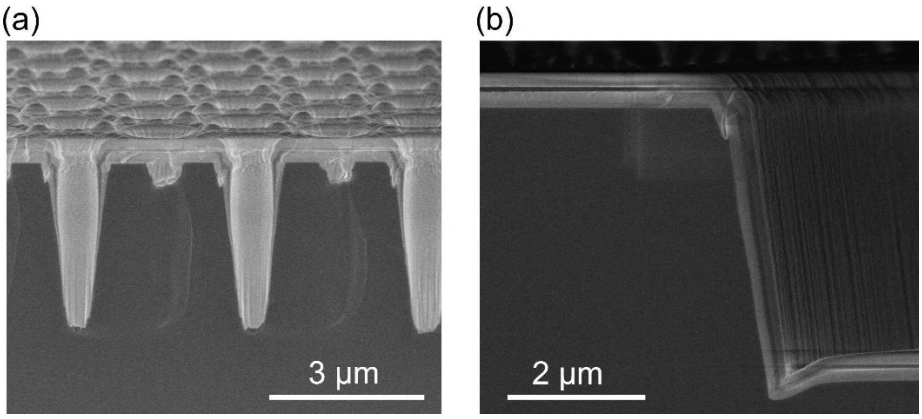


Fig. 3.5. (a) Cross-sectional SEM of the ONO passivation tri-layers on the nanostructures ; the holes are created by RIE with tapering sidewall angle, and they are 1300 nm in diameter, 2000 nm in period, and 3 μm in depth. (b) Cross-sectional SEMs of the ONO passivation layer on the mesa sidewall. ONO passivation is composed with one 80 nm thick Si3N4 film (darker film in the middle) sandwiched by two 220 nm thick SiO2 films (brighter film on both sides).

Although PECVD ONO passivation doesn't have full coverage of the holes, the dark current level is reduced by more than three orders of magnitude to around 960 nA at -10V, as shown in Fig. 3.6 (a). Interestingly, measured EQE of the PD with holes has increased after ONO passivation, and some resonant peaks (i.e. around 820, 850, and 870 nm) can be noticed in Fig. 3.6 (b). SiO_2 and Si_3N_4 film has a lower refractive index than Si and can reduce some of the surface reflection and allow light to penetrate into the PDs, and thus play a role in improving the EQE of the PDs. In addition, as will be discussed in chapter 4, the dimensions/designs of the nanoholes also affect the overall EQE of the PDs. In this case, the reduced diameter of the holes by the ONO layer can also contribute to the EQE increase. On the other hand, the ONO passivation structure is very similar to antireflective (AR) coating, and this may explain the resonant peaks at a few specific wavelengths. The suppression of the dark current by the ONO passivation scheme is acceptable, however, we still notice there is a slight EQE voltage dependency after ONO passivation. The inability of the PECVD ONO passivation layer to fully passivate all the surfaces inside the holes

still provides traps for the photon-generated minority carriers and requires higher voltage to fully collect them.

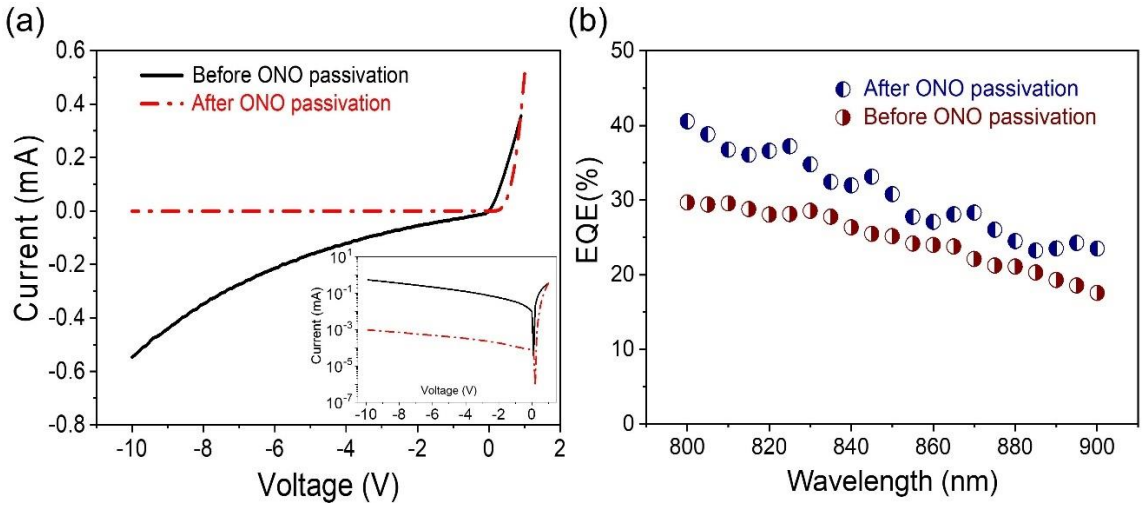


Fig. 3.6. (a) Current-voltage characteristics of PDs with holes before ONO passivation (black solid line) and after ONO passivation (red dashed line). Inset shows the log-linear plot. (b) EQE of PDs with holes before (red) and after (blue) at reverse bias of -10V for 800-900 nm wavelengths.

3.1.2 Thermal oxidation passivation

To improve the surface coverage of the high-aspect-ratio micro and nanoholes of the Si PDs, wet thermal oxidation is used to passivate the silicon surface. As illustrated in Fig. 3.7 (a) and (b), the thermal oxide layer has very conformal coverage of the holes in the PD. The thermal oxide layer thickness is around 120 nm, consistent in both the top and the bottom surfaces of the holes as well as the sidewall. Unlike PECVD process with precursor gases, thermal oxidation consumes the Si on the surfaces and transforms it into SiO_2. Due to the different molecular densities of Si and SiO_2, the volume of SiO_2 will be 2.16 times larger than the consumed Si. Taking this into consideration, around 56 nm Si surface has been transformed into SiO_2. It is reported that around 50 to 100 nm of Si surface can experience material damage throughout dry the etching process by physical ion bombardment [17, 18], and our thermal oxidation layer thickness can theoretically turn these damaged Si surfaces into SiO_2 dielectric layer, and therefore serve the passivation purpose.

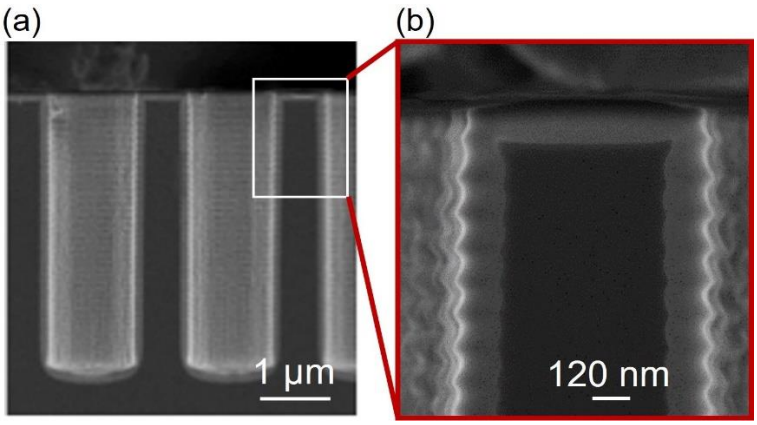


Fig. 3.7. (a) Cross-sectional SEM micrograph of the oxide layer uniformly deposited on the region of the hole by wet thermal oxidation; (b) Zoom-in image of fig (a) indicated by the arrow, showing the oxide layer is around 120 nm both on the top surface and sidewalls of the holes.

As shown in Fig. 3.8 (a), thermal oxidation passivation is very effective to reduce the dark current by more than four orders of magnitude to 260 nA at -10V. Figure. 3.8 (b) also shows that after the thermal oxidation, the EQEs of the PDs are not voltage-dependent, showing identical values at both -3 and -10V. This suggests that thermal oxidation has successfully removed the damaged Si surface, and it only needs a relatively low voltage to collect all the photon-generated carriers. However, compared to the unpassivated PDs, the EQEs of the PD after oxidation passivation have a noticeable drop. As it is discussed earlier, the SiO_2 layer can reduce the reflection and would help to improve the EQE a bit. In the meantime, the holes' dimension change by thermal oxidation is much smaller compared to the PECVD stack layers' growth. This EQE drop is likely to be caused by the dopant diffusion due to the prolonged high-temperature process. Since our PD has heavily doped n^+ and p^+ layers, under high temperature, these dopants can diffuse to the intrinsic region and cause the effective width of the depletion layer to shrink under the PD operations, thus resulting in reduced absorption of the photons (reduced EQE of the PDs). This is also confirmed by the increased capacitance values of the PDs after oxidation due to a reduction in the thickness of the depletion layer. In that sense, oxidation-based passivation is able to consume the damaged Si surface caused by dry etching, but the high-temperature process

changes the designed dopants concentration profile in our PDs. Thus, oxidation-based passivation is not a favorable passivation method for our device.

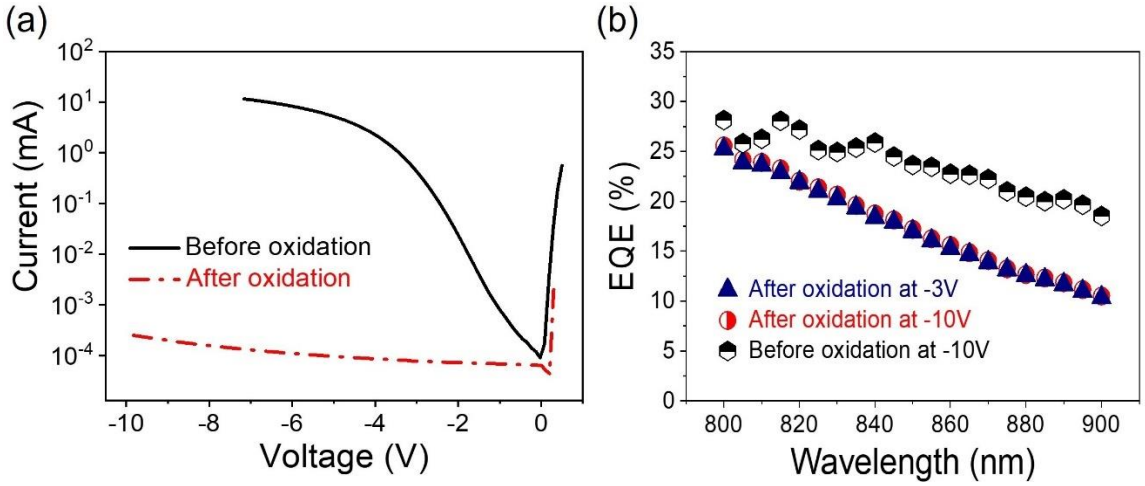


Fig. 3.8. (a) Log-linear Current-voltage characteristics of PDs with holes before thermal oxidation passivation (black solid line) and after thermal oxidation passivation (red dashed line); (b) EQE of PDs with holes before oxidation at -10V (black hexagonal) and after oxidation at both -3V (blue triangle) and -10V (red circle) for 800-900 nm wavelengths.

3.1.3 LIEE surface treatment/passivation

LIEE is an alternative process to remove the damaged Si surfaces and decreases dangling bonds and surface charging effects. LIEE can be performed in the same chamber as the standard RIE process by reducing the bias power. High ion energy etching introduces surface defects, while low ion energy etching can slowly remove surface defects with less surface defects [Fig. 3.9].

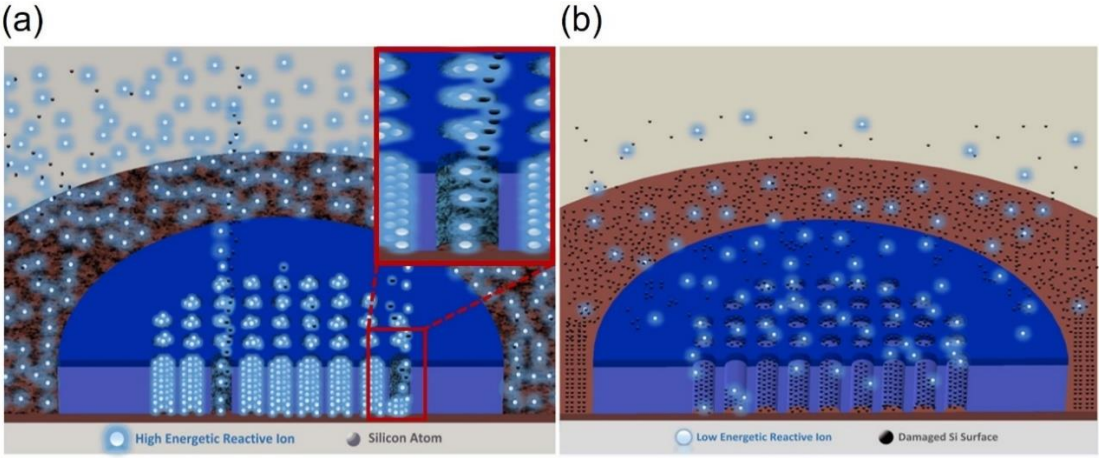


Fig. 3.9. C-Si PIN nano-holes device top-down fabrication by a reactive ion etching process. (a) C-Si PIN device top-down fabrication by high energy reactive ion etching. High energetic ion bombard Si surface to knock out Si atoms which induce damaged surfaces. Inset is a magnified view of highly energetic ions

bombarding nano-holes and knocking out c-Si atoms and leaving behind walls and bottom damaged surfaces. (b) Low energetic reactive ions etching slowly damaged c-Si surfaces and cleaning damaged affected devices surfaces.

A LIEE calibration has shown that the silicon etches rate is around 25 nm/min under the minimum allowable bias power of 3W in our tool. For practical purposes, RIE with an etch rate of 250 nm/min was used first, and LIEE was performed right after the standard RIE process for both holes and mesa etch [Fig. 3.10].

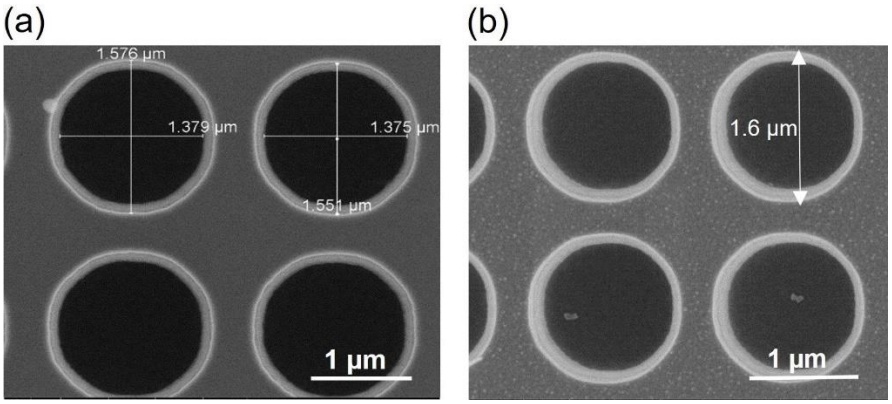


Fig. 3.10. (a) SEM images of nano-holes diameters after fabricating the device which induces a huge number of damaged surfaces. (b) Nano-hole diameters after etching ~100nm damaged nano-hole's sidewalls which increased the diameter 100 nm by LIEE process.

Figure. 3.11 shows the passivation quality of LIEE method. The dark current level has been suppressed by more than four orders of magnitude, down to 460 nA. However, similar to the PECVD passivation, the EQEs of PDs with LIEE passivation is still voltage dependent. This suggests that there are still many surface states on the silicon that could not be removed by LIEE, and result in some loss in the carrier collections. Overall, compared to other passivation schemes, LIEE is scalable and controllable, and most importantly, it can be easily implemented in the same etch system right after RIE, and may have advantages in yield and productivity.

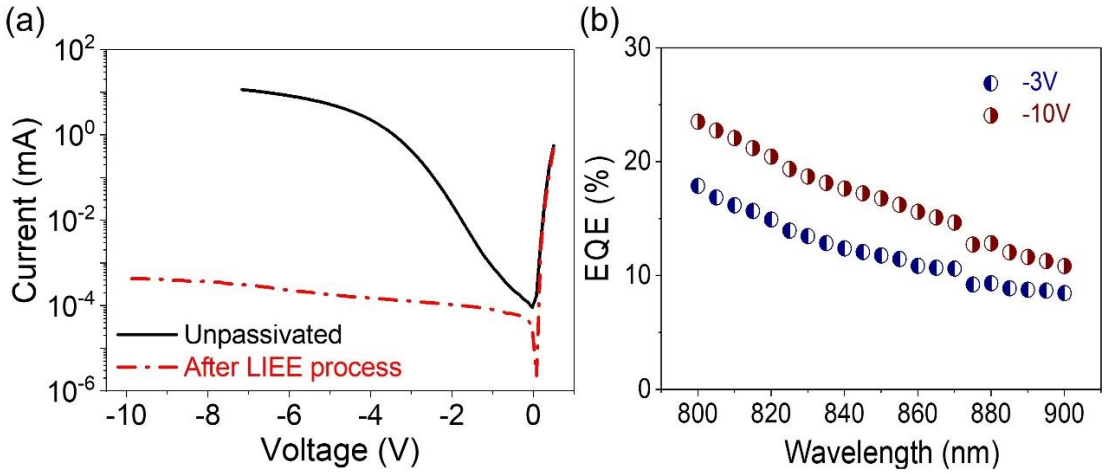


Fig. 3.11. (a) Log-linear I-V characteristics of PDs with holes without LIEE (black solid line) and with LIEE passivation (red dashed line). (b) EQE of PDs with holes after LIEE passivation at both −3 V (blue circles) and −10 V (red circles) for 800–900 nm wavelengths. The holes are created by RIE with a tapering sidewall angle, and they are 1500 nm in diameter, 2000 nm in the period, and around 3 μm in depth.

3.1.4 Hydrogenation by HF treatment

Saturating the dangling bonds with hydrogen atoms (hydrogenation) eliminates dangling bonds, surface states, and metallic channels, as shown theoretically in [2]. Experimentally, hydrogenation of dangling bonds can be achieved with HF treatments, where Si dangling bonds exclusively react with H ions. Figure. 3.12 (a) shows that the dark current of the PD with holes is reduced to less than 160 nA at -10V, more than four orders of magnitude reduction compared to the unpassivated PDs. Among all the passivation schemes discussed in this chapter, hydrogenation passivation provides the smallest dark current level of the PD with holes. Figure. 3.12 (b) indicates that the EQEs of the PDs with holes after HF passivation has improved compared to the ones before HF treatment and show no sign of voltage dependency. This suggests that most of the surface states and dangling bonds have been successfully passivated by the hydrogen atoms, and only a smaller voltage is able to create the full depletion width and sweep all the photon-generated minority carriers.

Under normal storage conditions (room temperature and ambient environment) of our PDs, we keep track of the dark current level of many Si PDs with photon-trapping holes after the HF treatment. After one year, the dark current level of most PDs is still in the range of 100-300 nA.

Thus, hydrogenation by HF treatment offers a facile, low temperature, low-cost passivation technique for the PDs with high-surface-to-volume nanostructures.

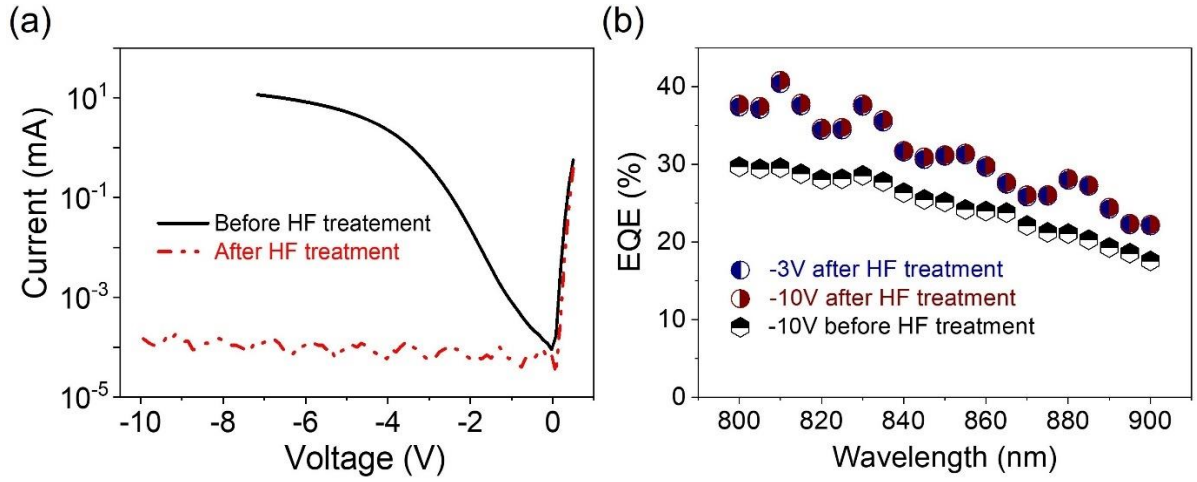


Fig. 3.12 (a) Log-linear current-voltage characteristics of PDs with holes before (black solid line) and after (red dashed line) HF treatment; (b) EQE of PDs with holes before HF treatment at -10V (black hexagonal) and after HF treatment at both -3V (blue circle) and -10V (red circle) and before for 800-900 nm wavelengths.

3.6 Comparison of different passivation schemes

several surface passivation techniques including PECVD ONO stack layers, thermal oxidation, LIEE, and hydrogenation by HF treatment are studied to identify their effects on dark current and EQEs of Si PIN PDs with high-surface-to-volume ratio nanostructures for optical communication applications. Table. 3.1 shows a summarized comparison of the overall quality of these passivation schemes on the PDs. The passivation schemes presented in this paper can reduce the density of surface states on the Si surfaces induced by the top-down dry etching processes while fabricating the micro-/nanoholes. All the passivation schemes discussed in this chapter can suppress the dark current to an acceptable level (a nA range); however, some techniques may affect the EQE of the PDs by either changing the dimension of the holes, surface refractive index or causing unintended dopants diffusion. These results offer essential insights for optimizing the performance of Si PIN high-speed based on high aspect ratio nanostructures, especially with heavily doped p and n layers that serve as contact layers. The results can be applied to PV application, as well.

Passivation Schemes	PECVD	Oxidation	LIEE	HF
Dark Current Suppression	> 3 orders	> 4 orders	> 4 orders	> 4 orders
Dimension change of the nanostructures	Yes	Yes, small	Yes, small	No
Refractive index change on the surface	Yes	Yes	No	No
Surface states removal	Partial	Complete	Partial	Complete
PD EQE voltage dependency	Yes/slightly	No	Yes	No
Changes in the EQE	Yes	Yes	Negligible	Yes
Process Temperature	Relatively low	High	Low	Low

Table. 3.1. Comparison of Different Passivation Schemes on the Si *pin* PD with High Surface-to-Volume-Ratio Nanostructures

References

[1] M. Tao, D. Udeshi, N. Basit, E. Maldonado, and W. P. Kirk, "Removal of dangling bonds and surface states on silicon (001) with a monolayer of selenium," *Applied physics letters,* vol. 82, no. 10, pp. 1559-1561, 2003.

[2] T. Yamada, C. W. Bauschlicher, and H. Partridge, "Substrate for atomic chain electronics," *Physical Review B,* vol. 59, no. 23, p. 15430, 1999.

[3] W. Shockley, "On the surface states associated with a periodic potential," *Physical review,* vol. 56, no. 4, p. 317, 1939.

[4] Y. Chabal, G. Higashi, K. Raghavachari, and V. Burrows, "Infrared spectroscopy of Si (111) and Si (100) surfaces after HF treatment: Hydrogen termination and surface morphology," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films,* vol. 7, no. 3, pp. 2104-2109, 1989.

[5] H. Ubara, T. Imura, and A. Hiraki, "Formation of Si・H bonds on the surface of microcrystalline silicon covered with SiOx by HF treatment," *Solid State Communications,* vol. 50, no. 7, pp. 673-675, 1984.

[6] Y. Bao, M. Laitinen, T. Sajavaara, and H. Savin, "Ozone-based atomic layer deposition of Al2O3 from dimethylaluminum chloride and its impact on silicon surface passivation," *Advanced Electronic Materials,* vol. 3, no. 6, p. 1600491, 2017.

[7] T. Pasanen, V. Vähänissi, N. Theut, and H. Savin, "Surface passivation of black silicon phosphorus emitters with atomic layer deposited SiO2/Al2O3 stacks," *Energy Procedia,* vol. 124, pp. 307-312, 2017.

[8] O. Schultz, A. Mette, M. Hermle, and S. W. Glunz, "Thermal oxidation for crystalline silicon solar cells exceeding 19% efficiency applying industrially feasible process technology," *Progress in Photovoltaics: Research and Applications,* vol. 16, no. 4, pp. 317-324, 2008.

[9] N. Balaji, S. Q. Hussain, C. Park, J. Raja, J. Yi, and R. Jeyakumar, "Surface passivation schemes for high-efficiency c-Si solar cells-A review," *Transactions on Electrical and Electronic Materials,* vol. 16, no. 5, pp. 227-233, 2015.

[10] S. Mack *et al.*, "Silicon surface passivation by thin thermal oxide/PECVD layer stack systems," *IEEE Journal of Photovoltaics,* vol. 1, no. 2, pp. 135-145, 2011.

[11] D. R. Kim, C. H. Lee, P. M. Rao, I. S. Cho, and X. Zheng, "Hybrid Si microwire and planar solar cells: passivation and characterization," *Nano letters,* vol. 11, no. 7, pp. 2704-2708, 2011.

[12] A. S. Mayet *et al.*, "Inhibiting device degradation induced by surface damages during top-down fabrication of semiconductor devices with micro/nano-scale pillars and holes," in *Low-Dimensional Materials and Devices 2016*, 2016, vol. 9924: SPIE, pp. 36-42.
[13] A. S. Mayet *et al.*, "Surface passivation of silicon photonic devices with high surface-to-volume-ratio nanostructures," *JOSA B,* vol. 35, no. 5, pp. 1059-1065, 2018.
[14] Y. Gao *et al.*, "Photon-trapping microstructures enable high-speed high-efficiency silicon photodiodes," *Nature Photonics,* vol. 11, no. 5, pp. 301-308, 2017.
[15] P.-Y. Gao, L. You, and R. J. Huang, "Method for forming a hardmask employing multiple independently formed layers of a PECVD material to reduce pinholes," ed: Google Patents, 2004.
[16] S. Wang, A. Lennon, B. Tjahjono, L. Mai, B. Vogl, and S. Wenham, "Overcoming over-plating problems for PECVD SiNx passivated laser doped p-type multi-crystalline silicon solar cells," *Solar Energy Materials and Solar Cells,* vol. 99, pp. 226-234, 2012.
[17] G. Kumaravelu, M. Alkaisi, A. Bittar, D. MacDonald, and J. Zhao, "Damage studies in dry etched textured silicon surfaces," *Current Applied Physics,* vol. 4, no. 2-4, pp. 108-110, 2004.
[18] S. Pang, "Surface damage induced by dry etching," in *Handbook of Advanced Plasma Processing Techniques*: Springer, 2000, pp. 309-360.

Chapter 4 Enhancing optical efficiency and operational speed of Si PIN photodetectors by integrating photon trapping structures and lateral optical modes propagation

4.1 Photon trapping theory implementation in Si photodetectors

Many researchers investigated several wide-spectral photon-trapping schemes for a variety of applications including photovoltaic (PV) devices to address the weak optical absorption in Si [1-3]. Such schemes include the formation of micro and nanowires [4], nanoholes [5], photonic crystals [2, 6] and graded-index multilayer films that exhibited efficient absorption by trapping the photons and thereby enhancing the absorption possibly with the generation of lateral modes at near infra-red (NIR) wavelengths where absorption coefficient is < 1000 cm^{-1}. Recently, based on a similar approach, near unity absorption was demonstrated for solar cells with absorption thickness of ~10 µm [7].

The designed PDs have 2D periodic nanoholes, whose cross-sections are in the *x-y* plane and axes are in the *z*-direction, as shown in Fig. 4.1. The nanohole array supports a set of modes depending on the parameters of the array, collective modes are formed similar to the modes in photonic crystals [2]. The analysis of photonic crystals reveals that under certain parameters, slow modes can appear. Several research showed that slow modes can contribute to considerably higher absorption [8].

The longer the waves propagate into *i*-region the better is the absorption for a wider range of the wavelength. The PD diameter in *x-y* plane is much larger than that of the thickness of the *i*-region and the modes in *x-y* plane are absorbed almost completely compared to the modes propagating in the *z* direction. At the same time the photocurrent generated in the *i*-region flows in the *z* direction that allows us to achieve high-speed operation because of its narrow thickness and hence small transient time. The effect is similar to the Lambertian reflector that helps to trap light in Si [9]. The Lambertian limit for the enhanced absorption length is $4n^2L$, where *n* is the refractive

index of Si and *L* is the absorption length. The limit can be exceeded for the nanoholes if most of the light modes supported by the nanohole structure are trapped in *x* and *y* directions until it gets completely absorbed.

Photon-trapping (PT) theory successfully converts of an initial incident vertical plane wave to an ensemble of lateral collective modes realized in a 2D periodic array of nanoholes. Figure. 4.1. shows a nanohole arrays illuminated with a vertical plane wave that generates laterally propagating modes. The initial transient time-evolution from time t = 0 to 21 femtoseconds is depicted in the figure for the 2D periodic boundary condition. The simulation includes the SOI (SiO_2) bottom layer and was done for several wavelengths in the range of 800-950 nm. This is the result of finite-difference time-domain (FDTD) simulations that shows the lateral waves appear around the holes and form the collective lateral modes with time. These basic features were the same for different wavelengths and we showed only the simulations for 850 nm in Fig. 4.1.

FDTD simulation results for cylindrical holes and tapered/funnel-shaped holes are shown in Fig. 4.1 (a) and Fig. 4.1 (b), for the wavelength 850 nm, respectively. The size, depth and the shape profile of the nanoholes can have influence on the initial generation of lateral modes and intensity distribution between the *n, i* and *p* regions. Photons can be trapped between the top and the bottom boundaries of the hollow nanoholes if the relation between k_z and k_c satisfy the condition for the full reflection. The lateral waves start to form in the *x-y* plane and is trapped in Si. Light propagation in a 2 μm layer without nanoholes is about 6.7 fs. The simulation shows with nanoholes, the duration of the optical field in the material is over 55 fs, or about over 8 times longer. The longer the optical field stays in Si, the more it gets absorbed by the photodetector (PD).

The simulations used Si material and the perfectly matched layer (PML) boundary conditions in the lateral directions. The PDs are simulated numerically using FDTD to examine absorption for the wavelength range 800-900 nm under the boundary condition in the PML formulation with the Si complex permittivity.

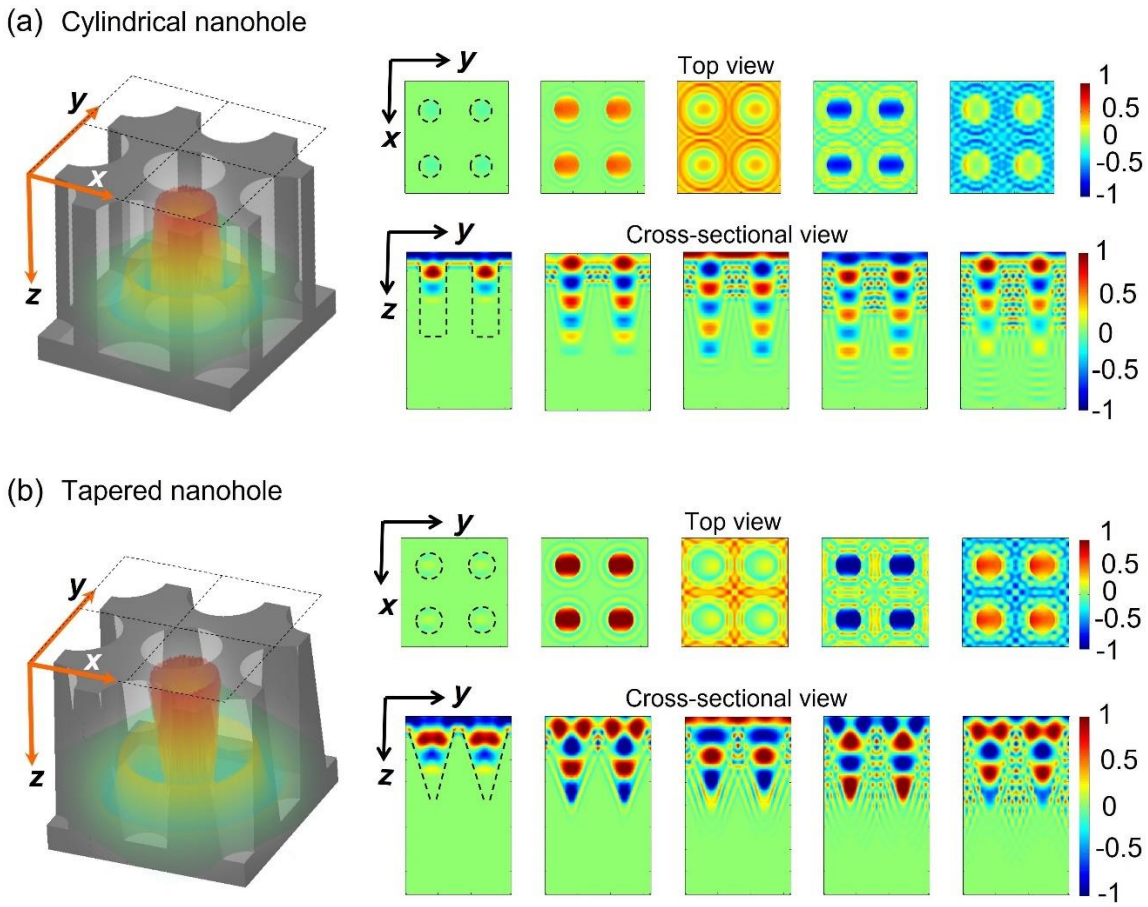


Fig. 4.1. Nanohole designs on Si illuminated by a normal incident beam of light. (a) Cross-sectional square lattice pattern of cylindrical holes showing a vertically oriented photons beam propagating in the lateral orientation. FDTD numerical simulations show the formation of a lateral modes around holes with diameter 1500 nm arranged in a lattice with period 2000 nm: E_x components of the field in the square lattice for cylindrical holes with time increasing from left to right. Top row shows the *x-y* plane with light illuminating the holes in *z* direction and bottom row shows *y-z* plane with light illuminating the holes from the top to the bottom. The time changes from the left to the right as t=1.4 femtoseconds (fs), 6.2 fs, 11 fs, 16 fs, 21 fs. The field first goes into the hole and then it spreads into Si as cylindrical waves. (b) Cross-sectional square lattice of tapered holes exhibiting photon propagation in the lateral orientation. Tapered nanoholes are designed with 2000 nm period 1700 nm hole diameter and a tapering angle of 66^o. The top row shows the E_x component of the field in *x-y* plane with light coming from the *z* direction and the bottom row shows the *y-z* plane with light coming from the top to the bottom. The time is changing from the left to the right as t=1.4 fs, 6.2 fs, 11 fs, 16 fs, 21 fs.

4.1 Device design

The Si photodetector was designed as P-doped layer/ Intrinsic layer (i-layer) / N-doped layer (PIN) and (NIP) configuration. The photodetector structure was epitaxially grown on an SOI substrate that has 0.2 µm device layer (*p*-Si) [Fig. 4.2 (b)]. The thin absorption region is designed to have 2 µm thick *i*-Si to minimize the transit time for electrons and holes. A lattice matched 0.25 µm p^{++}

$Si_{0.988}Ge_{0.01}B_{0.002}$ was used as the bottom *p*-contact layer, as well as an etch-stop layer for the *n*-mesa isolation process. A 0.25 µm phosphorus doped n^{++} thin layer served as the top *n*-ohmic contact. High doping decreases the minority carrier lifetime and minimizes the diffusion of photo-carriers generated in the *n* and *p*-layers into the high field *i*-region, in addition to reducing the series resistance. Figure 4.2 (a) shows a schematic of the complete fabricated devices with coplanar waveguide (CPW) which is used for the RF high-speed measurements. An array of nanoholes is introduced and optimized to develop a photon trapping photosensors while a control/planar photosensor (with no nanoholes) as a reference device. Figure 4.2 (b) shows the cross-sectional details of the fabricated devices. The structure was optimized for top-illumination by multimode optical fiber.

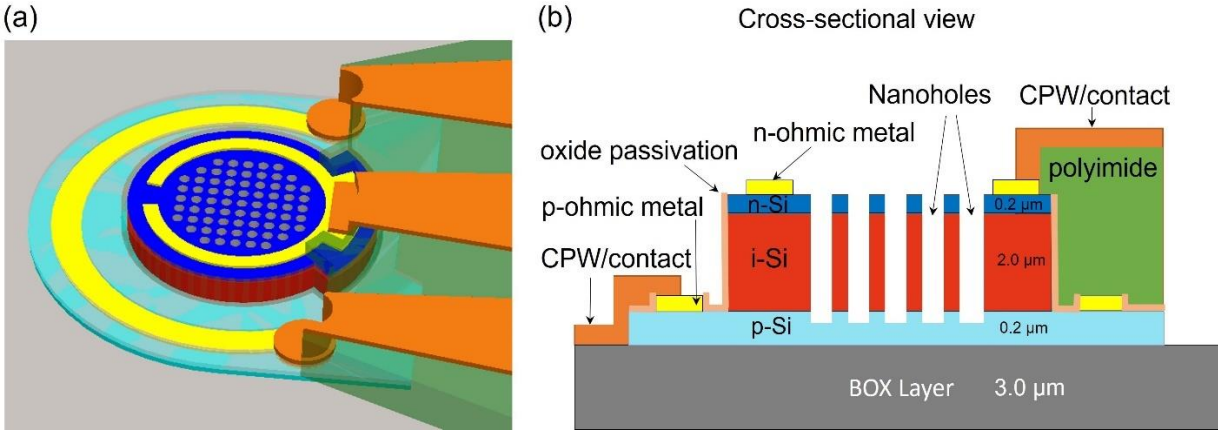


Fig. 4.2. Schematics of the nanoholes Si PD design. (a) Top-view of the Si PT PD. (b) Cross-sectional view.

4.2 Optical Simulation and Optimization

To reach a maximum optical efficiency at 850 nm with only 2 µm thin Si layer that allows high-speed PD operation more than 25 GHz 3dB bandwidth, many photon trapping structures are simulated numerically using Finite-Difference Time-Domain (FDTD). Figure 4.3 (a) depicts the propagation of lateral modes in an area that was not illuminated. Light absorption in Si is expressed using a complex dielectric permittivity based on the Lorentz model with the parameters that fit crystalline Si at wavelengths of 800–900 nm. The simulations used the perfectly matched

layer (PML) boundary conditions in the lateral directions. Only the leftmost column of funnel-shaped holes was illuminated, and it can be seen that the lateral modes propagate into the non-illuminated area, with amplitude decreasing with distance due to the cylindrical geometry of the modes and due to absorptions in the Si. Figure 4.3 (b) shows the effective index versus distance from the top for funnel/tapered shaped nanoholes with a diameter of 1,500 nm at the top, a lattice periodicity of 2,000 nm and a tapered angle of 66°. Funnel-shaped holes provide better coupling into the lateral modes than the cylindrical holes, which results in smaller reflection. The photodiodes were then simulated numerically using FDTD to examine and maximize the optical absorption for the wavelength range 800–900 nm for the following diameters and periods (d/p): 1,300/2,000 nm, 1,500/ 2,000 nm, 700/1,000 nm and 630/900 nm. Most of the field intensity is trapped in the slab, and one can calculate the trapped photons in the photodiodes by subtracting the reflected (R) and transmitted (T) components from the total intensity. The results of the FDTD numerical simulations are shown in Fig. 4.3 (c) for a hexagonal lattice funnel-shaped holes (d/p: 1,300/ 2,000 nm and 700/1,000 nm) with different sidewall angles (75°, 66°, −75°) in a 2-μm-thin Si depletion region. The simulation results suggest that a positive sidewall angle has a better optical absorption efficiency over a negative sidewall angle where the bottom diameter is larger than the top diameter of the nanoholes. The FDTD simulation results show that photodiodes with tapered holes confine light more efficiently than photodiodes with cylindrical holes as can be shown in the inset of Fig. 4.3 (c).

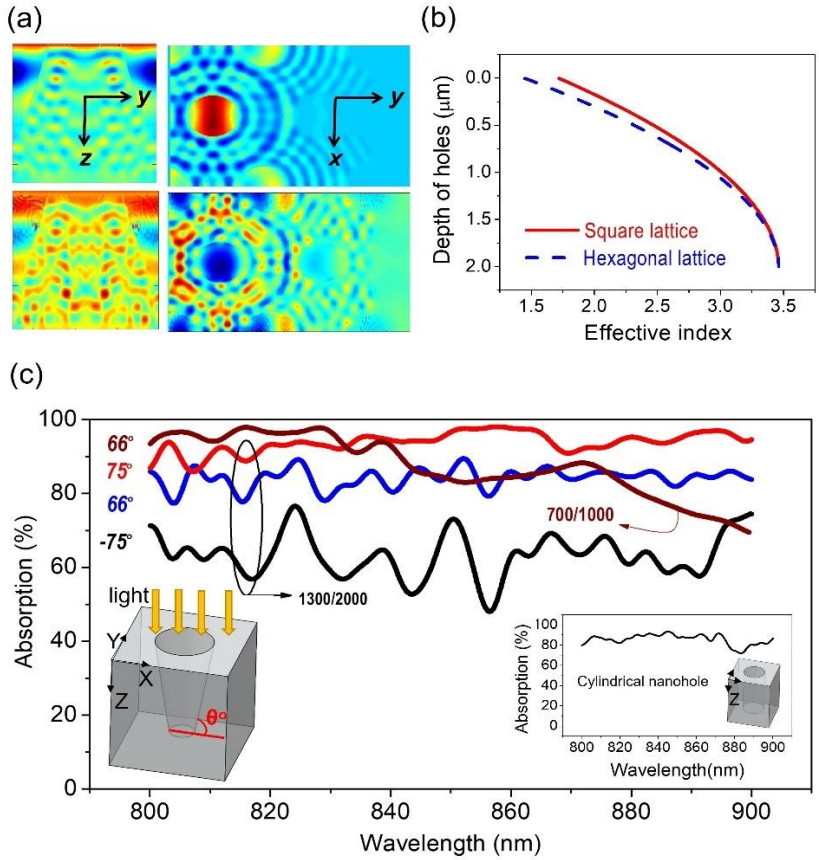


Fig. 4.3. (a) Lateral field propagation in the hexagonal tapered nanohole lattice: *y-z* plane in the left column and x-y plane in the right column. Time increases from top to bottom. For simulations, only left column of the holes was illuminated, and it depicts the lateral wave propagating from left to right. For the tapered nanoholes, the lateral modes are stronger than that of the cylindrical ones. (b) The effective refractive index vs. distance from the top for the tapered nanoholes with diameter 1500 nm at the top, lattice period 2000 nm, and tapered angle 66^{o}. The effective index profile gradually increases from the surface of the photodiodes to the bottom of the holes. (c) Absorption (*1-R-T)* in 2 μm Si integrated with tapered holes (1300 nm diameter, 2000 nm period), and ~2 μm depth of etching with angles of 75°, 66°, -75° (holes are wider at the bottom). A single absorption curve for 700 nm, 66° tapered holes with 1000 nm period is also presented. The inset shows individual components; absorption (A), reflection (R) and transmission (T) for a cylindrical hole array.

4.3 Device processing and fabrication

4.3.1 Si PIN design doping profile

The device doping profile is designed to have 2.5 μm thin Si i-layer as an absorbing layer. Si PIN and NIP structures were designed and optimized as can be seen in Fig. 4.4 (b) and (d), respectively. The doping profile was verified via SIMS measurement as can be seen in Fig 4.4. The bottom p-layer is Boron-doped (5 x 10^{20} cm^{-3}) p^{++} $Si_{0.988}Ge_{0.01}B_{0.002}$ which serves as a bottom contact layer. While the top n-layer is Phosphorous doped (~10^{20} cm^{-3}) n^{++} Si layer which serves

as a top contact layer. The highly doped p and n layers are designed to decrease the minority carrier's lifetime, minimize the diffusion of the photocarriers, and reduce the series resistance. It should be noted that, the i-layer thickness was reduced due to the dopant atoms diffusion from n^{++} and p^{++} layers into the i-layer. As a result, we only have left with ~2 µm thin Si i-layer as an absorbing layer which minimizes the transit time for electrons and holes.

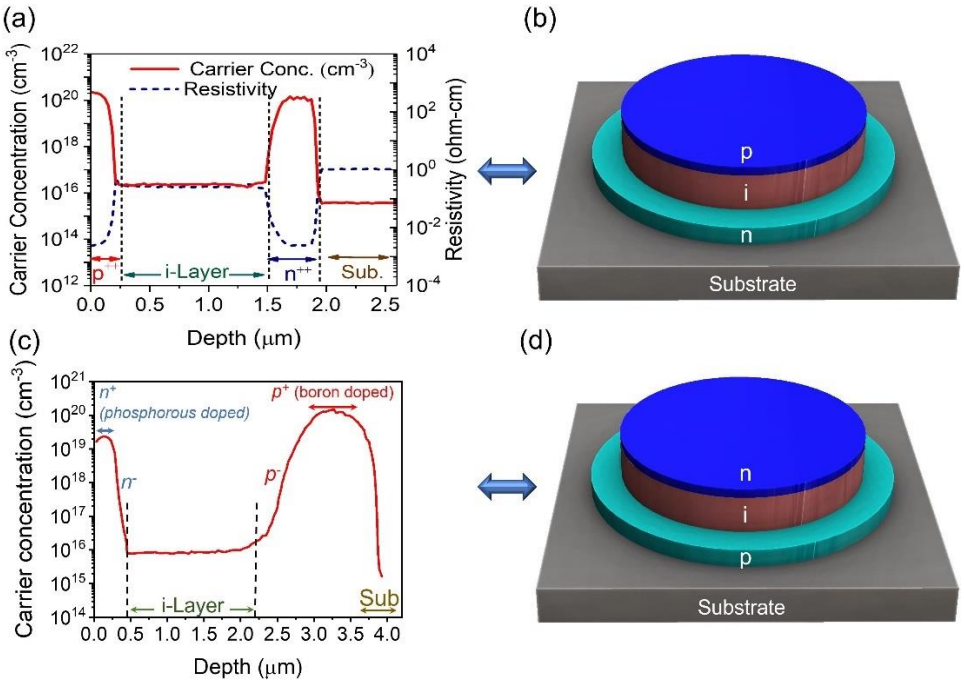


Fig. 4.4. Carrier concentration profile of the fabricated photodiode device. (a) Doping profile of fabricated PIN devices. (b) schematic of PIN device. (c) Doping profile of fabricated NIP devices. (d) schematic of NIP device.

4.3.2 Photodetector fabrication process

The fabrication processes for the photodetectors are CMOS compatible. Class 100 cleanroom facility was used during the fabrication process. The starting pin SOI wafer was pre-cleaned in piranha solution to remove any organic contaminants. Then, the wafer was spin coated with bottom anti-reflective coating (BARC) layer and deep ultraviolet (DUV) resist. BARC is used to absorb light and has a little reflection at the resist and BARC interface, thus improving the resolution of the patterned resist. Subsequently, the nanoholes pattern was generated by DUV

photolithography. It required different DUV resist coating thicknesses as well as different exposure doses for tapered and cylindrical hole fabrication, as shown in table 4.1.

Nanohole design	DUV resist coating thickness (μm)	DUV exposure dose (mJ/cm^2)	Etching method
Cylindrical	0.4	18	DRIE
Tapered	1.7	45	Two step RIE

Table 4.1 Comparison between cylindrical and tapered nanohole etching schemes.

Figure 4.5 shows the schematics of the fabrication processes of the photon-trapping photodiodes (PDs). There are two types of nanoholes (cylindrical and tapered) in the fabricated PDs, and their fabrication processes are slightly different which is explained in the following section.

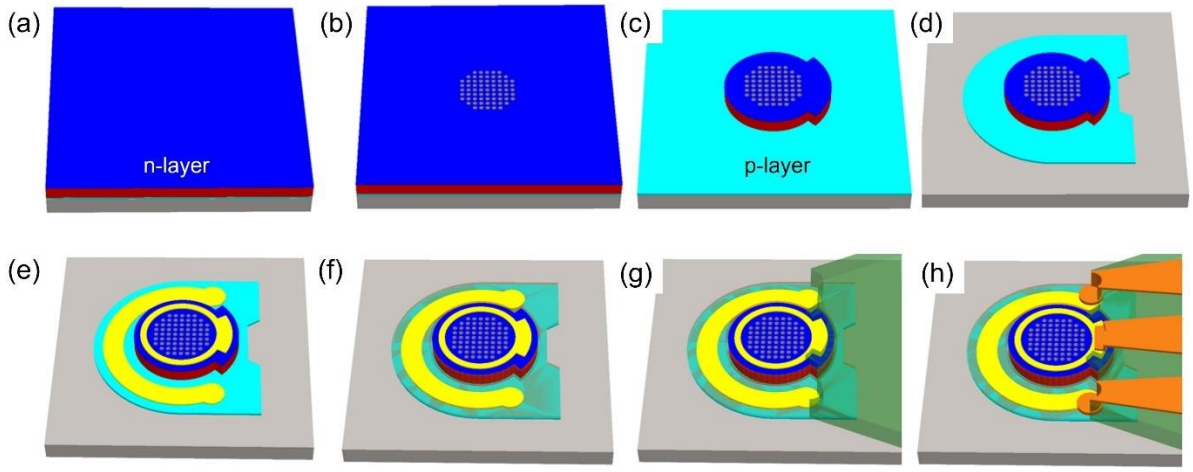


Fig. 4.5 Schematic diagram of fabricating the photon trapping PDs. (a) Starting wafer (grey: SOI wafer substrate; turquoise: p-type layer, composed of 0.2 μm of SiGeB and 0.25 μm p-Si SOI device layer; red: 2 μm i-Si layer; blue: 0.2 μm n-Si layer). (b) DUV photolithography and holes etch to create tapered or cylindrical holes with diameters ranging from 600 to 1500 nm in a square or hexagonal lattice. (c) N-mesa etches to p-Si layer. (d) P-mesa etches to the substrate layer. (e) Ohmic metal deposition (100 nm Al, 20 nm Pt) followed by HF dip passivation. (f) Sandwiched insulation layer (150 nm Si_3N_4/300 nm SiO_2/150 nm Si_3N_4) PECVD deposition to isolate the n and p mesas. (Semitransparent brownish layer represents this insulation layer on both n-mesa sidewall and top surface of p-mesa with contacts opening). (g) Polyimide planarization (semitransparent green color). (h) Coplanar waveguides (CPWs) metal deposition (brown color).

4.3.3 Photon trapping nanoholes fabrication process

After optimizing the photon trapping structures in FDTD simulations, nanoholes with different diameters and periodicity are implemented in the photodetectors accordingly. The Si PIN wafer

was precleaned in a piranha solution to remove any organic residue. For the invented nanoholes only, a 100 nm of PECVD Silicon nitride (Si_3N_4) thin film was coated on the wafer at 250 °C for KOH etched holes. Once the nanoholes were patterned, the wafer was put inside an oven at 120°C to hard bake the DUV resist. Reactive Ion Etch (RIE) or Deep Reactive Ion Etch (DRIE) were used to forming tapered or cylindrical holes, respectively. Nanoholes fabrication process for the cylindrical, funnel/tapered, and inverted pyramids are outlined below.

4.3.3.1 Cylindrical nanoholes fabrication process

DRIE is a highly anisotropic etch process used to create high aspect ratio vertical holes, and it utilizes Bosch process which alternates between two modes to achieve holes with almost 90º anisotropic etching [10]. One mode is isotropic etching of Si by sulfur hexafluoride (SF_6) gas, and the other mode is passivation/deposition by octafluorocyclobutane (C_4F_8) gas to protect the sidewalls. The schematics and actual SEM images of the cylindrical etched holes by DRIE are shown in Fig. 4.6 (a) and (b), respectively. The scalloping caused by the switching cycles of DRIE process was minimized to be less than 35 nm to achieve smooth surfaces of the sidewalls as can be seen in Fig. 4.6.

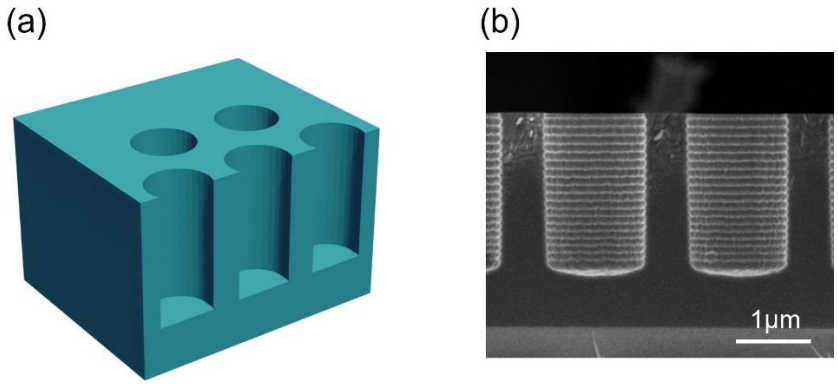


Fig. 4.6. Cylindrical holes etched in the active region of the PDs. (a) Schematic diagram of the cylindrical holes. (b) SEM image of cross-sectional cylindrical holes etched by DRIE.

4.3.3.2 Funnel/tapered nanoholes fabrication process

Funnel/tapered nanoholes with 50º-80º can be produced by adjusting the isotropic etching and deposition cycles or simultaneously employing the SF_6 and C_4F_8 gases with the right ratio [11-

13]. However, the isotropic etch nature of the SF_6 gas in DRIE process results in an almost identical lateral etch rate as vertical etch rate and thus produces large undercut beneath the photoresist [14]. Since the spacing between the holes in our PDs is very small, ranging from 270 to 700 nm, it is not sufficient enough to create tapered etched holes with microns deep by DRIE method. Therefore, RIE process was employed to etch a gradual funnel profile holes. In our RIE etching system, HBr and Cl_2 gases were used to etch Si, and it normally produces almost vertical holes with an angle of 83^o-87^o. To create tapered sidewall profile, one can start with a near vertical hole etch and then convert it into a tapered one after an additional maskless etching step that eroded the silicon structure laterally while etching along the vertical direction [14]. However, the maskless etch step can also remove very thin top n-layer in our PDs. We employed a similar etch scheme as maskless etch to create tapered holes, but with pyramid-shaped islands resist profile. Figure. 4.7 shows the schematics of the tapered holes in the fabricated PD device. Due to the high density of the holes in our PD device, the photoresist between the holes is consumed faster than bulk photoresist during the RIE process. As Fig 4.7 (b) shows, the photoresist (blue color) in the spacing of the holes formed pyramid-shaped islands (~250 nm thick) when the bulk resist remains around 400 nm thick. These pyramid-shaped islands enable the lateral etch of the holes and formed a widened opening at the top session with 60^o-70^o sidewall while the sidewall still keeps a nearly vertical profile at 84^o at the bottom. To achieve this tapered structure by this etch process, the DUV resist thickness has to be precisely controlled around 1.7 µm, so that the bulk resist was consumed around 400 nm when the holes were close to their desired etch depth.

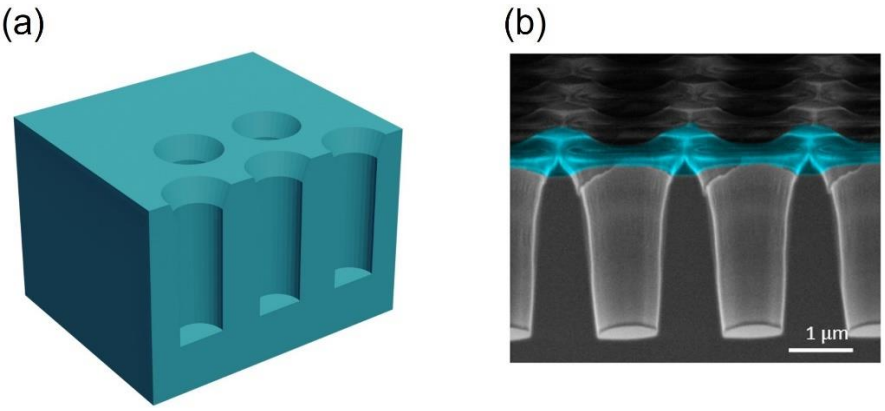


Fig. 4.7. Funnel/tapered holes in PD device. (a) Schematic of the tapered holes. (b) SEM image of the cross-section of the tapered holes by two step RIE etch.

4.3.3.3 Inverted pyramid nanoholes fabrication process

In this process, a 100 nm of silicon nitride (Si_3N_4) layer was grown on Si wafer by Plasma Enhanced Chemical Deposition (PECVD). The thin layer of Si_3N_4 is serves as a hard mask on the Si wafer. After patterning the hard mask, it was etched by DRIE to form the holes. Next, the wafer was immersed in 24% KOH solution for 2 min at 65 °C. KOH anisotropic wet etch can produce inverted pyramid-profile structures with a fixed sidewall angle of 54.7° in the (1 0 0) silicon wafer. The intersection of the (1 1 1) plane results in a self-limiting etch and hence the depths of the different holes are determined by the diameter of the opening hole in Si_3N_4. Furthermore, due to the etch rate difference in (1 0 0), (1 1 0), and (1 1 1) planes, the KOH wet etch creates undercut beneath the silicon nitride mask and forms square inverted pyramid-shaped holes as can be seen in Fig. 4.8 (b) which shows the hard mask pattern is circular.

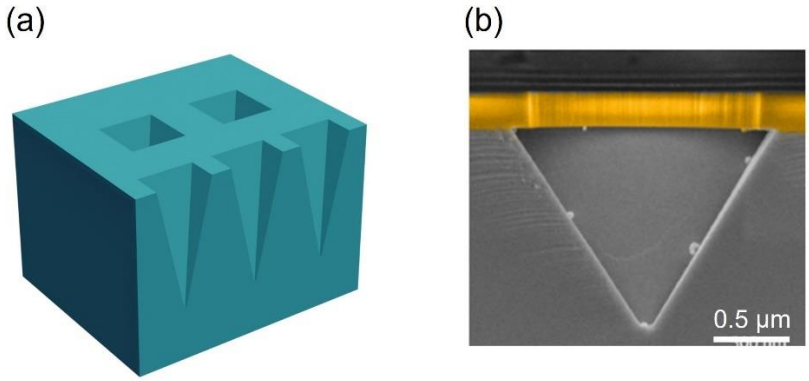


Fig. 4.8. Inverted holes in PD device. (a) Schematic of the inverted pyramid holes with sidewall angle of 54.7° by wet KOH etch with 300 nm patterned PECVD silicon nitride hard mask (brown color). (b) SEM image of the cross-section of the inverted pyramid hole.

4.3.4 Contacts formation

To ensure minimum contact resistance between the metal and semiconductor junction, ohmic contacts need to be formed. A 2 μm wide ring around the active region (with holes) and 5 μm wide half ring were patterned on n-mesa and p-mesa, respectively, using S1813 g-line resist photolithography. Then, O_2 plasma was used to clean the Si surface as well as to descum the resist on the sidewall. Another BOE (1:6) dip ensures the native oxide on Si surface is removed upon metal deposition. 100 nm of aluminum (Al) and 20 nm of platinum (Pt) were sputtered accordingly on the whole wafer. Pt was used to protect the Al film during HF dipping for surface passivation purposes. A standard lift-off process was then applied to remove the resist and form the contact patterns. Last, the sample was annealed at 465°C for 20 s in 20:1 N_2:H_2 environment for a rapid thermal process (RTP) to form the ohmic contacts. Figure 4.5 shows the fabrication steps.

4.3.5 Insulating layer deposition

A sandwiched insulating layer, composed of 150 nm Si_3N_4/300 nm SiO_2/150 nm Si_3N_4, was deposited by plasma enhanced chemical vapor deposition (PECVD) at 250°C and was subsequently patterned to open the ohmic contact regions to avoid the short between n and p mesas. The sandwiched layer was used to minimize the pinholes that may exist in a single oxide or nitride layer to enhance the insulating performance. A 3-μm-thick photo-curable polyimide layer was then deposited for surface planarization, Fig. 4.5 (g). The polyimide layer also serves as a dielectric layer to isolate the n and p mesas during the subsequent CPW metal deposition in addition to the sandwiched insulating layer. In addition, the polyimide layer reduces the parasitic capacitance arising from the large metal pads which could limit the response speed of the PD device. After patterning, polyimide film was cured at 350°C for 30 minutes under N_2 environment

in a vacuum oven. After thermal curing, the adhesion of the polyimide film to Si surface was tested with magic tape test.

4.3.6 Coplanar waveguide (CPW) deposition

Similar to ohmic contacts process, coplanar waveguides (CPWs) were then patterned, and Ti/Al/Pt (5/300/20 nm) stack was DC sputtered, followed by a lift off process as can be seen in Fig. 4.5 (h). Titanium Ti serves as an adhesion layer to the top Pt surface of the ohmic contacts.

4.3.7 Photon trapping structures designs variations

Photon trapping structures were studied and optimized through intensive simulations according to many factors, such as nanoholes diameter, periods, depth, unit cell orientation, materials thickness, materials layers (beneath the substrate/top of the substrate), and nanoholes shapes profile. The nanoholes are oriented in a hexagonal or square lattice cell as can be seen in Fig. 4.9.

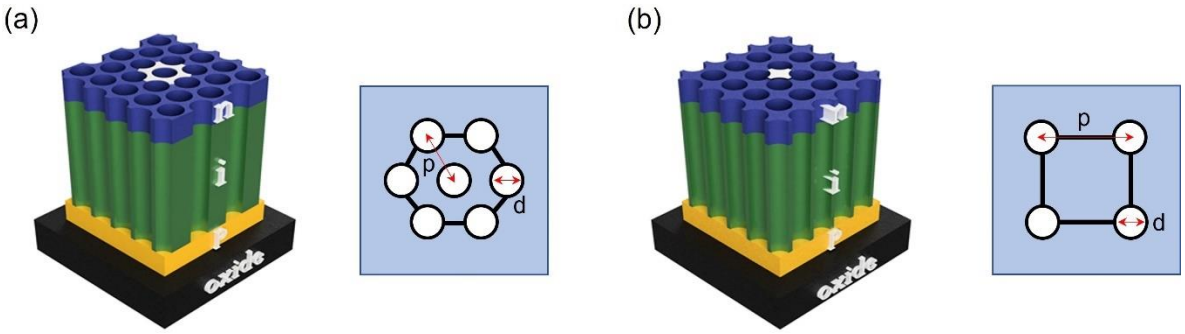


Fig. 4.9. Photon trapping structures orientation, d represents hole diameter and p represents hole period. (a) Hexagonal lattice, and hexagonal unit cell. (b) Square lattice, and square unit cell.

To evaluate and examine the simulation results, many designed of nanoholes were fabricated accordingly. A variation of different diameters (d) that varies between 630 nm to 1500 nm and periods (p) that varies between 900 nm to 3000 nm were experimentally demonstrated. The dimensions and parameters of the photon trapping structures were chosen to be optimized according to the desired wavelength. The periodic spacing between structures is reduced in each set of devices by keeping the d fixed, allowing to increase the number of nanoholes that can be accommodated on the surface of PD. The depth of the nanoholes was etched to be around 2 μm

for funnel shape, while it varies between 450 to 1000 nm for inverted pyramids. Also, unpatterned device is fabricated as a reference which we define a control device to compare with the PT PDs. The devices are fabricated on bulk silicon or silicon on-insulator (SOI) wafers also for comparison as can be depicted in Fig. 4.10.

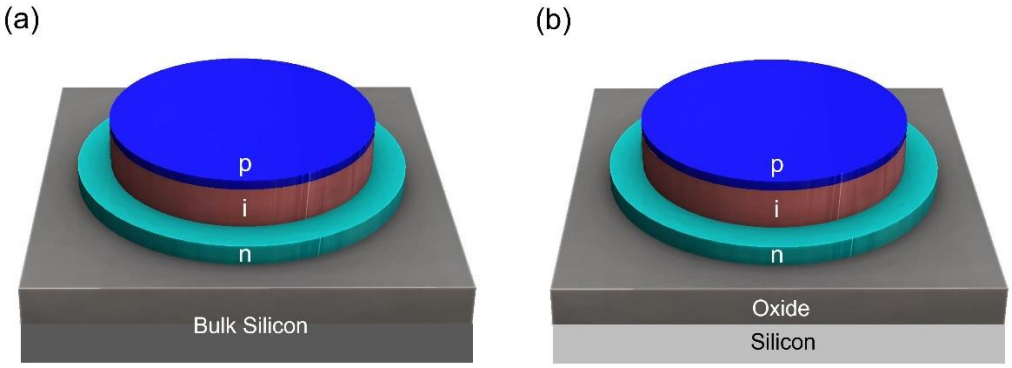


Fig. 4.10. Types of Si wafer substrates. (a) Schematic of bulk silicon. (b) Schematic of silicon on insulator (SOI).

Different diameters of photodetectors (D) were fabricated in this work ranging from 30 µm to 500 µm. Such variation allows us to study the effect of capacitance and EQE as a different number of holes can be accommodated on the surface of the PD. Figure 4.11. shows SEM images for (D) 30 µm, 50 µm, and 80 µm diameter photodetectors.

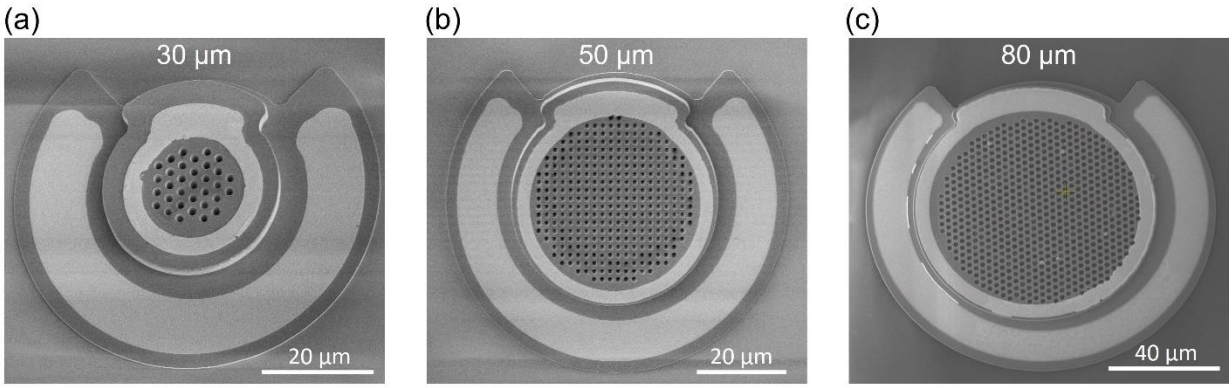


Fig. 4.11. SEM images of the fabricated photodetectors. (a) 30 µm diameter PD, (b) 50 µm diameter PD, and (c) 80 µm diameter PD

The following table 4.2. shows the variations of the structures, profile, substrate types, and photodetectors diameters that were investigated experimentally.

Specification	Variation
Wafer substrate	Bulk silicon/ silicon on insulator (SOI)
Photon trapping - Nanoholes diameter (d)	630 nm-1500 nm
Photon trapping - Nanoholes periodicity (p)	900 nm-3000 nm
Photon trapping - Nanoholes etching profile	Cylindrical, Funnel/tapered, Inverted pyramid
Photon trapping - Nanoholes lattice orientation	Square, Hexagonal
Photodetector diameter (D)	30, 40, 50, 80, 100, 250, 500 µm

Table. 4.2. Photon-trapping PDs design specifications and variations.

The nanoholes are etched on the surface of the photodetector at different depths. As aforementioned etching profiles are cylindrical, funnel/tapered shape, and inverted pyramids. These structures are arranged in a square or hexagonal lattice. The etching profile and dimensions accuracy are verified by the top and cross-section views of Scanning Electron Microscopy (SEM) as can be depicted in Fig. 4.12.

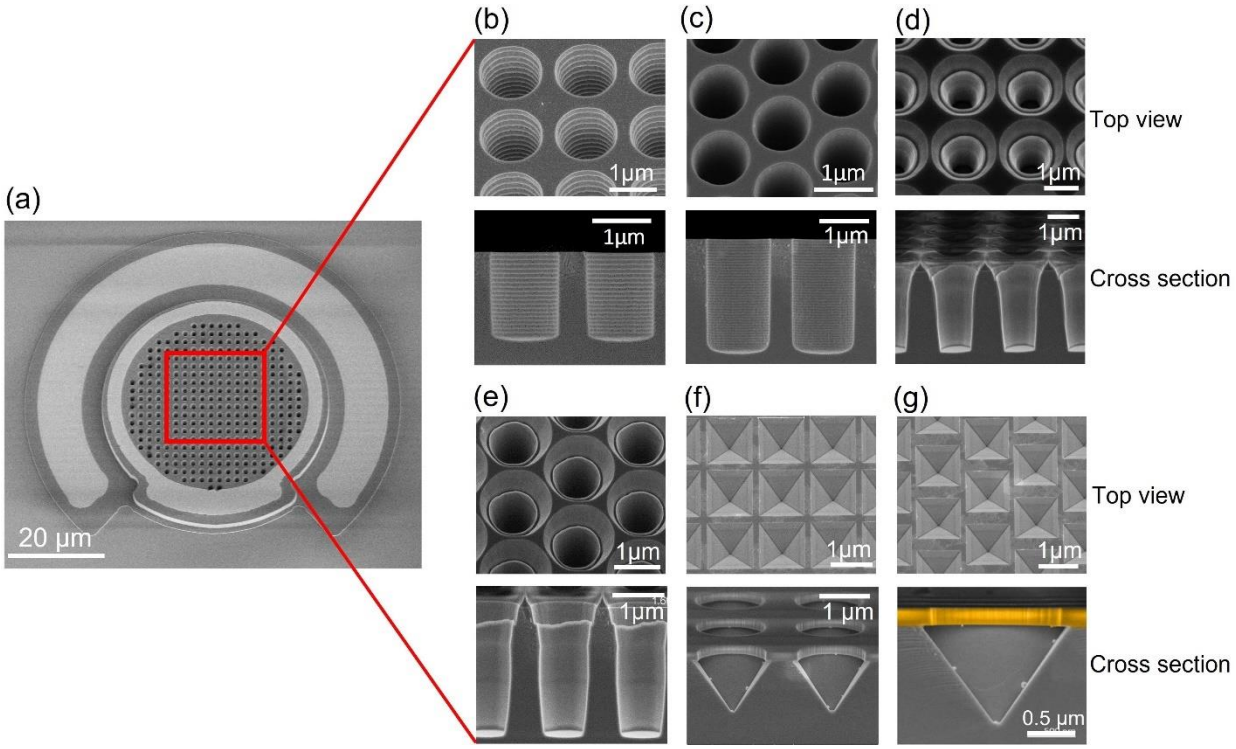


Fig. 4.12. SEM Top and cross-section view of the nanohole array etched in Silicon PD. The images describe a complete PD (a), and the different profiles fabricated as photon trapping nanoholes including:

(b) cylindrical square lattice, (c) cylindrical hexagonal lattice, (d) funnel-shape square lattice, (e) funnel-shape hexagonal lattice, (f) inverted pyramid square lattice, and (g) inverted pyramid hexagonal lattice.

4.4 Results and Discussion

4.4.1 Dark current and surface passivation treatment

Si photodetectors with photon trapping structures fabrication produces many surface defects. These defects produce vacancies, interstitials, dislocations, stacking faults, surface roughness, and impurities formed by surface damage during top-down etching cause low shunt resistance and high leakage/dark current which dramatically affect the performance/sensitivity of electronic and optoelectronic devices. As a key factor in achieving highly efficient silicon-based devices, electrical losses at the surfaces should be minimize. For this reason, effective passivation of the surface is required to eliminate the electrical losses. Surface states passivation can be chemical, in order to reduce the density of surface states by terminating dangling bonds, or can be field effect-based, by applying a built-in electric field in order to drive one of the carrier types away from the surface states. Figure 4.13 provides a summary of three different efficient passivation techniques for the Si optoelectronics with photon trapping nanoholes, more details can be found in chapter 3. Each technique has its advantages and disadvantages, and their tradeoffs need to be analyzed very carefully to acquire the best technique for cost and time effective processes. The results show that HF passivation effectively reduces the leakage/dark current in Si PDs integrated with nanoholes more than four orders of magnitude. Thin oxide layer passivation utilized in this study also demonstrates a protection of the device surfaces from minority carriers' recombination by electric field effect. On the other hand, LIEE, shows its compatibility and applicability for RIE system as its efficiency to remove damaged c-Si layer form the surfaces.

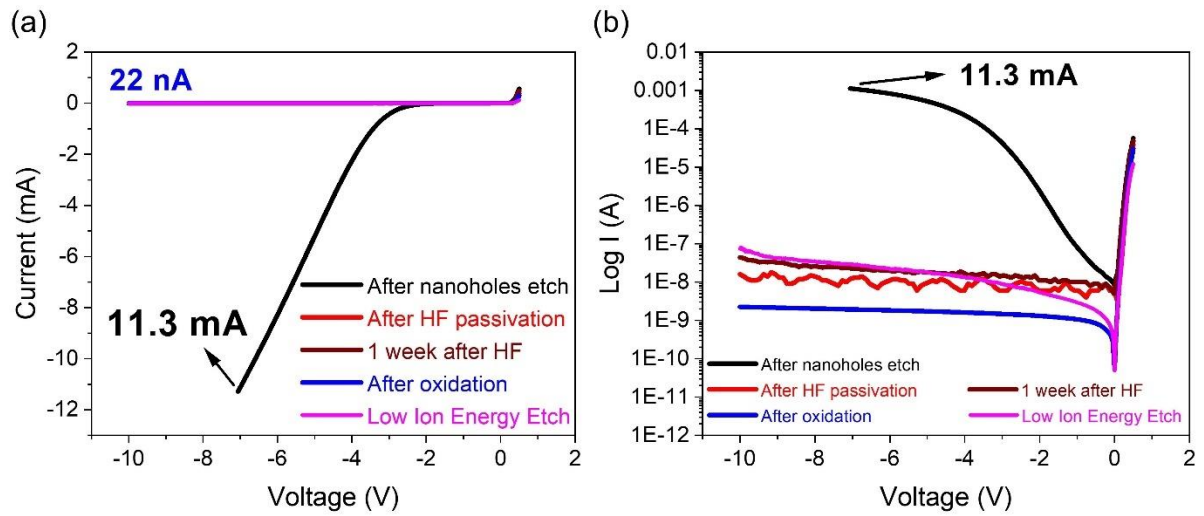


Fig. 4.13. A variation of passivation processes applied for reducing leakage current. (a) Leakage current before and after hydrogen passivation, oxidation, oxide removal and low ion energy etch (linear scale). (b) Logarithmic scale.

4.4.2 External Quantum Efficiency (EQE)

The External Quantum Efficiency (EQE) defined as the ratio of the number of charge carriers obtained to the number of incident photons, is a key parameter that describes the sensitivity of photodetector. This parameter is measured in our photon trapping Silicon PDs using a super continuum laser delivering the NIR light to the photodetector with a single mode fiber. To compare our results, the pin PD control (with no patterned nanoholes) is also measured as a reference.

4.4.2.1 EQE enhancement with respect to the number of photon trapping structures

To study the efficacy of implementing nanoholes in photodetectors and evaluate their impacts on the PDs EQE, a set of PDs have been fabricated with a constant surface diameter of 50 µm. Subsequently, as SEM images of Fig 4.13 (b) shows, we have gradually incremented the number of photon-trapping structures, starting with only 1 nanohole up to 820 nanoholes. Each of these photon trapping structures has a fixed diameter of 700 nm and a period of 1000 nm. Figure. 4.13 (a), shows the gradual increase in EQE from 12% in PD with only one nanoholes to more than 38% as the number of nanoholes increased to 820. The increase of the number of nanostructures, enhance the lateral propagation of light and reduce the flat area where light is loss due to

transmission, both effects contribute the enhancement of EQE in PDs. Consequently, the overall EQE of the PT devices is distinctly increased in comparison to the control device.

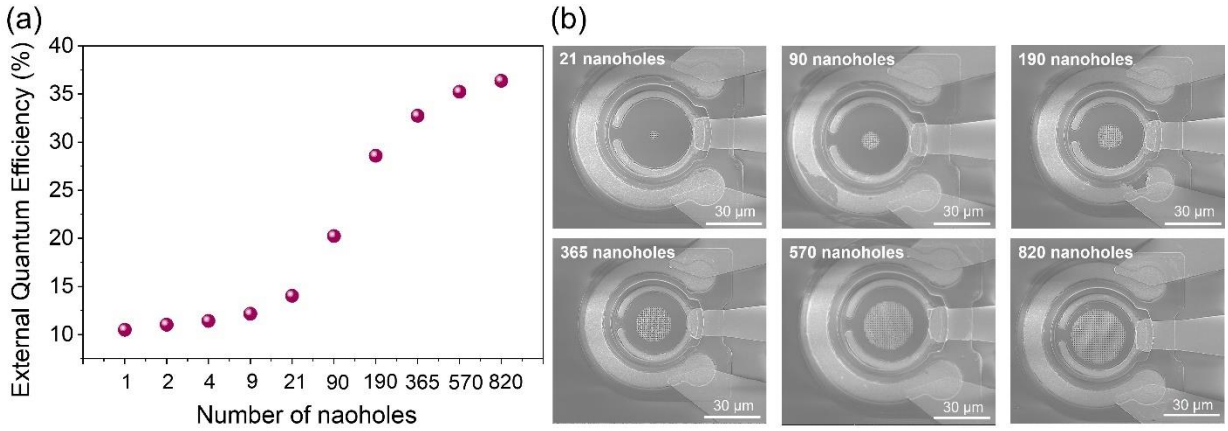


Fig 4.14. (a) EQE versus number of nanoholes. (b) SEM images of Si PDs with increasing number of nanoholes in 50 µm diameter PDs.

4.4.2.2 EQE compassion for the Si PDs integrated with photon trapping structures fabricated on Si-bulk wafer and Si-SOI wafer

As can be seen in Fig. 4.10, Si PIN PDs were fabricated on two different substrates. The first substrate is Si on bulk silicon, whereas the second substrate is Si on SOI (silicon on insulator). Figure 4.15. shows EQE characteristics of the fabricated PDs on bulk-si and SOI-si. The photon trapping PDs fabricated on a bulk Si wafer exhibit the EQEs between 15% and 32% at 900 nm and 800 nm, respectively. However, compared with the control and photon trapping PDs fabricated on bulk Si, the EQEs of photon trapping PDs on SOI substrate distinctly increased, resulting in a higher EQE ranging between 30% and 48% at 900 nm and 800 nm, respectively. To be consistent in the comparison, same structures were defined in both substrates PDs such as hexagonal unit cell, cylindrical nanoholes, nanoholes diameter (d) and nanoholes periodicity (p). These experimental results show that PDs build on a SOI platform are benefited by the existence of buried oxide under the device layer which acts as a semi-reflecting mirror as it further promotes the lateral propagation of the light modes.

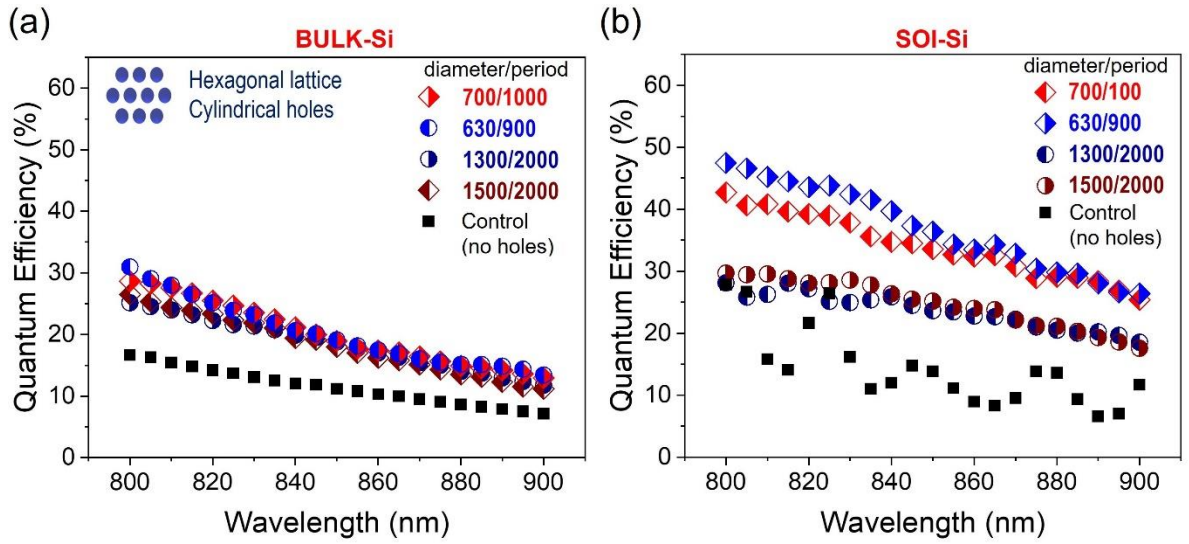


Fig 4.15. EQE comparison for bulk-Si and SOI-Si substrates with 2 µm absorbing i-layer. (a) EQE in bulk-Si with cylindrical nanoholes arranged in hexagonal pattern. (b) EQE in SOI-Si with cylindrical nanoholes arranged in hexagonal pattern.

4.4.3 Optical and Electrical Characterization for wavelengths (800-900 nm)

The simulation results (black and blue curves at the top) in Fig 4.15 (a) show that PDs with holes have an absorbing *i*-Si layer thickness between 1.1 to 1.3 µm, although the design thickness was 2 µm. Almost 6 to 10 times increased absorption and resultant EQE were observed for a wide spectral range compared to bulk Si with similar *i*-layer thickness. In the simulations, it is assumed that carrier generation mostly takes place in the *i*-layer along with a small fraction of carriers that get collected by the PD from the *n* and *p* contact layers. The inset shows the schematics of dopants diffusion from *p*-layer to *i*-layer, reducing the thickness of *i*-layer, and resulting in a reduced photon absorption. The discrepancy between the experiment and simulation originates primarily from the boron (B) diffusion into the *i*-Si region that reduces the *i*-region by more than half in thickness, negatively impacting the collection efficiency of a large fraction of the photo-generated carriers. The results presented in Fig. 4.14 (a) for an active PD region with integrated nanoholes (d/p: 700/1000) represent an effective absorption length equivalent to more than 13 times that of the absorption possible in bulk Si. In other words, at λ=850 nm, one needs more than 13 times thicker *i*-Si region to achieve the same magnitude of absorption with a flat Si thin film compared to Si film of same thickness that has integrated absorption enhancement

nanostructures. Such enhancement of absorption enabled by the integrated holes contributes to EQEs above 60 % [Fig. 4.14 (a)] at 800 nm. At the datacom wavelength (λ=850 nm), a Si PD with a flat surface designed with an i-layer thickness of 1.1 µm, will exhibit a EQE of only ~6 %, assuming all photons are impinged on the i-layer and a perfect anti-reflection coating is employed. In contrast, PDs with integrated nanoholes exhibited >52 % EQE at 850 nm in our experiments. Similar significant enhancement, close to an order of magnitude higher EQE, was observed in a wide spectral range from 800 to 900nm, as shown in Fig. 4.15 (a).

In order to accurately estimate the potential EQE for a PD with 2 µm *i*-layer thickness, the simulated EQE of the *pin* structure was corrected to a reduced value by subtracting the contributions of the lateral modes that are trapped and absorbed in the *n* and *p* regions of the PD structures. Most of the photo-carriers generated in such doped regions don't experience a drift field and, thus, don't contribute to the photocurrent. Figure 4.15(b) shows simulated EQEs for tapered holes of varying d/p illuminated with light at 850 nm wavelength. For comparison, measured QEs from PDs with integrated nanoholes and corresponding dimensions are also presented. The figure shows the difference between currently measured EQEs and potentially achievable EQEs with 2 µm of *i*-layer and abrupt *p-i* and *i-n* interfaces.

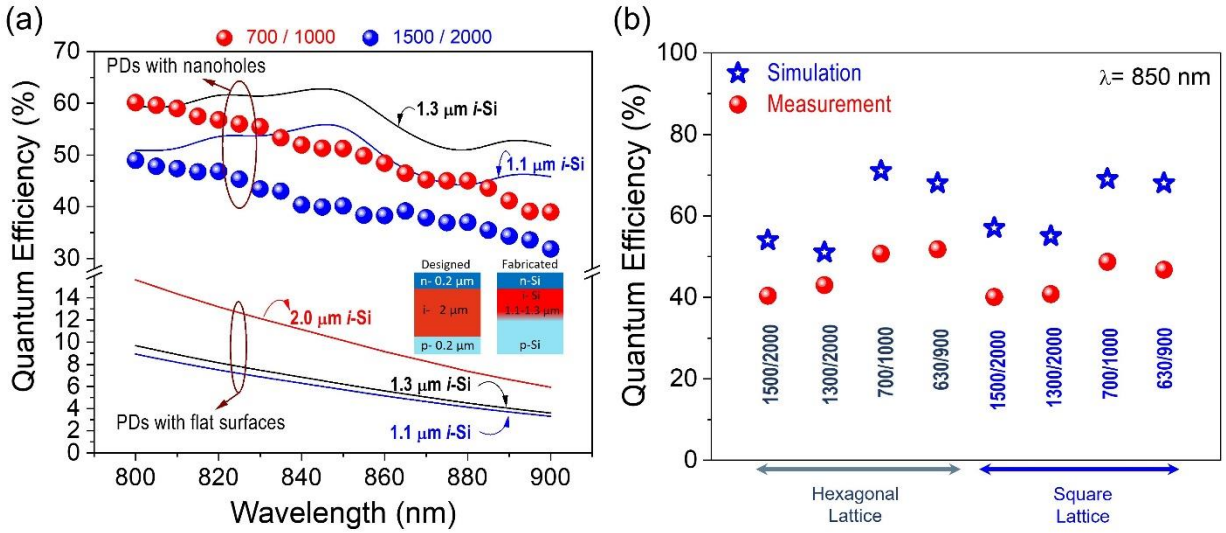
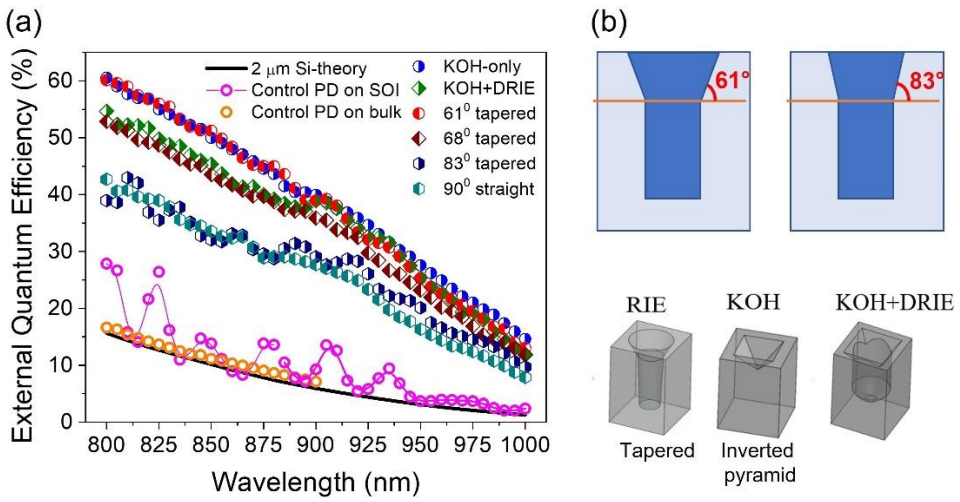


Fig. 4.16. Enhanced quantum efficiency enabled by integrated nanoholes. (a) The line represents the simulation data, and the symbols represent the experimental results. (b) Measured results vs. simulation results for 850 nm incident wavelength.

4.4.4 Photon trapping structures' factors affecting EQE of the photodetectors in near infra-red (NIR) window wavelengths (800-1000 nm)

Figure 4.17 demonstrates the experimentally measured EQEs from photodetectors with nanoholes (diameter (d)/period (p) = 700/1000 nm) in hexagonal lattice of different sidewall angles which are labeled with different colors. The holes with 90° angle are straight holes (cylindrical holes) created by DRIE, while the RIE etched funneled holes with of 61°, 68°, and 83° were created via different DUV resist coating thickness and varying RIE time. The purple circles in Fig. 4.17 (a) represents the measured EQEs of control (no holes) PD on SOI while the orange circles represent EQEs of control PD on bulk substrate. Figure 4.17 (b) shows the schematics view of the nanoholes structures and the SEM representation can be seen in Fig. 4.18 (b). EQE measurements reveal that photodetectors with nanoholes surpass their counterparts without holes regardless of the sidewall angles. At optical data communication wavelength of 980 nm, EQEs of the holes enabled photodiode are 10−20%, while the control PD only has less than 2%. In our case, the 10 times of EQE enhancement at the wavelength of 980 nm allows the operational wavelength of all-silicon photodiode extended to such wavelength close to the silicon's band edge. In addition, it also shows that the sidewall angles of the periodic nanoholes can greatly impact the EQE of the device: the smaller the sidewall angle, the higher EQE of the PDs. This is mainly because of the reduced reflection with funneled structure which can allow more coupling of light into the i-layer. The index difference at Si−air interface can be reduced by decreasing the amount of Si material in air matrix with those funnel-shaped holes. The lower index changes at Si− air interface can help light go through the medium instead of being reflected from the surface of the structure. The holes with 61° sidewall angle show the highest EQE over the spectrum that covers 900−1000 nm. The EQEs are very similar among the three types of holes between 900 and 1000 nm, with the KOH etched holes having slightly better performance. At the wavelength of 980 nm, the EQEs of holes from KOH etch, combined KOH/DRIE and RIE are 20, 18, and 18.5%, respectively.

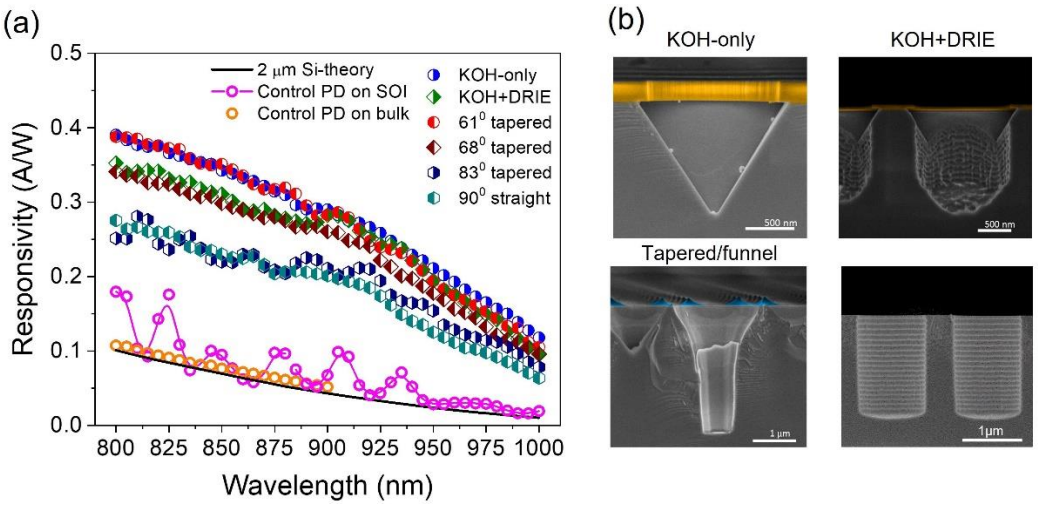


4.17. (a) EQE comparison of planar (control) Bulk-Si PD, and control SOI-Si PD vs. a variation of different photon-trapping designs fabricated on SOI-Si PDs. (b) Schematic representations of tapered holes angles and etching schemes (bottom).

It should be noted that although the geometries are quite different among these holes, the sidewall angles of the holes are similar: both KOH and combined KOH/DRIE etched holes have a fixed angle of 54.7°, while RIE etched holes have a sidewall angle of 61° at the opening. The depths of the holes for design (KOH and KOH+RIE) are quite different among these geometries: RIE etched holes have a depth of more than 2.5 μm, KOH etched holes only have depths of 500−600 nm, and combined KOH/ DRIE etched holes can reach to 800−900 nm. This indicates that, as the lateral propagating modes can be generated by the periodic holes, the depths of the holes do not seem to affect the EQEs as much as the sidewall angles do. The device responsivity can be calculated using the following Equation:

$$R = \eta * \frac{\lambda}{1.24} \left(\frac{A}{W}\right) \tag{4.1}$$

where R is responsivity, η is external quantum efficiency, and λ is the incident wavelength in μm. The PD responsivities of different holes between 900 and 1000 nm are shown in Fig. 4.18.



4.18. (a) Responsivity comparison of planar (control) Bulk-Si PD, and control SOI-Si PD vs. a variation of different photon-trapping designs fabricated on SOI-Si PDs. (b) SEM images of photon-trapping designs etching profiles.

It can be shown that the inverted holes etched by KOH have the best performance between 900 and 1000 nm. At the wavelengths of 980 and 1000 nm, the responsivities of the device with KOH etched holes are around 0.16 and 0.12 A/ W, respectively. They are almost 10-fold of the responsivities of the device without photon-trapping holes. The device responsivity values (measured at 850, 880, 910, and 940 nm) are sufficient to meet the power budget requirements of current SWDM systems[15]. The device can also be used in future SWDM systems using 980 nm as well as HPC and LIDAR systems. PDs EQEs and responsivities for 980 nm and 990 nm are summarized in table 4.2.

(a)

d/p:700/1000nm	EQE (%) @980 nm	EQE (%) @990 nm
KOH-only	19.8	17.4
KOH+DRIE	18.0	14.6
61° tapered	18.3	16.4
68° tapered	15.3	14.0
83° tapered	14.2	12.1
90° straight	11.6	10.0
Control PD on SOI	3.2	2.0
2 µm Si-theory	1.9	1.6

(b)

d/p:700/1000nm	Responsivity (A/W) @980 nm	Responsivity (A/W) @990 nm
KOH-only	0.156	0.138
KOH+DRIE	0.142	0.116
61° tapered	0.144	0.130
68° tapered	0.122	0.111
83° tapered	0.112	0.096
90° straight	0.092	0.079
Control PD on SOI	0.025	0.016
2 µm Si-theory	0.015	0.012

Table. 4.3. (a) EQE at 980 nm and 990 nm for control and photon-trapping designs Si SOI PDs. (b) Responsivity at 980 nm and 990 nm for control and photon-trapping designs Si SOI PDs.

4.4.5 Optimizing the optical absorption in photon trapping Si PD for a short-reach optical communication wavelength (λ=850 nm)

For a more in-depth analysis of how design of photon trapping structures affects the EQE on Si PDs, an input light of 850 nm wavelength (short-reach optical communication window) is injected, in photodiodes with all the design variations. As depicted in Fig. 4.19, in all the designs, keeping the hole diameter (d) fixed, and reducing the period (p), the EQE gradually increases. When photodetectors are fabricated on SOI substrate the EQE varies between 30% to 56%, while for devices on the bulk silicon substrate, the EQE only is enhanced between 15% and 25%. Our control device presents less than 15% of EQE in agreement with the theoretical value calculated for 2.5 µm-thick, silicon PD.

Comparing the etching profile of the structures, the inverted pyramid profile presents a higher enhancement compared to the inverted pyramid profile. This result can be attributed to the effectively graded refractive index profile at the air (n=1)/silicon (n=3.4) obtained by the inverted pyramid profile, providing superior antireflection with suppressed reflection over wide wavelength and angular range than traditional quarter-wavelength thin-film AR coatings [16].

Devices with a d of 1000 nm and a p of 1300 nm pronounce the highest EQE for 800nm, 850 nm, and 900 nm wavelength. This confirms that a high EQE can be attained for a relatively large d/p. In particular, the maximum efficiencies at the wavelengths of 800, 850, and 900 nm are measured as 58%, 56%, and 45%, respectively, for the photon-trapping PDs with $d/p \approx 0.77$. The enhanced absorption coefficients at wavelengths, $\lambda = 800$, 850, and 900 nm are calculated to be 4335.5, 4104.9, and 2989.2 cm^{-1} by assuming 2 µm of Si i-layer thickness, whereas the absorption coefficients for bulk Si at those λ points are 850, 535, and 306 cm^{-1}, respectively. Hence, a maximum of about >10x higher absorption enhancement is attained at some of the incident wavelengths by integrating inverted pyramids or funnel-shaped nanoholes in the PDs fabricated

on SOI substrates. Finite Differential Time Domain (FDTD) method is used to calculate the absorption, and consequently the EQE, of a silicon PD on SOI substrate with inverted pyramid shape structures, with the different diameters and periodic distances, previously presented. In this simulation, a plane wave with a wavelength of 850nm is normal incident to the surface of the photodetector. Periodic Boundaries Conditions (PBC) are set laterally between unit cells and Perfect Match Layer (PML) boundary conditions are set at the top and bottom of the Silicon photodetector. The absorption is obtained from the subtraction of the transmission and the reflection as A=1-T-R. Based on the analytical approach, it has been shown that more than 70% of EQE can be obtained by the designed photon trapping Si PDs, by increasing the number of periods of trapping structures and reaching the infinite periodic boundary condition. As the periodicity of the nanoholes is reduced, an enhancement in EQE is achieved for a broadband wavelength as can be seen in Fig 4.15.

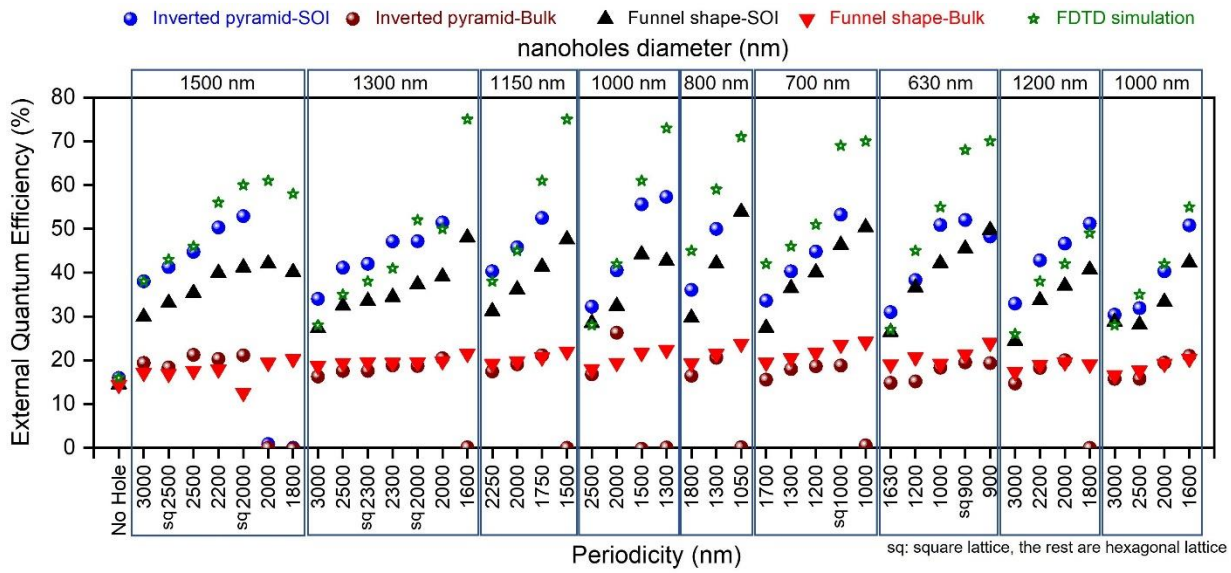


Fig. 4.19. Measured EQE of fabricated Si PDs vs. a variation of nanoholes PT designs at 850 nm wavelength. FDTD simulation for funnel design nanohole is included (green star).

4.4.6 Electrical characterization results for the optimized photon trapping structure near infra-red (NIR) window wavelengths (800-1100 nm)

Si photodetectors can be utilized for many applications that works in NIR regime (800-1100 nm). Fig 4.20 (a) presents the EQE of PDs designed with inverted pyramids with a hexagonal

nanoholes unit cell formation [Fig 4.12 (g)]. The nanoholes diameters were fixed to be 1000 nm where the nanoholes periodicity were varied between 1300 nm to 2500 nm. Overall, the range of wavelengths studied, the decrease in period have resulted in a higher EQE. The maximum efficiencies at wavelengths of 800, 850, and 900 nm are measured as 58%, 56%, and 45%, respectively for the photodetectors that designed with nanoholes diameter (d) of 1000 nm, and periodicity (p) of 1300 which corresponds to a ratio of d/p ≈ 0.77. The enhanced absorption coefficients at wavelengths, λ= 800, 850, and 900 nm are calculated to be 4335.5, 4104.9, and 2989.2 cm^{-1} by assuming 2 µm of Si i-layer thickness, whereas the absorption coefficients for bulk Si at those wavelengths are 850, 535, and 306 cm^{-1}, respectively. Therefore, around 10x higher absorption enhancement is achieved at some of the incident wavelengths by integrating inverted pyramids or funnel shape nanoholes in the PDs fabricated on SOI substrates as can be seen in Fig. 4.20 (b). The absorption enhancement attributed to the nanoholes photon trapping structures and the SiO_2 layer of the SOI substrate which acts as a semi-reflecting mirror due to the high refractive index difference between Si and SiO_2, resulting in an enhanced reflection and consequently a higher absorption in the i-layer of the PDs.

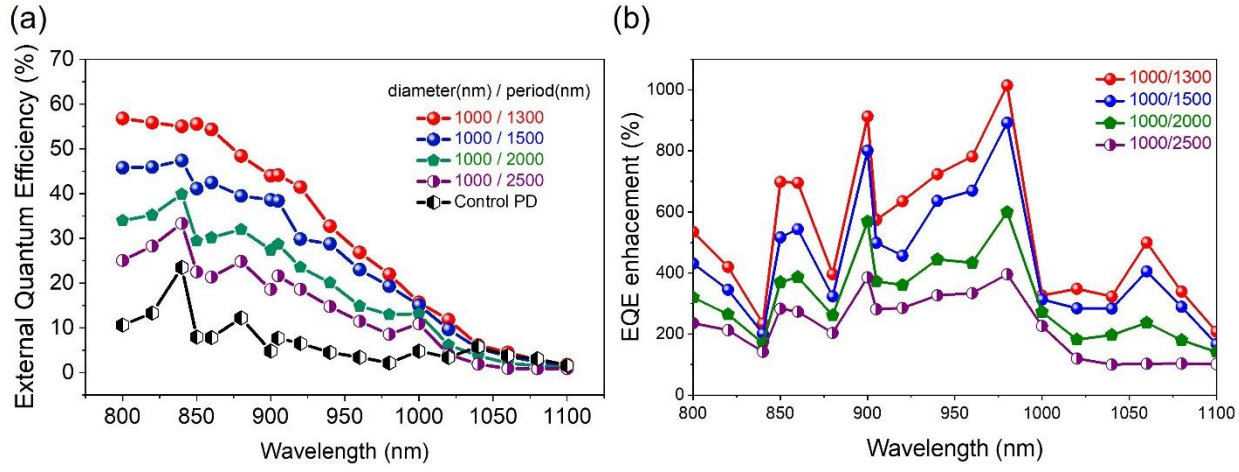


Fig.4.20. Measured EQE enhancement in the photon trapping Si PDs. (a) Broadband wavelengths for the NIR applications (800-1100 nm) vs. control (planar) PD. (b) EQE enhancement factors that surpassed 10x at 960 nm.

4.4.7 Enhancing optical absorption efficiency in Si PIN photon trapping photodetectors.

Utilizing the Bouguer-Beer-Lambert law and considering surface reflection losses [17], an effective absorption coefficient (α_{eff}), defined in Equation (4.2), is estimated to quantify the enhancement in photon absorption of the fabricated devices with photon-trapping structures.

$$\alpha_{eff}(\lambda) = -\frac{1}{d_{Si}}\left[\ln\left(\frac{1-QE_{meas}(\lambda)}{1-R_{reflection}(\lambda)}\right)\right] \quad (4.2)$$

Where d_{Si} is the thickness of the Si active layer of the photosensor, and QE_{meas}, and R_{meas} are the experimentally measured quantum efficiency and surface reflection of the devices respectively. A comparison of Si PIN photon trapping-based photodetector with typical bulk silicon ($\alpha_{silicon}$) and III-V GaAs (α_{GaAs}), a material that is currently used in the industry due to its direct bandgap and high mobility of its carriers can be depicted in Fig. 4.21. The α_{Si} value is 535cm^{-1} for the bulk Si, however, photon trapping structures enhances Si effective absorption to be α_{eff}=4100cm^{-1} , that is approximately an 8-fold improvement. The enhancement of absorption overpass GaAs at wavelengths beyond 900 nm, opens the possibility to develop receivers based on silicon instead of using GaAs, the current dominant material.

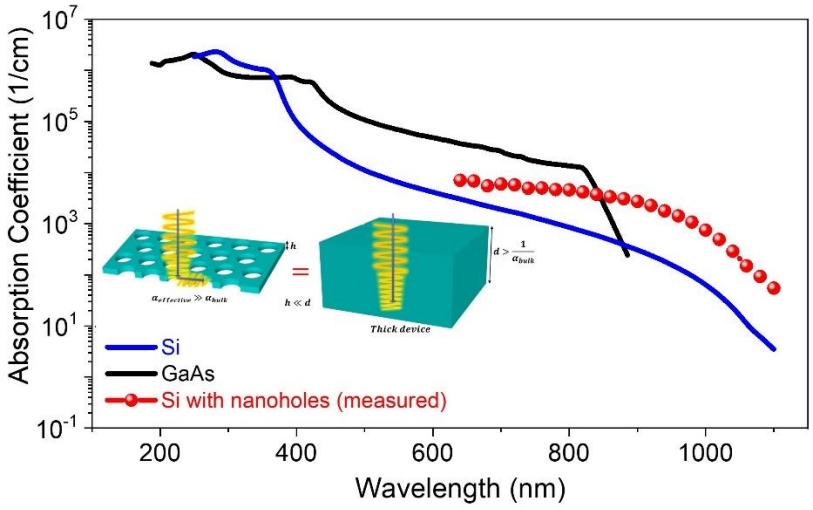


Fig.4.21. Experimental demonstration of absorption enhancement in Si and comparison with bulk silicon and GaAs.

4.4.8 Utilizing photon trapping structures for capacitance reduction and ultra-fast Si PDs operation

The 3dB bandwidth in pin photodetectors is mainly depended on two parameters: the carrier transit time (tr) and the RC constant-time [18]. By considering the pin PD as a parallel plate, the capacitance can be written as $C=\varepsilon_o\varepsilon_r A/w$, where ε_o and ε_r are the permittivity of vacuum (8.84 x 10-12 F/m) and silicon (11.68), respectively; w is the depletion layer width, typically the intrinsic-layer, and A is the junction area. The use of a thin i-layer reduces the transit time but increases the junction capacitance in the flat devices. Yet, the introduction of an array of nanoholes assists leads to the reduction of active cross-section area and materials of the PD. Consequently, the overall junction capacitance of the PD is assumed to be reduced. This reduction in the junction capacitance due to the presence of the photon trapping nanoholes can be taken into consideration to write the following modified expression of f_{3dB} as can be shown in Equation 4.3.

$$f_{3dB} = \frac{1}{\sqrt{[2\pi R \times C\ (1-ff)]^2+[t_r/0.44]^2}} \tag{4.3}$$

As t_r is the transit time required for the generated carriers to reach the electrode at saturation velocity, R is the resistance, typically assumed as 50 Ω, C is the capacitance, dominated by junction capacitance and ff is the filling fraction of the nanohole array.

Hence the integrated nanoholes not only provide photon-trapping and high optical absorption but also contribute to the reduction of the junction capacitance by decreasing the junction area in an axial PIN diode. Figure 4.22. demonstrates the capacitance–voltage measured from PDs (500 μm in diameter) with and without air nanoholes. The blue curve represents calculated C by considering reduced area caused by cylindrical air holes in the devices. It agrees well with the measured C of PDs with cylindrical holes. The capacitance reduction is enhanced by funnel-shaped holes, in accordance with larger reduction of top contact during funneling process.

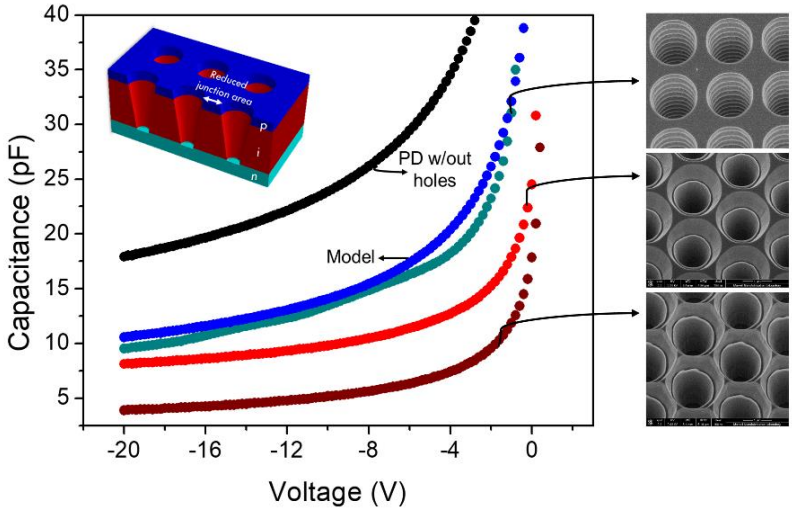


Fig. 4.22. Capacitance vs voltage (CV) characteristics of Si PDs without holes (control), with cylindrical, funnel and cross-linked holes, blue line indicates the estimated capacitance of cylindrical holes, inset: schematics of axial pin junction, indicating reduced junction area.

Due to the larger ratio between the active region over the total device area in PDs, with a bigger diameter in our current design, it is expected to observe a bigger capacitance difference in such devices as can be depicted in Fig. 4.23. The percentage of capacitance reduction has been recorded for all the periods and holes fabricated and compared with respect to the control device. PD's with a large diameter, such as 500 μm are expected to have more than 50% of capacitance reduction in the fabricated current designs. Devices with smaller diameter, such as 100 μm are estimated to have a capacitance reduction of around 30%. Smaller devices present lower capacitance reduction due to the number of holes that can be placed on its surface. The narrower distances between nanoholes are around 300 nm which present the higher capacitance reduction as can be seen in Fig. 4.23. However, state-of-the-art semiconductor foundries can fabricate narrower ohmic rings, allowing to increase the number of holes, and the distance between them, allowing to increase the filling fraction of the nanohole array and decrease its capacitance further. In such a case, it is expected to obtain a capacitance reduction of more than 50%, when nanoholes have d/p ratios higher than 0.8 and are arranged in a hexagonal lattice.

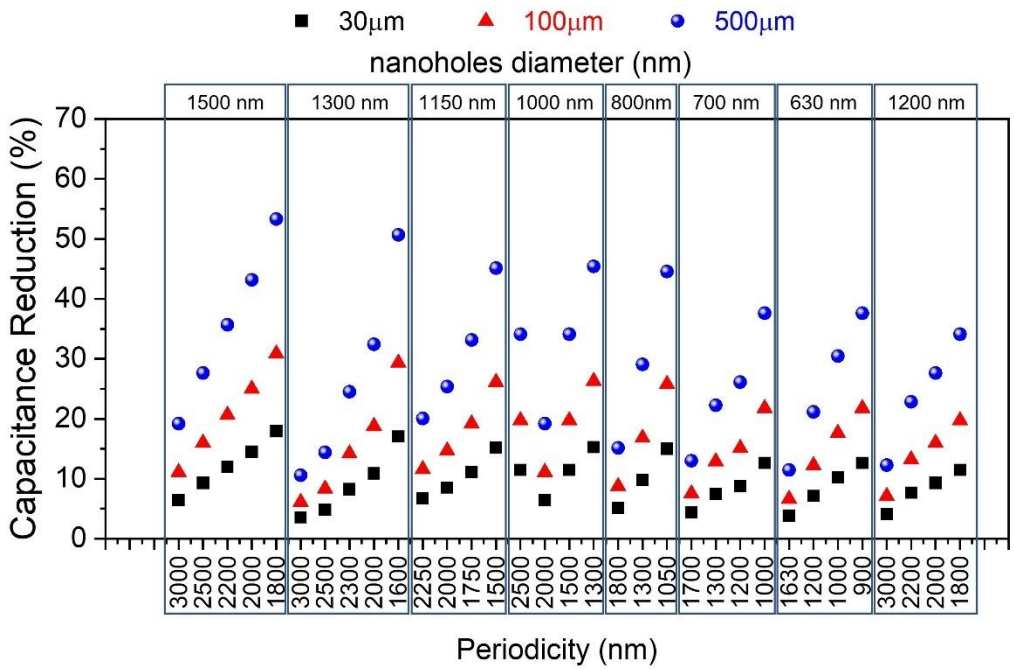


Fig. 4.23. Capacitance reduction in silicon PT PDs. Capacitance measurements were performed over PDs with different diameters and periods.

4.4.9 Capacitance reduction and pulse response enhancement in photon trapping Si PIN PDs

High-speed characterization has been performed using a mode-locked fiber laser with incident wavelength of 850 nm with an input average power of 100 μW. The FWHM of the laser pulse delivered to the PD surface was increased to ~5 ps due to propagation through a few meters of fiber. The light beam was aligned close to normal to the surface to reach maximum photocurrent. The device output signal was recorded by a sampling scope with a 3 dB bandwidth of 20 GHz (DSA8300, Tektronix). The measured results of capacitance-voltage (C-V) performed on the PDs with a diameter of 30 and 80 μm are shown in Fig. 4.24 (a) and Fig. 4.24 (c), respectively. The experimental C-V measurements between the control and the PT PD show a 15% and 35% of capacitance reduction for PDs with 30 and 80 μm of diameter, respectively. The percentage of area covered by the top ohmic contact is more considerable in PDs with mesas with a smaller diameter. The ratio of the active region to the total area of the PD is considered to estimate the capacitance of PDs with holes.

Figure 4.24 (b) shows the full-width-half-maximum (FWHM) of the impulse response has been reduced up to 25% in the PD with 80 μm diameter from FWHM of 101 ps in control PD to 76 ps in nanoholes PD. This is due to the reduced effective capacitance and consequently reduced RC time in PT PDs compared with the control devices. Higher FWHM and RC time reduction can be achieved in optimally designed PT PDs by fabricating them with closely packed nanoholes and narrower ohmic contacts in advanced semiconductor foundries[19].

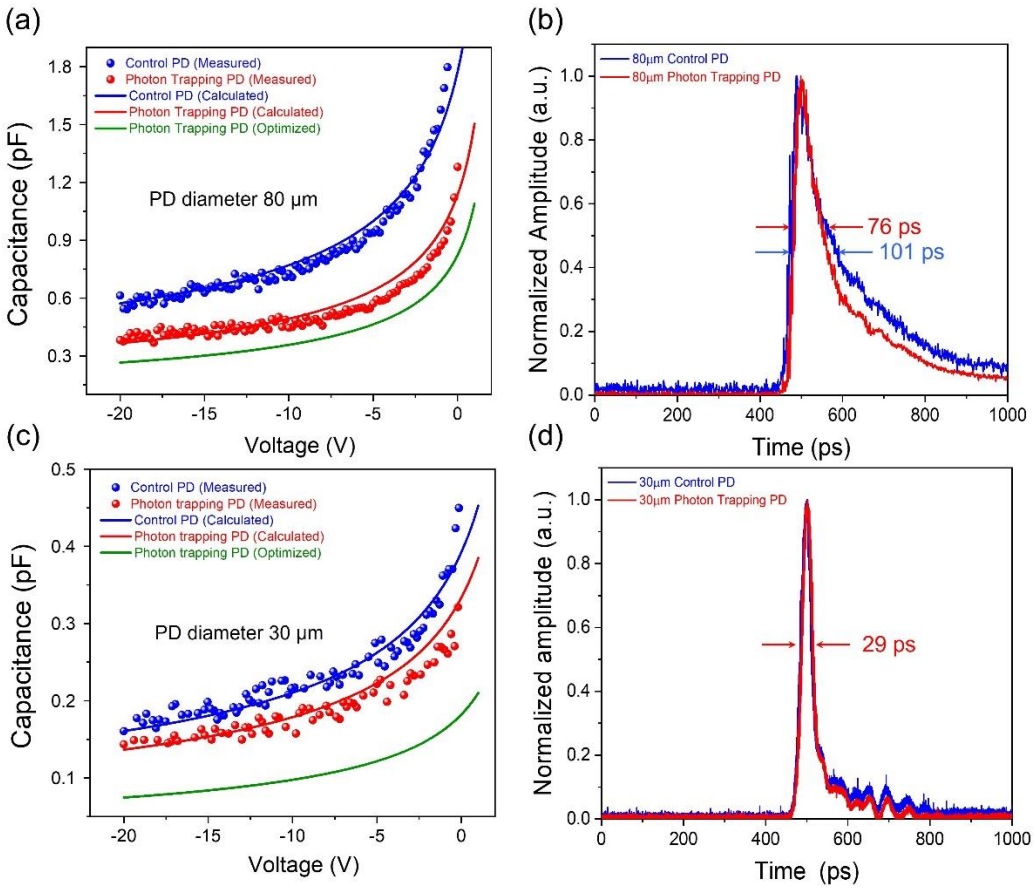


Fig. 4.24. (a) Capacitance–voltage characteristics of PDs comparing PT and control device in 80 μm diameters, confirming 35% capacitance reduction. This leads to up to 25% narrower FHWM in the pulse time response. (b) 25% narrower FWHM in 80 μm diameters with PT Si PD. Over 50% capacitance reduction can be realized by increasing the number of PT nanoholes. (c) Capacitance–voltage characteristics of PDs comparing PT and control device in 30 μm diameters, confirming 15% capacitance reduction. (d) FWHM of PT Si PD (30 μm diameter) with lightly better performance comparing to control Si PD.

The optimized calculated collective absorption enhancement of >75%, the capacitance reduction of >50% and the pulse response enhancement by FWHM reduction of >35% can be seen in Fig.

4.25 (a). Figure 4.25 (b) shows a drastic reduction in the capacitance can dramatically enhance the ultrafast operation of a PD. Figure 4.25 (c) shows the impulse response of the control PD with a diameter of 30 µm is measured to be 30 ps, and with optimum photon trapping nanoholes implementation can reach up to 19 ps FWHM[19].

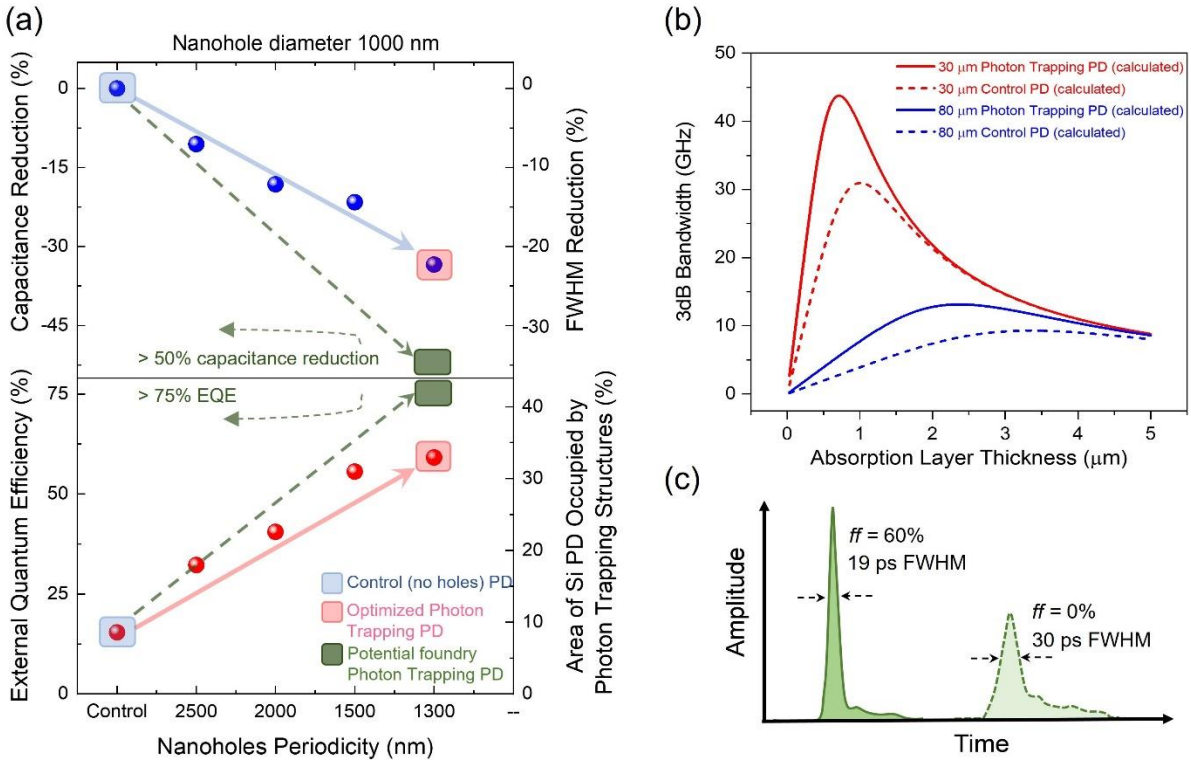


Fig. 4.25. (a) A study of >150 different device designs are used to optimize PT PDs with simultaneous improvement in EQE, reduction in capacitance, and enhancement in time response. A set of devices with a fixed d of 1000 nm and different periods are used to show that >50% of capacitance reduction and >75% of EQE can be achieved at 850 nm. (b) Modeling of 3 dB bandwidth versus absorption layer thickness considering 60% of capacitance reduction in PT PDs. (c) Sharper signal amplitude, and a narrower impulse response of 19 ps is possible in a 30 µm PT PD.

4.4.10 Photon trapping Si PD linearity characteristics

The photodiodes were biased at varying voltages and were found to show a flat EQE above 2.0 V bias. The *pin* PDs exhibit breakdown voltages larger than 30 V. The dark-current of a device with the diameter of 30 µm at -5 V bias was 0.06 nA as can be seen in Fig. 4.26 (a). In datacom and computer networks, the link length is between 100 m at 25 Gb/s to 300 m at 10 Gb/s [20] and the PDs may need to absorb higher than typical power used in communication links [21]. A thin

absorption region can limit the maximum power handling capability of a PD, contributing to some nonlinearities in the currents. Nonlinearity is caused by a decrease in the electric field under intense illumination that lowers the carrier velocity and decrease in the width of the depletion region due to a space-charge effect or an electric-field screening. This may degrade the signal-to-noise ratio, especially in the newly proposed 4 levels pulse-amplitude modulation (PAM-4) systems [22]. Due to effective light propagation parallel to the direction of the PD surface, the power per unit volume remains at a low level in our PDs, contributing to high linearity. Figure 4.26 (b) shows the fabricated photon trapping si PDs, even with a thinner absorption layer (~1 µm) than the design thickness (2 µm), the devices found to remain linear for as high as ~10 mA of DC current when biased above 5 Volts.

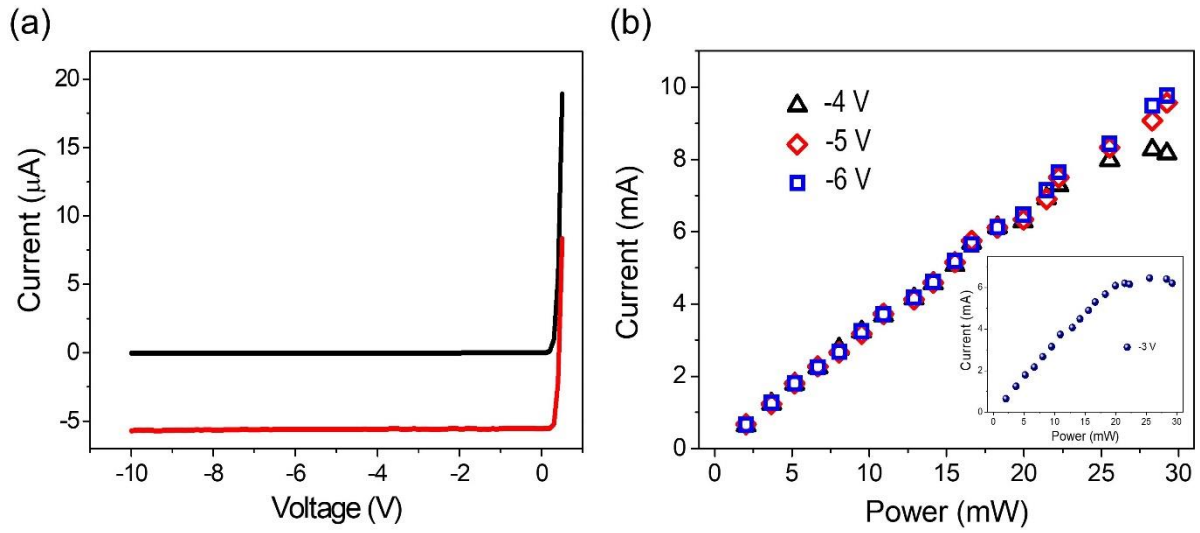


Fig. 4.26. DC and linearity characteristics of Si PIN. (a) Current-voltage (I-V) characteristics of a PD in dark and with illumination. (b) DC linearity characteristics of the PDs. Photon propagation parallel to the direction of the PD surface keeps the power per unit volume at a low level and contributes to high linear photocurrent.

4.4.11 Ultra-fast characteristics of the Si PD and ultimate bandwidth-efficiency

The fabricated ultra-fast Si PD SEM is shown in Fig. 4.27 (a), whereas photon trapping Si PD ultra-fast characteristics is shown in Fig. 4.27 (b). The measured pulse response when the device was biased at above 3V using a 25-GHz bias-T. The measured FWHM from the oscilloscope was

around 29-30 ps with a rise time of ~10 ps. Considering the 22-ps FWHM response for the 20-GHz oscilloscope and the optical laser pulse width of <1 ps, the actual response of the device was estimated to be 20 ps at 850 nm based on Equation 4.4. [23],

$$\tau_{meas} = \sqrt{\tau_{actual}^2 + \tau_{scope}^2 + \tau_{optical}^2} \tag{4.4}$$

where τ_{meas}, τ_{actual}, τ_{scope} and $\tau_{optical}$ are the measured, actual, oscilloscope, and laser optical pulse widths in time domain. This is acceptable for Gaussian pulses and is a valid approximation for our actual measurements. This is the fastest reported response for a silicon photodetector with such high quantum efficiency. The performance corresponds to a data transmission rate of 25 Gb/s or higher, there is a residual photocurrent tail after the pulse fall-time due to slow diffusion of photo-generated minority carriers in *p*- and *n*-layers where the doping profile is soft and not abrupt with the *i*-layer due to dopant diffusion of boron (B) and phosphorus (P) during the epitaxial growth. The slow diffusion tail can be minimized by growing more abrupt *p*-*i* and *i*-*n* interfaces.

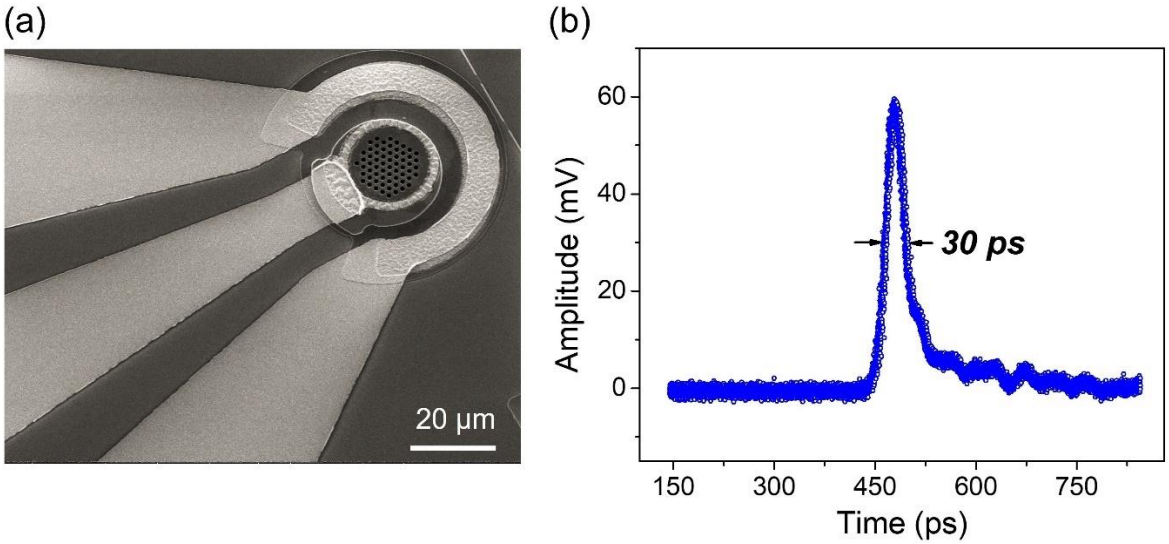


Fig. 4.27. (a) SEM image of the fabricated Si photon-trapping PD with a high-speed coplanar waveguide (CPW) transmission line. (b) By illuminating a PD with a sub-picosecond pulse, a 30 picosecond FWHM response was observed by a 20-GHz oscilloscope, which is a measurement setup with limited response. When corrected for the oscilloscope bandwidth and laser pulse width, the device temporal response is estimated to be 20 ps at 850 nm.

The 3 dB frequency bandwidth of a photon trapping PD can be further optimized by the reduction of capacitance observed in our devices, and by using a proper intrinsic layer thickness. Figure 4.28 shows the estimated 3 dB bandwidth of PD for the intrinsic layer thickness in a conventional PD and the novel photon-trapping PDs (assuming a 60% of capacitance reduction) for a 12 µm diameter device. Hence a PD with 12 µm of diameter is expected to have its highest 3 dB frequency of operation over 100 GHz with only 0.4-0.7 µm of thickness. Enhancing the 3dB frequency value >30% is possible if 50% of its capacitance is reduced. With the photon-trapping approach, such speed enhancement can be considered since the capacitance is reduced. Additionally, the efficiency enhancement allows us to consider such thin layers. Figure 4.28. illustrates the possibility for optimization of the intrinsic layer thickness with such a high 3 dB bandwidth. Sensors that require photodetectors with a large area, such as single-pixel imagers, would be limited in speed of operation due to their large junction capacitance related with the area of the device. However, photon trapping structures implemented in such devices can decrease their capacitance, enhance the optical absorption and enhance their speed of operation, enabling imaging systems with higher resolution which will be discussed in chapter 8.

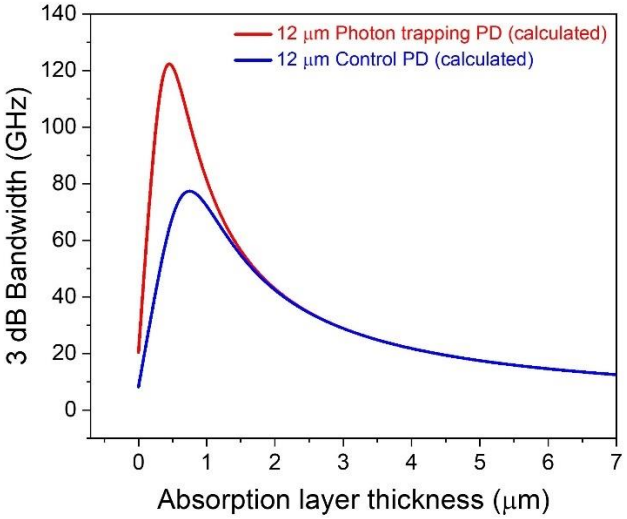


Fig. 4.28. Estimated 3 dB bandwidth of operation for silicon PDs with different absorption layer thicknesses for the 12 µm diameter PDs. A photon-trapping PD is assumed to achieve over 100 GHz 3-dB bandwidth of operation which would require a thickness of 0.4- 0.7 µm.

References

[1] S. John, "Why trap light?," *Nature materials,* vol. 11, no. 12, pp. 997-999, 2012.

[2] Y. Park *et al.*, "Absorption enhancement using photonic crystals for silicon thin film solar cells," *Optics express,* vol. 17, no. 16, pp. 14312-14321, 2009.

[3] M. D. Kelzenberg *et al.*, "Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications," *Nature materials,* vol. 9, no. 3, pp. 239-244, 2010.

[4] E. Garnett and P. Yang, "Light trapping in silicon nanowire solar cells," *Nano letters,* vol. 10, no. 3, pp. 1082-1087, 2010.

[5] S. E. Han and G. Chen, "Optical absorption enhancement in silicon nanohole arrays for solar photovoltaics," *Nano letters,* vol. 10, no. 3, pp. 1012-1015, 2010.

[6] K. X. Wang, Z. Yu, V. Liu, A. Raman, Y. Cui, and S. Fan, "Light trapping in photonic crystals," *Energy & Environmental Science,* vol. 7, no. 8, pp. 2725-2738, 2014.

[7] P. Kuang, S. Eyderman, M.-L. Hsieh, A. Post, S. John, and S.-Y. Lin, "Achieving an accurate surface profile of a photonic crystal for near-unity solar absorption in a super thin-film architecture," *ACS nano,* vol. 10, no. 6, pp. 6116-6124, 2016.

[8] T. F. Krauss, "Slow light in photonic crystal waveguides," *Journal of Physics D: Applied Physics,* vol. 40, no. 9, p. 2666, 2007.

[9] E. Yablonovitch and G. D. Cody, "Intensity enhancement in textured optical sheets for solar cells," *IEEE Transactions on electron devices,* vol. 29, no. 2, pp. 300-305, 1982.

[10] F. Laermer and A. Schilp, "Method of anisotropically etching silicon," ed: Google Patents, 1996.

[11] P. Dixit, S. Vähänen, J. Salonen, and P. Monnoyer, "Effect of process gases on fabricating tapered through-silicon vias by continuous SF6/O2/Ar plasma etching," *ECS Journal of Solid State Science and Technology,* vol. 1, no. 3, p. P107, 2012.

[12] H.-D. Ngo *et al.*, "Plasma etching of tapered features in silicon for MEMS and wafer level packaging applications," in *Journal of Physics: Conference Series*, 2006, vol. 34, no. 1: IOP Publishing, p. 045.

[13] D. S. Tezcan *et al.*, "Development of vertical and tapered via etch for 3D through wafer interconnect technology," in *2006 8th Electronics Packaging Technology Conference*, 2006: IEEE, pp. 22-28.

[14] F. Saffih, C. Con, A. Alshammari, M. Yavuz, and B. Cui, "Fabrication of silicon nanostructures with large taper angle by reactive ion etching," *Journal of vacuum science & technology b, nanotechnology and microelectronics: materials, processing, measurement, and phenomena,* vol. 32, no. 6, p. 06FI04, 2014.

[15] Y. Gao *et al.*, "High speed surface illuminated Si photodiode using microstructured holes for absorption enhancements at 900–1000 nm wavelength," *ACS Photonics,* vol. 4, no. 8, pp. 2053-2060, 2017.

[16] J. Zhao and M. A. Green, "Optimized antireflection coatings for high-efficiency silicon solar cells," *IEEE Transactions on electron devices,* vol. 38, no. 8, pp. 1925-1934, 1991.

[17] T. G. Mayerhöfer, S. Pahlow, and J. Popp, "The Bouguer-Beer-Lambert law: Shining light on the obscure," *ChemPhysChem,* vol. 21, no. 18, pp. 2029-2046, 2020.

[18] S. B. Alexander, *Optical communication receiver design*. SPIE Press, 1997.

[19] C. Bartolo-Perez *et al.*, "Maximizing Absorption in Photon-Trapping Ultrafast Silicon Photodetectors," *Advanced Photonics Research,* vol. 2, no. 6, p. 2000190, 2021.

[20] E. R. Fuchs, R. E. Kirchain, and S. Liu, "The future of silicon photonics: not so fast? Insights from 100G ethernet LAN transceivers," *Journal of Lightwave Technology,* vol. 29, no. 15, pp. 2319-2326, 2011.

[21] J. A. Tatum *et al.*, "VCSEL-based interconnects for current and future data centers," *Journal of Lightwave Technology,* vol. 33, no. 4, pp. 727-732, 2015.
[22] B. Moeneclaey *et al.*, "A 64 Gb/s PAM-4 linear optical receiver," in *2015 Optical Fiber Communications Conference and Exhibition (OFC)*, 2015: IEEE, pp. 1-3.
[23] K. Rush, S. Draving, and J. Kerley, "Characterizing high-speed oscilloscopes," *Ieee Spectrum,* vol. 27, no. 9, pp. 38-39, 1990.

Chapter 5 Efficient low-cost silicon solar cells integrated with surface light-trapping nanostructures for indoor and outdoor self-standing IoT sensors

5.1 Light-trapping Si photovoltaic (PV)

Effective light trapping structures have been of great interest as a method of enhancing light absorption in ultrathin film silicon-based solar cells (SCs)[1-5]. In this chapter, various nanohole (NH) arrays are designed, simulated, and experimentally investigated as light-trapping (LT) structures. The absorption in the ultrathin film (2 μm) crystalline silicon (c-Si) is maximized by optimizing the NH size, period, and pattern geometry. Surface NH structures were used to demonstrate an enhancement of more than 80% in conversion efficiency η>7 % with only 2 μm ultrathin Si and more than two folds short-circuit current density (Jsc =30.1 mA/cm^2) compared to its counterpart of planar (control) ultrathin Si. Furthermore, it has been shown that NH arrays exhibit a significant anti-reflection effect and a correlation between the reflection and wavelengths is presented. Such ultrathin Si and highly efficient photovoltaics (PV) have the ability to be utilized for the emerging indoor and outdoor self-standing IoT sensors and portable devices.

5.2 Solar cell design

The designed LT solar cell schematics are shown in Fig. 5.1. The structure consists of a 2 μm thin intrinsic layer (i-layer) sandwiched between heavily doped p-type and n-type layers. The ultrathin absorbing layer was grown on a 300 nm thin Si device layer of an SOI substrate which has a 3 μm thin silicon dioxide (SiO_2) layer on the handle wafer. All solar cells are designed with an identical hole depth of ~ 1.8 μm. Square and Hexagonal lattice unit cells NH arrays are designed to examine the effect of array geometry on enhancing absorption in SCs. Circular NHs are chosen for surface texturing with the same lattice periodicity (p) in both the x and y directions to offer topography independence over the planar directions. Filling fraction (ff), defined as the fraction of area occupied by silicon in a unit cell, is also an important parameter in designing NH

arrays. It can be found by $1 - \pi d^2/4p^2$, where d and p are the diameter and pattern's periodicity of the circular holes, respectively.

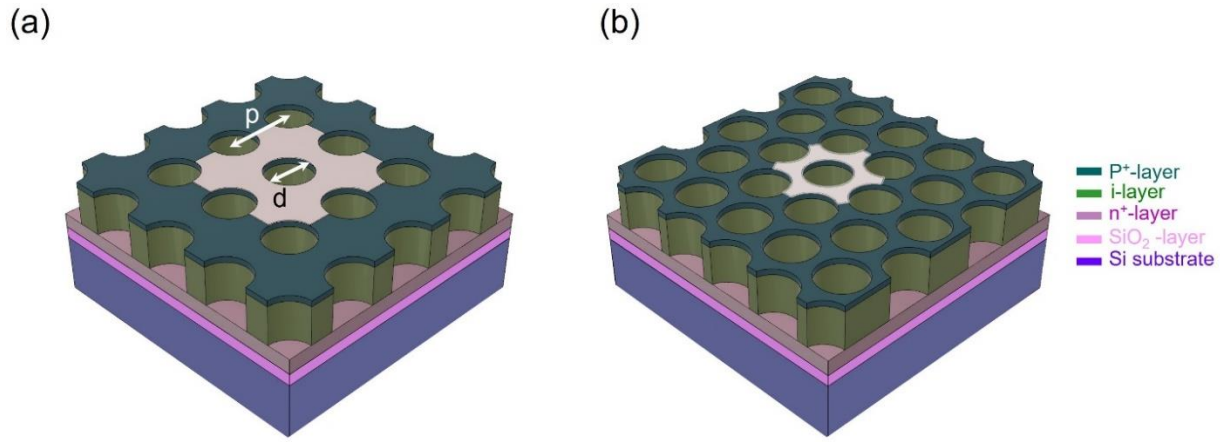


Fig. 5.1. Schematics of the ultrathin film solar cell with surface NH light-trapping (LT) structures on a silicon-on-insulator (SOI) wafer, where d is the hole diameter and p is the pattern periodicity. (a) Square lattice, b) Hexagonal lattice NH array.

5.3 Optical simulation

The optics of the thin-film c-Si SCs is investigated with the aid of the Finite-Difference Time-Domain (FDTD) method. The influence of light-trapping NH arrays integrated with SCs is studied on the absorption, quantum efficiency, and reflection, where both square and hexagonal lattices are taken into consideration. The simulated electromagnetic (EM) energy field distribution within the silicon absorber layer is presented in Fig. 5.2 (a)-(c) for a monochromatic incident wavelength of 670 nm. The cross-sectional views presented in Fig. 5.2 (a) (x-z plane, cross-sectional view) and Fig. 5.2 (b) (x-y plane, top view) are EM light confinement inside the active region of the SC with hexagonal array geometry. The structure is illuminated by a short-pulsed plane wave (λ=400-1100 nm) normal to the surface and the Poynting vector is recorded right after the pulse passes the 2 μm-thin devices. It can be seen that NHs can support a group of vertical and lateral modes in a wide range of wavelengths. Holes direct the modes to the silicon sidewalls and provide a lateral Poynting vector that leads to horizontal (parallel to the surface) wave propagation. Furthermore, the top air-Si and the bottom Si-SiO_2 interfaces confine the guided lateral modes to propagate along the absorption region. Additionally, the bottom SiO_2 layer improves the light-

trapping in the active region by providing back reflection. However, solar cell devices fabricated on bulk silicon wafers pronounce less capability to maintain lateral mode propagation as a considerable number of photons pass through the device layer into the silicon substrate. Moreover, propagated lateral modes from different holes can couple together to enhance light trapping effectively due to the periodic arrangement of NHs. Next, the cross-section for the energy density distribution of the square lattice NH array is shown in Fig. 5.2 (c). Similar to the hexagonal NH pattern, square lattice shows the capability to support both vertical and lateral modes as well as coupling of the propagating modes to the side walls and directing the Poynting vector laterally.

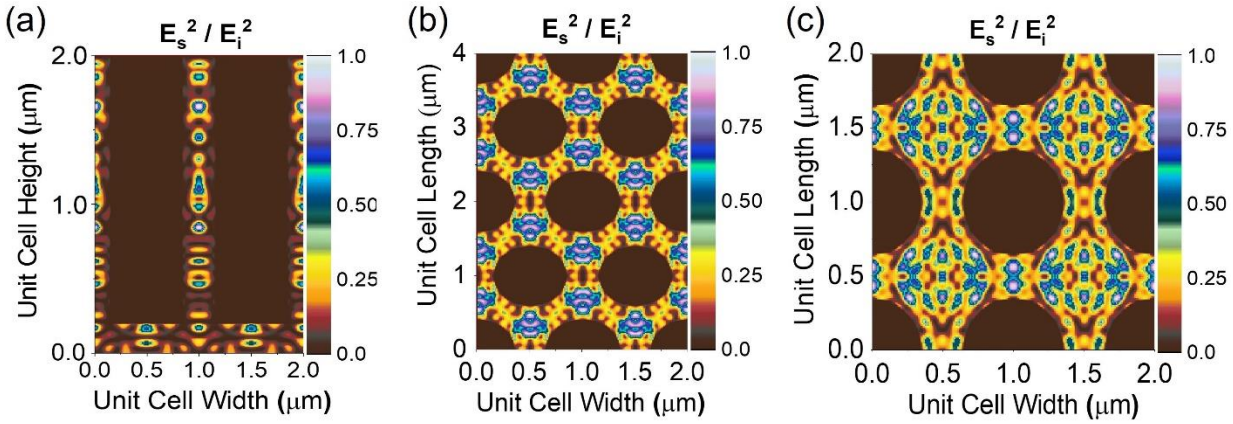


Fig. 5.2. Electromagnetic (EM) energy field distribution. (a) Cross-section view x-z plane, b, c) hexagonal and square lattice top view (x-y plane) for energy density distribution (λ=670nm) shows the lateral field propagation in 2 μm ultra-thin c-Si.

The optical confinement profile of each hole with six field peaks in a hexagonal lattice pattern is shown in Fig. 5.3 (a), where it clearly shows the coupling of the lateral modes in a 3D plot. Fig. 5.3 (b) is a 2D surface optical confinement representation of Fig. 5.3 (a). In the hexagonal arrangement, the central hole is surrounded by six adjacent holes that lead to mode coupling in six directions. However, compared to the hexagonal pattern, the square lattice exhibits a relatively lower ability to couple guided modes in the active region. Thus, less photon absorption can be expected. This is also confirmed by the calculated absorption as shown in Fig. 5.4 (a).

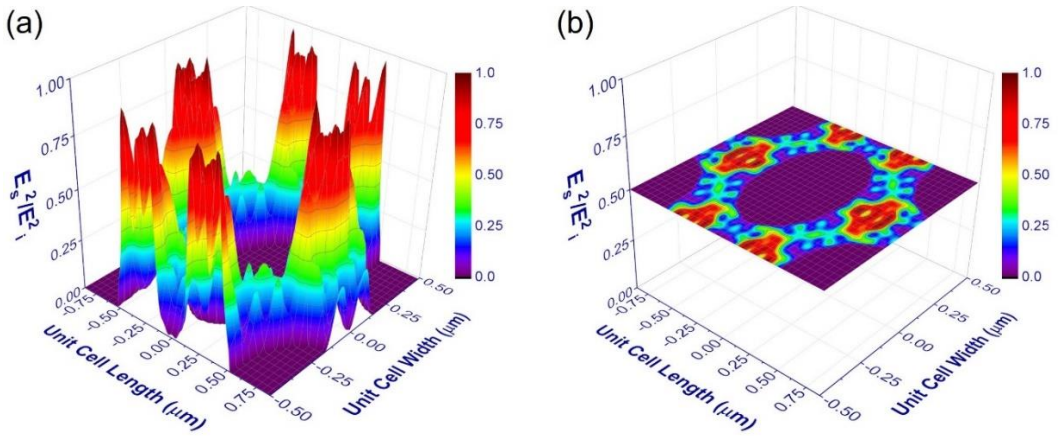


Fig. 5.3. Optical light confinement in a hexagonal lattice. (a) 3D demonstration of light concentration (six peaks) due to the coupling of guided modes in silicon side walls. (b) 2D representation of light confinement.

In the following, the influence of the light-trapping NH structures is investigated on the absorption and reflection of the ultrathin c-Si SCs. LT Solar cell with tapered side wall profile of the NHs is included with a hexagonal lattice to compare with other designs. The simulated absorption and reflection spectrum of solar cells with NH surface arrays are compared with flat SC as shown in Fig. 5.4 (a) and (b), respectively. The overall absorption in the solar cells is distinctly increased by employing the NH arrays, while the reflection is reduced in both shorter and longer wavelengths. The drop in absorption near the UV region (λ=400 nm) is mainly due to the higher refractive index difference in the interface of silicon/air, which also increases reflection from the surface as seen in Fig. 5.4 (b). Maximum absorption occurs in the visible region (~550nm) and slightly diminishes with Fabry-Perot resonances at longer wavelengths as it approaches silicon bandgap wavelength. Figure 5.4 (a) includes the optical spectrum of two ordinary indoor light sources, a white lamp (standard F3 illuminant) and a white normalized and superimposed on SCs absorption for indoor applications[6]. The white LED and fluorescent light (F3) primarily radiate in the visible wavelength range while the solar radiation spectrum covers a large range from the UV to IR longer wavelengths.

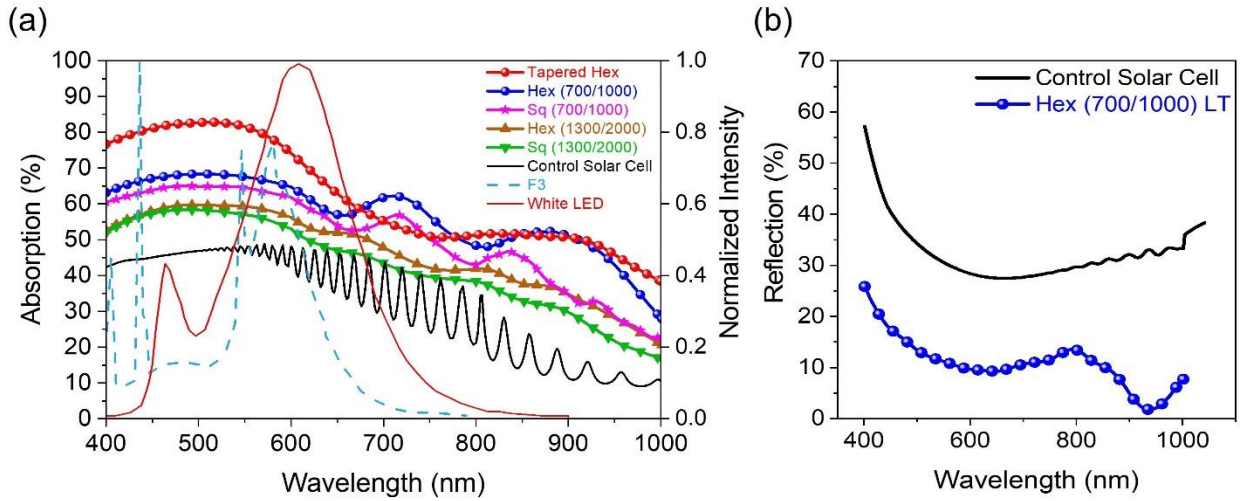


Fig. 5.4. Calculated absorption and reflection. (a) Absorption of hexagonal, square lattice NH arrays (d/p=700/1000, 1300/2000), and tapered hexagonal compared to non-patterned 2 μm thin Si. The LED and fluorescent lamp (F3) spectra are normalized to show indoor application optical coverage in Si. (b) Calculated reflection of hexagonal (d/p=700/1000) light-trapping (LT) compared to non-patterned 2 μm silicon SC.

Then the hexagonal arrangement of NHs -both 1300/2000 nm and 700/1000nm manifests more light trapping ability than similar NHs with square lattice. Stronger coupling of guided lateral modes in hexagonal structures can be an appropriate explanation for this observation. Furthermore, NHs with smaller d/p dimensions (closer to the incident wavelengths) are found to be highly pronounced in improving absorption in both hexagonal and square arrays. Hence, it can be concluded that a larger number of holes per unit area together with an optimum filling fraction (ff) are imperative to maximize absorption. However, tapering the holes (tapered sidewalls of the holes) offer a couple of advantages over cylindrical profile holes. FDTD simulation shows that tapered holes have higher optical absorption and lower reflection than cylindrical holes. In the tapered holes, the effective refractive index gradually varies from the surface through the Si, while the effective refractive index abruptly changed in the cylindrical holes. Hence, the design of the funnel-shaped hole offers an effect similar to a graded-refractive-index antireflection (AR) coating [7].

In the next step, the ultimate efficiency (η) of the thin-film solar cell is calculated, which is defined as the maximum efficiency of a PV cell when each photon with sufficient energy (<$\lambda_{bandgap}$) generates a pair of electron-hole (at $0^{o}K$ temperature) and is given by:

$$\eta \frac{\int_0^{\lambda_g} I(\lambda)\ A(\lambda) \frac{\lambda}{\lambda_{bandgap}} d\lambda}{\int_0^{\infty} I(\lambda)\, d\lambda} \tag{5.1}$$

where $I(\lambda)$ is the AM1.5 solar spectrum [8]. Absorption corresponding to the wavelength A(λ) is calculated from equation (5.2):

$$A(\lambda) = (1 - R(\lambda))\,(1 - e^{-\alpha_{eff}(\lambda)d}) \tag{5.2}$$

where d is the absorption layer thickness and $R(\lambda)$ and $\alpha_{eff}(\lambda)$ are the device reflectance and effective absorption coefficient as a function of wavelength, respectively. The ultimate efficiency for ideal Si-based SC (A=100%) is 44%. The ultimate efficiency for SCs with NH arrays of hexagonal and square arrangements is calculated and compared with the control solar cell. As expected, tapered holes with hexagonal pattern presents the highest calculated ultimate efficiency of 30%, and around 24% experimentally measured (ultimate efficiency derived from Fig. 5.7), which is ~80% higher than non-patterned structure or the planar control solar cells as can be seen in Fig. 5.5. Subsequently, hexagonal pattern with cylindrical holes (700/1000) shows a high ultimate efficiency compared to the remainder's designs.

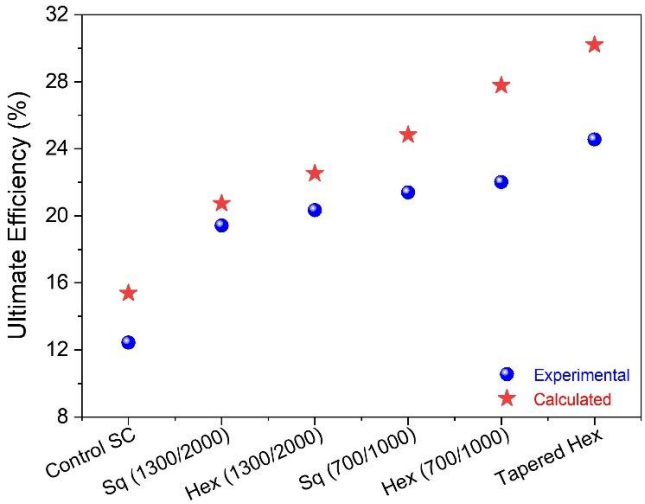


Fig. 5.5. Ultimate efficiency of SCs without NH array and SCs with light-trapping designs.

5.4 Solar cell Fabrication

Silicon SCs are fabricated with a mesa-type structure, where the doping layers are epitaxially grown as a P-I-N structure with an absorbing i-layer thickness of 2 µm while the p-type and n-type heavily doped (top and bottom) layers are around 0.25 µm, respectively. Figure 5.6 (a) shows the complete solar cell integrated with LT nanoholes array on the active area. Different nanohole designs are implemented in the silicon SCs such as cylindrical holes, and tapered (Tap) holes, which are arranged as square lattice pattern [Fig. 5.6 (b)] and hexagonal lattice patter [Fig. 5.6 (c,d)]. Cylindrical holes are referred to nanoholes with a straight hole's side walls [Fig. 5.6 (b,c)] while tapered holes side walls have a tapered side walls profile [Fig. 5.6 (d)). The holes formation process scheme is further discussed in section 4.4.3. The device was immersed in diluted HF solution (1:10=HF:H2O) for few seconds to passivate the dry etched induced surface damages in Si surface[9, 10]. The top view SEM images of square, hexagonal, and tapered profile arrangements of holes presented in Fig. 5.6.

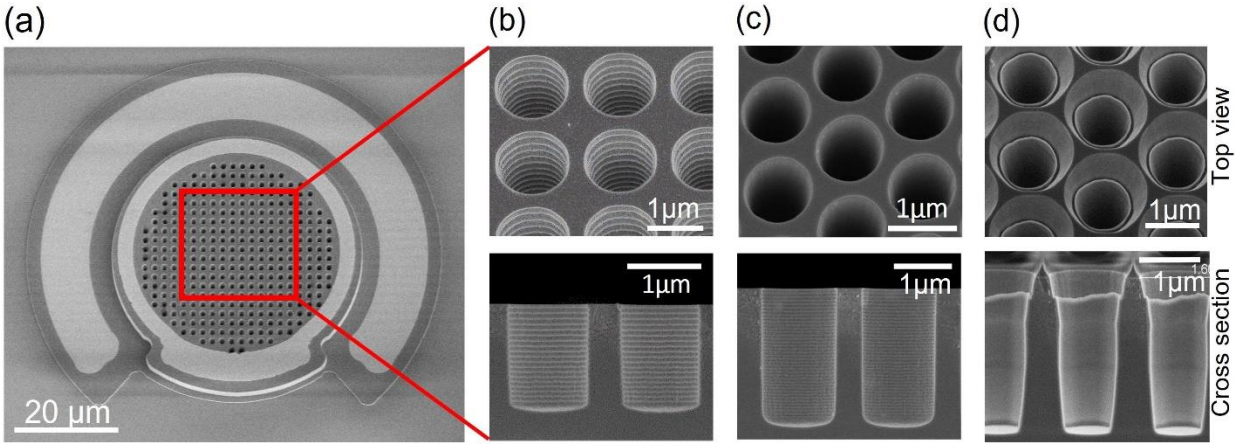


Fig. 5.6. Scanning electron micrograph (SEM) image of the fabricated solar cells. (a) Completed solar cell device integrated with LT nanoholes. (b) Squared lattice cylindrical holes (Top and cross-section view), (c) Hexagonal lattice cylindrical holes (Top and cross-section view). (d) Hexagonal lattice tapered holes (Top and cross-section view).

5.5 Experimental results and discussion

5.5.1 External Quantum Efficiency (EQE)

In this section, the fabricated SCs are characterized and analyzed based on the measured external quantum efficiency (EQE). The EQE of hexagonal (cylindrical and tapered design) and square periodic NH arrays-based solar cells is measured and compared with a control SC. The measurement is performed for a wavelength spectrum ranging from 450 nm to 1100 nm for 2 µm ultrathin i-layer absorbing SC. This range of wavelengths covers the optical spectrum for indoor and outdoor SCs spectrum. It is evident that LT nanoholes present much higher EQE, compared to their counterpart of control SC. Furthermore, the experimental findings exhibit a good agreement with the simulated results. However, the discrepancy between expected and measured results is mainly due to fabrication issues such as non-ideal hole shapes, undesirable material defects, and surface traps. LT nanoholes designed with hexagonal lattice pattern and tapered holes shows the highest EQE for a wide range of the incident spectrum among all other designs as expected. While cylindrical holes with hexagonal lattice design show better performance than the square lattice design due to its superior light coupling design. The LT design with a comparable hole diameter and periodicity to the incident wavelength shows better absorbing performance than structures with larger holes and periodicity dimensions. Figure. 5.7 presents the characterized EQE for different LT designs with their counterpart of control SC. Additionally, the spectrum of indoor (F3 white fluorescent and White LED (2700 K)) and outdoor solar spectrum (AM1.5G) light source are superimposed in the same figure[6]. The EQE experimental results present the efficacy of LT designs to enhance absorbing performance of ultrathin low-cost flexible SCs for indoor and outdoor self-standing IoT sensors.

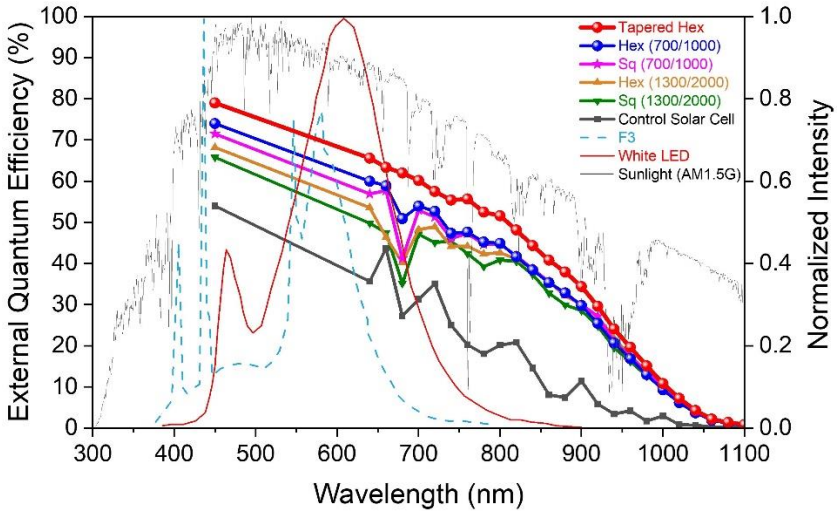


Fig. 5.7. Measured EQE of tapered, hexagonal (Hex), square (Sq) light-trapping (LT) NH array structure compared to the control solar cell. Sunlight spectrum for outdoor SC, F3 white fluorescent, and white LED (2700 K) for indoor SC are superimposed and normalized for their peak intensity values.

5.5.2 Optical and Electrical characterizations

The fabricated SCs then optically and electrically characterized and analyzed based on optical reflection, the J-V curves, open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}), fill factor (FF), and energy conversion efficiency (η). Figure 5.8 (a) presents the fabricated SC's surface reflection measurement. The reflection from the top surface of the NH light-trapping SC is distinctly reduced in comparison with the control solar cell, indicating that the structure acts as an effective anti-reflection coating. In addition, for the tapered holes, the effective refractive index gradually varies from the surface through the Si, while the effective refractive index abruptly changed in the cylindrical holes. Hence, the design of the funnel-shaped hole offers an effect similar to a graded-refractive-index antireflection (AR) coating [7], and hence further suppresses the incident reflections. The ability of NHs to inhibit reflection is more tangible in shorter wavelengths close to the UV region where the reflectance from the planar silicon slab increases drastically. Furthermore, the experimental findings exhibit a good agreement with the simulated results. Intriguingly, unlike the conventional solar cells, such a high reduction of reflection is achieved without using any antireflection coating and/or front transparent conductive oxide (TCO) layer. The measured reflectance of our optimized structure (represented by the solid line in the

attached measurement) and compared it with some literature results (dashed line) as seen in Fig. 5.8 (a) [11]. The results show that our optimized structure reduces reflectance compared to traditional AR coatings. Our optimized periodic hole design provides a simple, efficient and cost-effective alternative to traditional AR coatings for improving the absorption of thin silicon films, making it a promising solution for the photovoltaic industry. Although, it is worth noting that if ARC were to use in addition to the photon-trapping holes, the reflectance would further reduce in the proposed device structure.

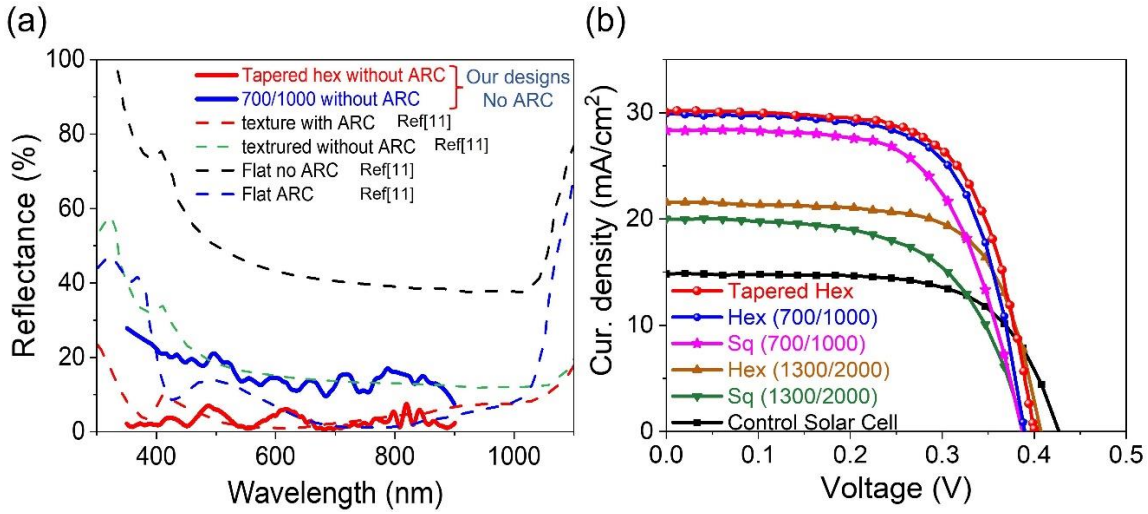


Fig. 5.8. Experimental characterizations for control SC and LT SC. (a) Reflection measurements for control SC vs. tapered hex and cylindrical hex nanoholes SC. (b) Current density for the fabricated SCs.

Next, the photovoltaic performance is characterized for the fabricated SCs with the aid of a solar cell simulator setup under AM1.5G spectrum illumination. The measured J-V characteristics curves for different light-trapping structures with holes and control solar cells are presented in Fig. 5.8 (b). Additionally, other basic performance parameters of open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}), filling factor (FF), and conversion efficiency (η) are calculated based on the J-V curves. The results are summarized in table 5.1. A 500 μm diameter solar cell with a tapered hexagonal NH array exhibits a maximum short circuit current density of Jsc=30.1 mA/cm^2 ; pronouncing more than two folds higher JSC as compared to the similar size device without NH array (14.84 mA/cm^2). The c-Si solar cell with a light-trapping NH structure of tapered hexagonal

lattice arrangement outperforms the control solar cell as well as all other SCs with NH arrays with a maximum energy conversion efficiency of 7.78%. The efficiency enhancement is almost 80% higher than the control solar cell without NH array (4.18%). The measured conversion efficiency for tapered hexagonal design is marginally higher than cylindrical hexagonal (700/1000) SC. It can be concluded that NHs' dimensions play a pivotal role in boosting PV performance. Taking hexagonal arrays into account, arrays with smaller d/p size exhibit ~40% higher J_{sc} compared to larger sized NH arrays.

Light-Trapping Pattern (diameter/periodicity)	V_{oc} (V)	I_{sc} (mA/cm^2)	FF (%)	η (%)
Control Solar Cell	0.42	14.84	66.02	4.16
Sq (1300/2000)	0.39	20.04	60.14	4.69
Hex (1300/2000)	0.40	21.57	67.98	5.97
Sq (700/1000)	0.38	28.32	62.74	6.88
Hex (700/1000)	0.38	30	66.11	7.70
Tapered Hex	0.39	30	66.19	7.78

Table. 5.1. Characteristics of PVs with LT NHs compared to their control counterpart solar cells (AM1.5G illumination).

5.5.3 Solar cells LT designs and conversion efficiency

Many light-trapping solar cells were designed and fabricated to examine their performances. The highest conversion efficiency (η) of LT SCs was obtained for the tapered hexagonal LT designs. The cylindrical holes with hexagonal lattice patterns also present an enhanced SC conversion efficiency compared to the cylindrical holes with a square lattice pattern. However, both designs outperformed the conversion efficiency of the control solar cell as can be seen in Fig. 5.9 (a). It should be noted that, light-trapping designs solar cells can be arranged in many different parameters and hence can be optimized according to powering indoor or outdoor flexible sensors/portable devices. Figure. 5.9 (b) depicts tapered holes in square and hexagonal lattice pattern respectively. While Fig. 5.9 (c) presents cylindrical holes in in square and hexagonal lattice pattern, respectively.

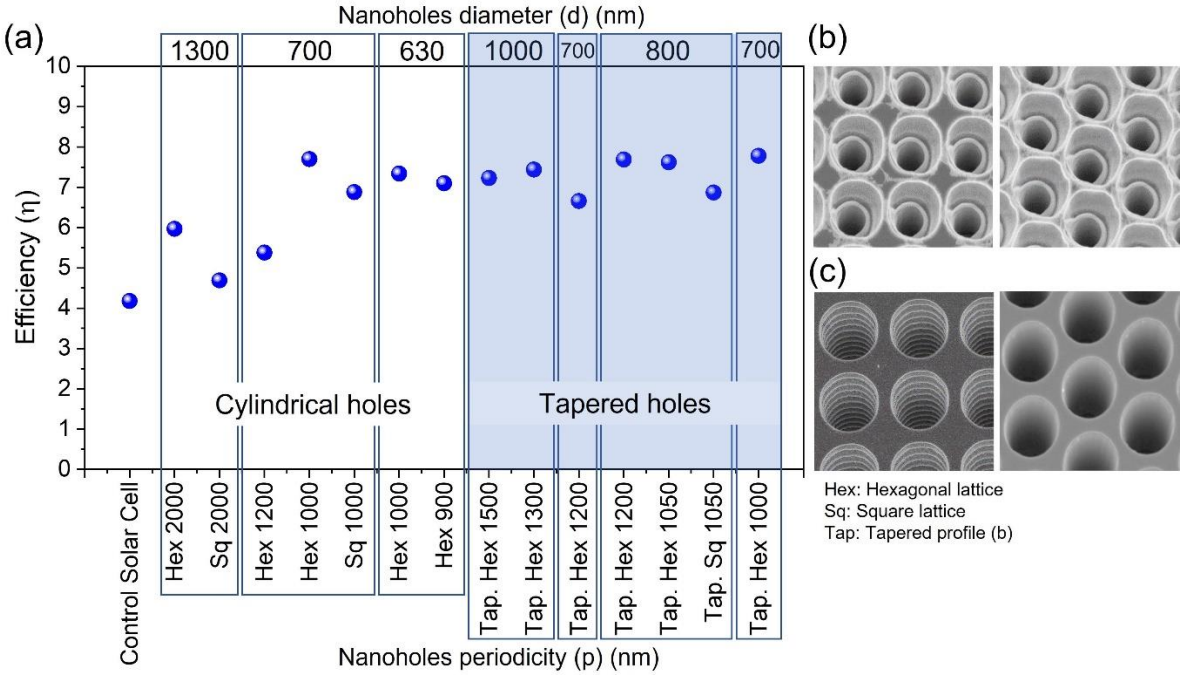


Fig. 5.9. A variation of different LT SCs designs compared to their counterpart control solar cell.

Simulation and experimental results have proven that significant enhancement in absorption for a wide spectrum up to silicon bandgap (NIR) has been accomplished through well-designed NH arrays with hexagonal and square geometries. Fabricated devices exhibit a high Jsc of 30.1 mA/$cm2$ and a fill factor of 66% has been achieved, resulting in a solar cell efficiency of 7.78% at AM1.5G with c-Si with 2 μm ultrathin absorbing i-layer. These results represent an enhancement of more than 80% in conversion efficiency as well as more than two-fold increase in the short-circuit current density compared to planar ultrathin film based SCs of similar thickness.

References

[1] G. Demésy and S. John, "Solar energy trapping with modulated silicon nanowire photonic crystals," *Journal of Applied Physics,* vol. 112, no. 7, p. 074326, 2012.

[2] S. Eyderman, S. John, and A. Deinega, "Solar light trapping in slanted conical-pore photonic crystals: Beyond statistical ray trapping," *Journal of Applied Physics,* vol. 113, no. 15, p. 154315, 2013.

[3] Y. Gao *et al.*, "High speed surface illuminated Si photodiode using microstructured holes for absorption enhancements at 900–1000 nm wavelength," *ACS Photonics,* vol. 4, no. 8, pp. 2053-2060, 2017.

[4] S. E. Han and G. Chen, "Optical absorption enhancement in silicon nanohole arrays for solar photovoltaics," *Nano letters,* vol. 10, no. 3, pp. 1012-1015, 2010.
[5] N. A. Yahaya, N. Yamada, Y. Kotaki, and T. Nakayama, "Characterization of light absorption in thin-film silicon with periodic nanohole arrays," *Optics express,* vol. 21, no. 5, pp. 5924-5930, 2013.
[6] V. Bahrami-Yekta and T. Tiedje, "Limiting efficiency of indoor silicon photovoltaic devices," *Optics express,* vol. 26, no. 22, pp. 28238-28248, 2018.
[7] J.-Q. Xi *et al.*, "Optical thin-film materials with low refractive index for broadband elimination of Fresnel reflection," *Nature photonics,* vol. 1, no. 3, pp. 176-179, 2007.
[8] E. D. Palik, *Handbook of optical constants of solids*. Academic press, 1998.
[9] A. S. Mayet *et al.*, "Surface passivation of silicon photonic devices with high surface-to-volume-ratio nanostructures," *JOSA B,* vol. 35, no. 5, pp. 1059-1065, 2018.
[10] A. S. Mayet *et al.*, "Inhibiting device degradation induced by surface damages during top-down fabrication of semiconductor devices with micro/nano-scale pillars and holes," in *Low-Dimensional Materials and Devices 2016*, 2016, vol. 9924: SPIE, pp. 36-42.
[11] H. Kanda *et al.*, "Al2O3/TiO2 double layer anti-reflection coating film for crystalline silicon solar cells formed by spray pyrolysis," *Energy Science & Engineering,* vol. 4, no. 4, pp. 269-276, 2016.

Chapter 6 High-efficiency and High-speed Si Avalanche /Single-photon Avalanche (APD/SPAD) photodetectors for low-light-level detection

6.1 Si CMOS compatible photon-trapping (PT) APDs/SPADs

An extremely low number of photons detectors operating at ultra-fast speed and high bandwidth are crucial for optical communications and emerging new technologies and applications. Emerging technologies require extremely sensitive, low-power, mass-manufacturable photodetectors such as Light Imaging and Ranging (LiDAR), Quantum Communications, Biophotonics, medical imaging systems, and other emerging applications. Recently, Avalanche Photodetectors (APDs) and Single Photon Avalanche Photodetectors (SPADs) detectors can meet those requirements. However, their bandwidth, sensitivity, and noise limitation must be overcome[1].

Currently, the conventional solution for low-light-level detection in many applications is the use of APDs and SPADs. Avalanche Photodetectors (APDs) are highly sensitive photodetectors (PDs) with an internal gain mechanism generated by the impact ionization of their carriers. This mechanism provides higher signal-to-noise ratios and higher optical sensitivities. The gain depends on the internal electric field and consequently on the applied reverse bias. In APDs, the output photocurrent is linearly proportional to the input optical power when APDs work at lower than their breakdown voltage. While Single Photon Avalanche Photodetectors (SPADs) is also designed as avalanche PD that operate at higher reverse bias voltage (above the breakdown voltage), and this operation mode is known as Geiger mode operation[2]. The carriers generated by photon absorption undergo avalanche gain, initiating the breakdown of the diode junction. SPADs identify as a PD that can detect extremely low-intensity signals (down to a single photon level). Figure 6.1 shows the operation regime of conventional PD, APDs, and SPADs modes.

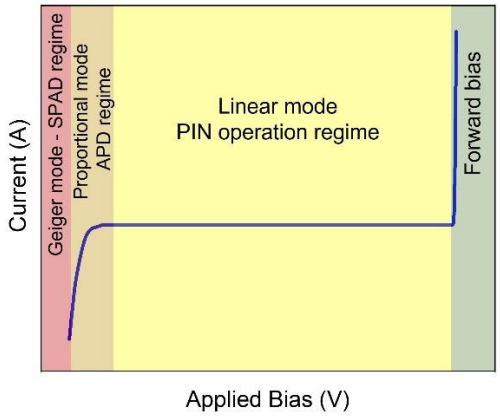


Fig. 6.1. Current-Voltage characteristics (operational mode) of PD, APD, and SPAD.

Silicon-based APDs and SPADs have the advantage to facilitate the fabrication of arrays integrated with other electrical components using the current CMOS foundry processes. All these advancements introduce the solutions for low-light-level photon detection required in many emerging applications.

To enhance these Si APDs and SPADs' performances, this chapter discusses the implementation of photonic nanostructures in photodetectors to boost their responsivity and gain by guiding the light parallel to its surface, which greatly enhances the interaction with the semiconductor material.

These APDs and SPADs with photon-trapping (PT) holes have the capability to be monolithically integrated with CMOS/BiCMOS application-specific integrated circuits (ASICs) and could offer a promising solution for waveguide photodetectors required for Photonic Integrated Circuits (PICs). Such APDs and SPADs are designed with the implementation of proper doping profiles for high amplification, thin Si layer for high speed (short transient-time), and optimized design of micro/nanoholes for highly sensitive and ultrafast optical receivers/sensors.

6.2 Engineering the gain and bandwidth in Si APD/SPAD enabled by designing photon-trapping nanostructures

APDs and SPADs depend on the probability of photogenerated carriers triggering a multiplication process. Photon penetration depth plays a vital role in this process. In silicon APDs, a significant

fraction of the short visible wavelengths is absorbed close to the device surface which is typically highly doped to serve as a contact. Most of the photogenerated carriers in this region can be lost by recombination, get slowly transported by diffusion, or multiplied with high excess noise. On the other hand, the extended penetration depth of near-infrared wavelengths requires thick semiconductors for efficient absorption. This diminishes the speed of the devices due to the long transit time in the thick absorption layer that is required for detecting most of these photons. This section demonstrates the possibility to drive photons to a critical depth in a semiconductor film to maximize their gain-bandwidth performance and increase absorption efficiency. This methodology for engineering the penetration depth for different wavelengths in silicon is enabled by integrating photon-trapping nanoholes on the device surface. The penetration depth of short wavelengths such as 450 nm is increased from 0.25 µm to more than 0.62 µm. On the other hand, for a long wavelength like 850 nm, the penetration depth is reduced from 18.3 µm to only 2.3 µm, decreasing the device transit time considerably. Such capabilities allow increasing the gain in APDs by almost 400× at 450 nm and by almost 9× at 850 nm. This engineering of the penetration depth in APDs would enable device designs requiring higher gain bandwidth in emerging technologies such as Fluorescence Lifetime Microscopy (FLIM), Time-of-Flight Positron Emission Tomography (TOF-PET), quantum communications systems, and 3D imaging systems[3].

Figure. 6.2. demonstrates the control of the penetration depth of light into silicon APDs which promotes the initialization of impact ionization by electrons and leads to a lower multiplication noise, and a higher gain bandwidth desired in avalanche-based photodetectors.

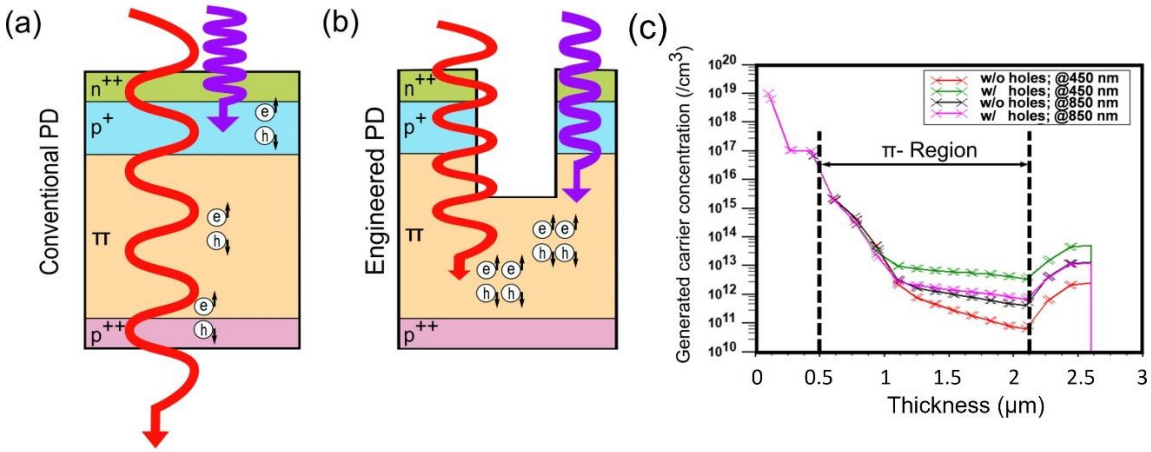


Fig. 6.2. Schematics of Si APDs layers. (a) Conventional penetration depth of short and long wavelengths in an avalanche PD structure with separate absorption and multiplication layers. Short wavelengths (such as blue light from 380 nm to 485 nm) are mostly absorbed close to the surface due to their high absorption coefficient. Longer wavelengths (such as red and near-infrared light from 625 nm to 1100 nm) travel deeper into the device. (b) A potentially engineered PD with integrated photon-trapping nanoholes can modify the penetration depth of the incident light. Shorter wavelengths travel deeper while longer wavelengths can be absorbed in a shorter distance. (c) Generated carrier concentration comparison between w/o holes and w/ holes PD structures both for 450 nm and 850 nm wavelengths.

6.2.1 Optical/Electrical simulations, Design, and Fabrication

6.2.1.1 Optical/Electrical simulations

To study the impact of photon-trapping structures on generated conducting carriers in presence of illumination, an ATLAS Silvaco TCAD simulation is performed. The presence of photon-trapping structures increases the carrier generation by an order of magnitude for 450 nm as well as 850 nm light wavelengths as shown in Fig. 6.2 (c). Such enhancement in the generated carrier concentration could be attributed to penetration depth modulation for both wavelengths. Due to the diffraction, the penetration depth for lower wavelengths such as 450 nm, increases, and due to the very same diffraction, the penetration depth for higher wavelengths such as 850 nm, decreases—resulting in enhanced absorption in the π-region (photogeneration i-layer)—causing enhanced carrier generation.

Additionally, FDTD analysis determines the power absorption more precisely in different regions of the semiconductor and calculates the penetration depth of the incident light in the engineered device. The light is incident from the top at an angle normal to the surface. Periodic Boundary

Conditions (PBC) are applied in the lateral directions and Perfect Matching Layers (PML) are applied in the vertical directions. The total power of the light absorbed is calculated throughout the semiconductors and integration is performed for every 50 nm of depth to calculate the power decay against the distance from the surface. Such a process allows for comparing the penetration depth (δ) of the incident light for PDs with different photon-trapping nanoholes ($\delta_{engineered}$) and conventional PDs ($\delta_{conventional}$). The first set of FDTD simulations is performed to understand the penetration depth and the optical generation of carriers when light with wavelengths of 450 nm and 850 nm is injected into the fabricated devices. The next set of optical simulations is used to calculate the penetration depths generated by varying parameters for holes with depths at a fixed wavelength, and when different wavelengths are incident in the photodetector.

6.2.1.2 Device Design and Fabrication

Si PDs are fabricated with a mesa-type structure, where the doping layers are epitaxially grown as a P-I-N structure with a total thickness of 2.5 μm as can be seen in Fig. 6.3. This structure will favor the enhancement of shorter wavelengths, but a similar approach can be implemented on an N-I-P structure for longer wavelengths. Different nanohole designs are implemented in the silicon photodetectors: inverted pyramid, funnel shape, and cylindrical hole. These nanoholes have a diameter (d) of 1000 nm and a periodicity (p) of 1300 nm. The depths of the cylindrical and funnel-shaped holes were measured to be 2 μm and 2.5μm, respectively. For the inverted pyramid hole, the depth was measured to be 0.8 μm, which is calculated by considering the etching angle in silicon of 54.7o w.r.t. the surface, created when KOH is used to etch silicon in the <100> plane.

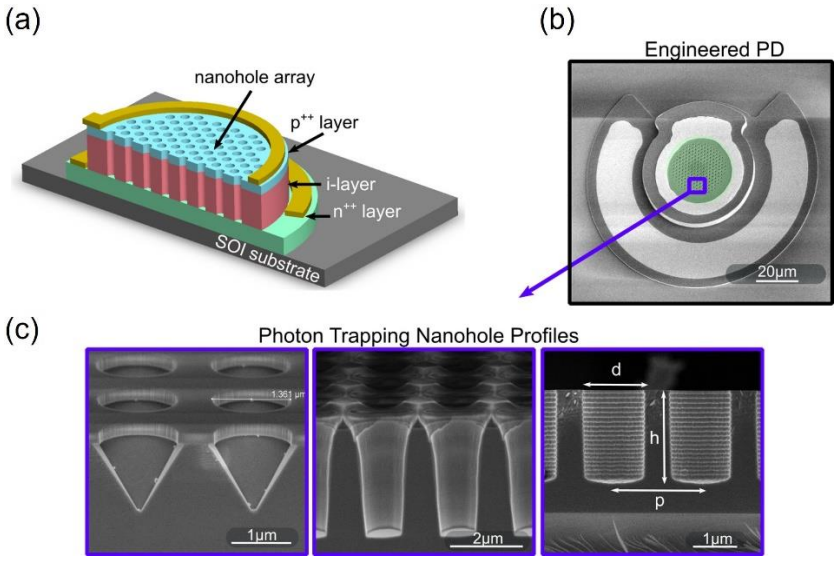


Fig. 6.3. Device design and structure. (a) Schematic of engineered PD with photon trapping nanoholes. (b) SEM of fabricated PD. (c) Different photon trapping nanohole profiles to study the penetration depth and gain.

6.2.2 Results and Discussion

6.2.2.1 Multiplication Gain at Near Infrared (NIR, λ=850 nm)

The implementation of this nanohole profile in the fabricated PDs reduces the reflection from 32% to 17% and enhances the absorption in the 2.5 μm-thickness devices from 8% to 61% as can be seen in fig. 6.4 (a) at an incident (NIR) wavelength of 850 nm. The fabricated devices exhibit a gain factor increase from M = 97.9, in the conventional PD, to a maximum of M= 893 for the engineered PD with the inverted pyramid hole profile, followed by the funnel (M = 770.3) and the cylindrical hole profile (M = 515.2) [fig. 6.4 (e)]. The amount of light absorbed with respect to the thickness of the PD is presented in fig. 6.4 (b). When overlapping the schematic of the doping profile of Fig. 3 (c), it is observed that more light is absorbed in the i-layer (π-layer). The FDTD simulations showed that the penetration depth (δ) of the 850 nm wavelength-light in the inverted pyramid design was reduced from $\delta_{conventional}$ = 18.4 μm to $\delta_{engineered}$ = 2.3 μm [fig. 6.4 (d)]. This nanohole design exhibited higher absorption, shorter penetration depth, and greater maximum gain. The control of the penetration depth, the reduction of reflection, and the increase of

absorption, all collectively increase the gain and allow the fabrication of Si PDs with thinner absorbing layers for high bandwidth operation.

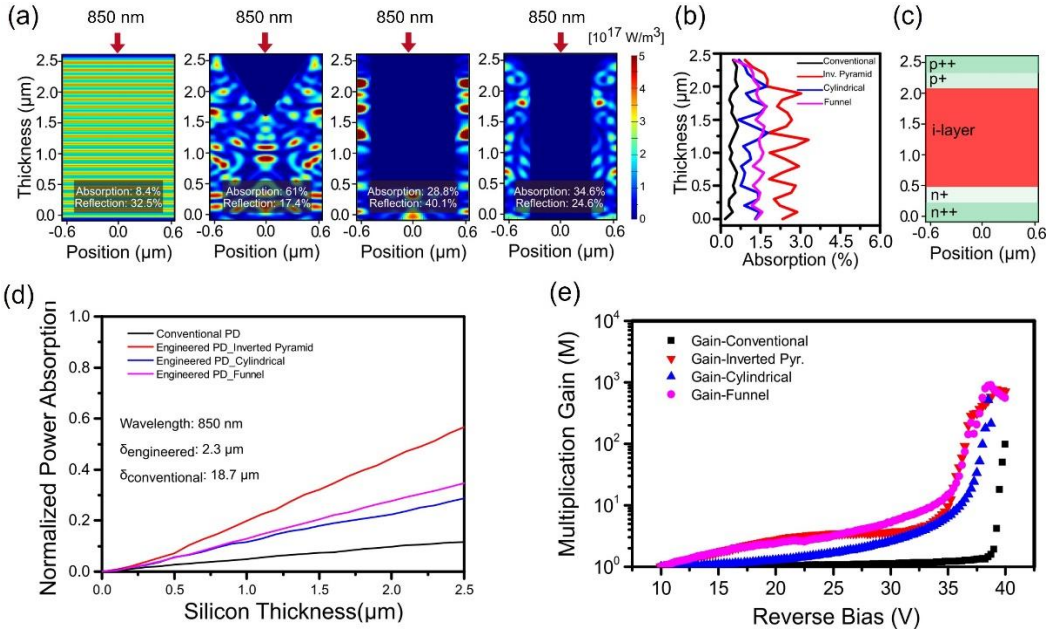


Fig. 6.4. (a) Power absorption of light at 850 nm wavelength in the conventional and engineered PDs with diverse nanohole profiles, simulated by FDTD. (b) Percentage of absorbed light with respect to. the depth. (c) Schematic of the doping profile of the fabricated PD. (d) Comparison of the penetration depth between conventional ($\delta_{conventional}$) and engineered ($\delta_{engineered}$) APDs for 850 nm wavelength. δ is reduced from 18.7 μm to 2.3 μm. (e) Experimental multiplication gain measurements: comparison between conventional PD and engineered PDs with different nanohole profiles.

6.2.2.2 Multiplication Gain at the visible wavelength (λ=450 nm)

The implementation of nanoholes enhances the absorption in silicon from 60% to 83.5%, and a reduction in reflection from 40% to 14% [Fig. 6.5 (a)] at an input visible wavelength of 450 nm. The fabricated conventional (planar) Si PDs exhibited a maximum multiplication gain of 11.9. On the other hand, our engineered PDs present a gain of M = 4707.9 for the cylindrical hole, followed by the funnel-shaped nanohole (M = 3925) and the inverted pyramid (M = 3508.3) as can be seen in Fig. 6.5 (d). FDTD simulations of the PD with cylindrical holes show that the 450 nm-wavelength light penetrates deeper into the semiconductor [Fig. 6.5 (b)], moving from a penetration depth of 0.25 μm in the conventional PD to a maximum of 0.75 μm in the engineered PD with cylindrical nanohole as presented in Fig. 6.5 (c). Contrary to the 850 nm wavelength case, at 450 nm the gain increases in devices with nanohole designs that allow a deeper penetration depth. In addition

to the gain enhancement, Fig. 6.5 (e)-(g) shows the current-voltage characteristics under dark conditions and illumination for a conventional PD [Fig. 6.5 (e)] and for engineered PD-Cylindrical with an input wavelength of 450 nm (f), and 850 nm (g).

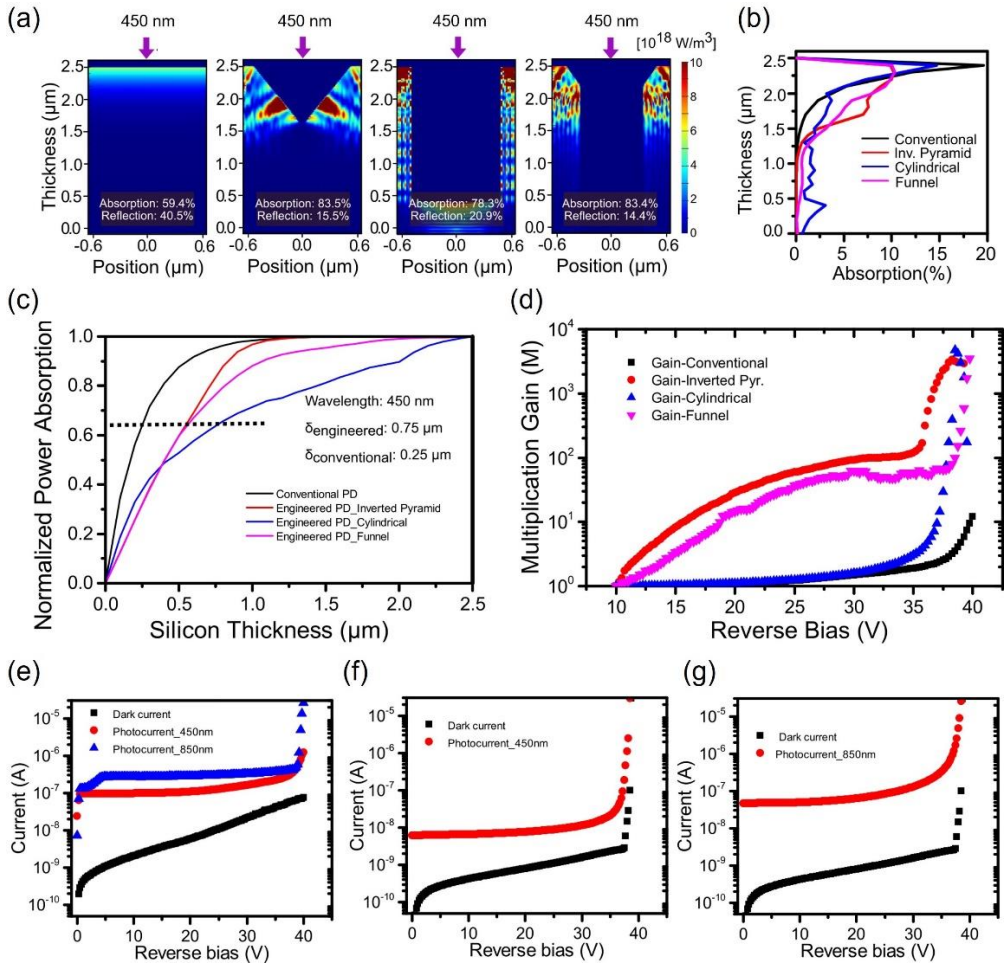


Fig. 6.5. (a) Power absorption of light at 450 nm wavelengths in the conventional and engineered PDs with different nanohole profiles, simulated by FDTD. (b) Percentage of absorbed light with respect to the depth. (c) Comparison of penetration depth between conventional (δconventional) and engineered (δengineered) APD. δ increased from 0.25 μm to 0.75 μm. (d) Experimental multiplication gain measurements comparing conventional PD and engineered PDs. The gain increases by nearly a factor of four hundred, from 11.9 to more than 4000. (e-f) Current-Voltage under dark conditions and illumination for a conventional PD (e), and Engineered PD-Cylindrical with an input light wavelength of 450 nm (f), and 850 nm (g).

We measured the multiplication gain of the fabricated nanostructured silicon APD at 450 nm and 850 nm wavelengths and compared it with a flat silicon APD on the same wafer. Figure 6 shows the multiplication gain in these two devices where we see more than two orders of gain

improvement by proper control of the penetration depth. Moreover, the same structure can perform significantly better in a broad range of wavelengths at low reverse bias voltage as can be seen in Fig. 6.6.

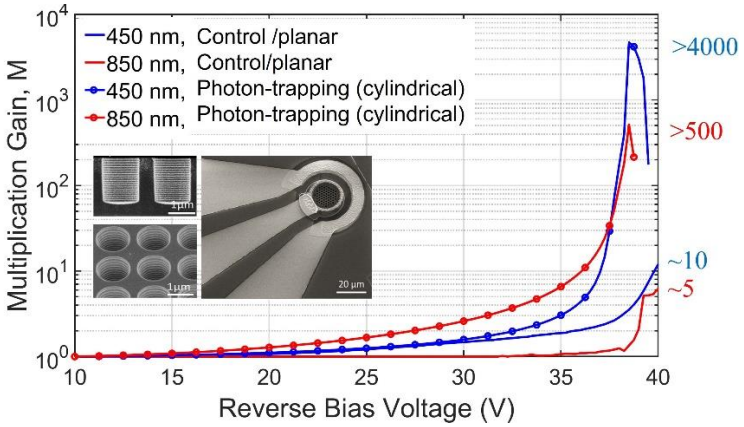


Fig. 6.6. Comparison of multiplication gain between a nanostructured device (cylindrical holes) to a control device at 450 nm and 850 nm wavelengths.

Finally, Table 6.1 summarizes the obtained results with respect to. the penetration depth, gain and External Quantum Efficiency (EQE) obtained in our fabricated devices at 450 nm and 850 nm wavelength light.

	Wavelength (nm)	Conventional	Inverted Pyramid	Cylindrical	Funnel
Penetration depth (μm)	450	0.25	0.55	0.75	0.61
	850	18.7	2.3	>2.5	>2.5
Multiplication Gain (M)	**450**	**11.9**	**3508.3**	**4707.9**	**3925.8**
	850	**97.9**	**893.8**	**515.8**	**770.3**
External Quantum Efficiency (%) for M=1	450	54	82	74	79
	850	14	56	39	42

Table 6.1. Penetration depth, multiplication gain, and EQE in silicon photodetectors with different nanohole profiles. The gain in APDs with photon-trapping holes is measured to be almost 400-fold higher at 450 nm and almost 9-fold higher at 850 nm.

6.2.2.3 Engineering the photon penetration depth at the visible wavelength (λ=450 nm)

A series of simulations have been performed in Si PDs with absorbing layers of only 1.2 μm-thickness to understand the influence of the nanohole depth and incident light wavelengths, in the

penetration depth. By varying the nanohole depth (h) from 0 nm (conventional PD) to 1200 nm, the impact of this parameter on penetration depth is analyzed at the incident wavelength of 450 nm with an incident angle normal to the surface of the device. Cylindrical holes, with 480 nm diameter (d) and 500 nm period (p) are used in this study. The power absorption with respect to depth is calculated for each 50 nm segment along with the depth. Figure 6.7 (a) shows that the penetration depth increases from 0.25 µm in the conventional PD to a maximum of 0.63 µm when cylindrical holes are etched with 1200 nm depth. However, etching the nanoholes can also reduce the absorption and increase the transmission of light, making it necessary to optimize the etching depth. Figure 6.7 (b) shows that this design's maximum absorption and penetration depth is obtained with a nanohole depth of 800 nm where 84% of the light is absorbed and the penetration depth is 0.54 µm.

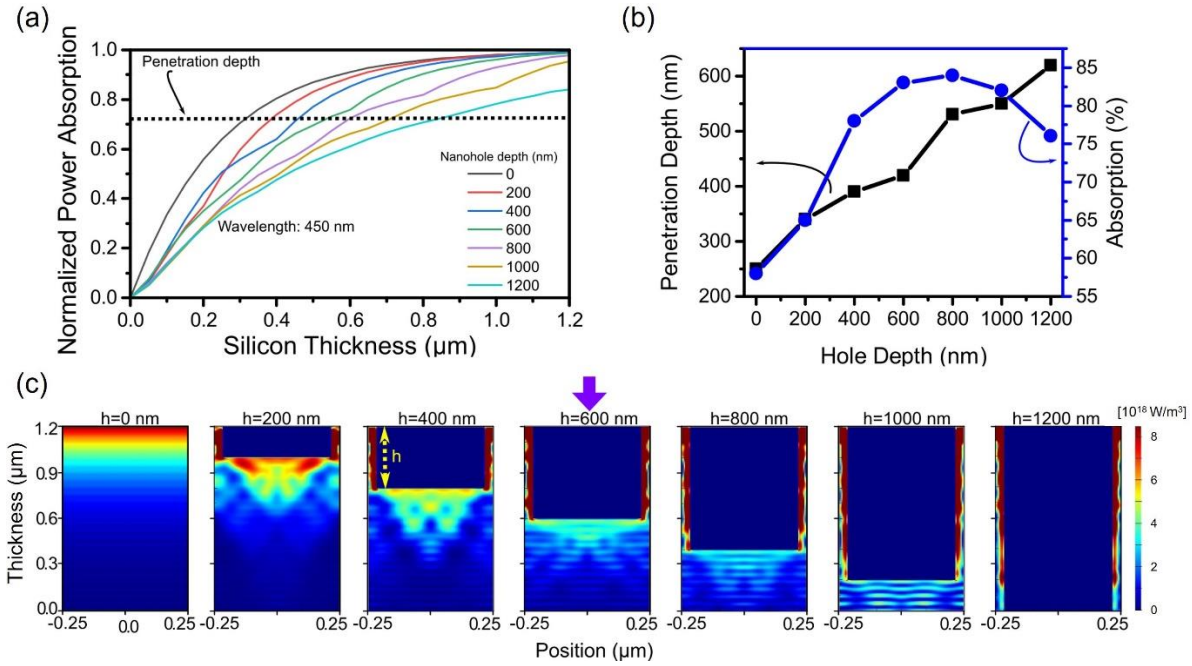


Fig. 6.7. (a) Penetration depth of 450 nm wavelength light in varying photon-trapping nanohole depths. The penetration depth increases with the depth of the hole from 250 nm to 620 nm. (b) Absorption and penetration depth for different hole depths at 450 nm wavelength. A maximum of 84% of absorption can be obtained at 800 nm nanohole depth. (c) Optical absorption profile obtained by FDTD for an incident light of 450 nm.

6.2.2.4 Engineering the photon penetration depth for visible and NIR wavelengths (λ =300-850 nm)

A broad range of applications works in the visible wavelengths, making it important to study the change in penetration depth inside of silicon for different input wavelengths from 300 nm to 850 nm when implementing the nanoholes in silicon. In this section, the nanohole depth is fixed at 400 nm and the diameter and the period are kept unchanged (480 nm diameter and 500 nm period). Figure 6.8 (a) shows the normalized power absorption for different wavelengths in the engineered PD with respect to its thickness. These curves are used to calculate their respective penetration depth. Figure 6.8 (b) compares the penetration depth of conventional devices and the engineered PDs. For wavelengths below 450 nm, our simulations show that a greater penetration depth is achieved [Fig. 6.8 (b), inset]. On the other hand, from 500 nm to 850 nm wavelength, the increase in absorption achieved with nanoholes decreases the penetration depth to a range between 0.55 µm to 2.3 µm. Shorter wavelengths (such as 450 nm) are observed to penetrate deeper into silicon. While photons with longer wavelengths (such as 850 nm) are forced to propagate to shallower depths. Figure 6.8 (c) represents the different distributions of light absorbed in the conventional silicon and engineered PD for 450 nm wavelengths.

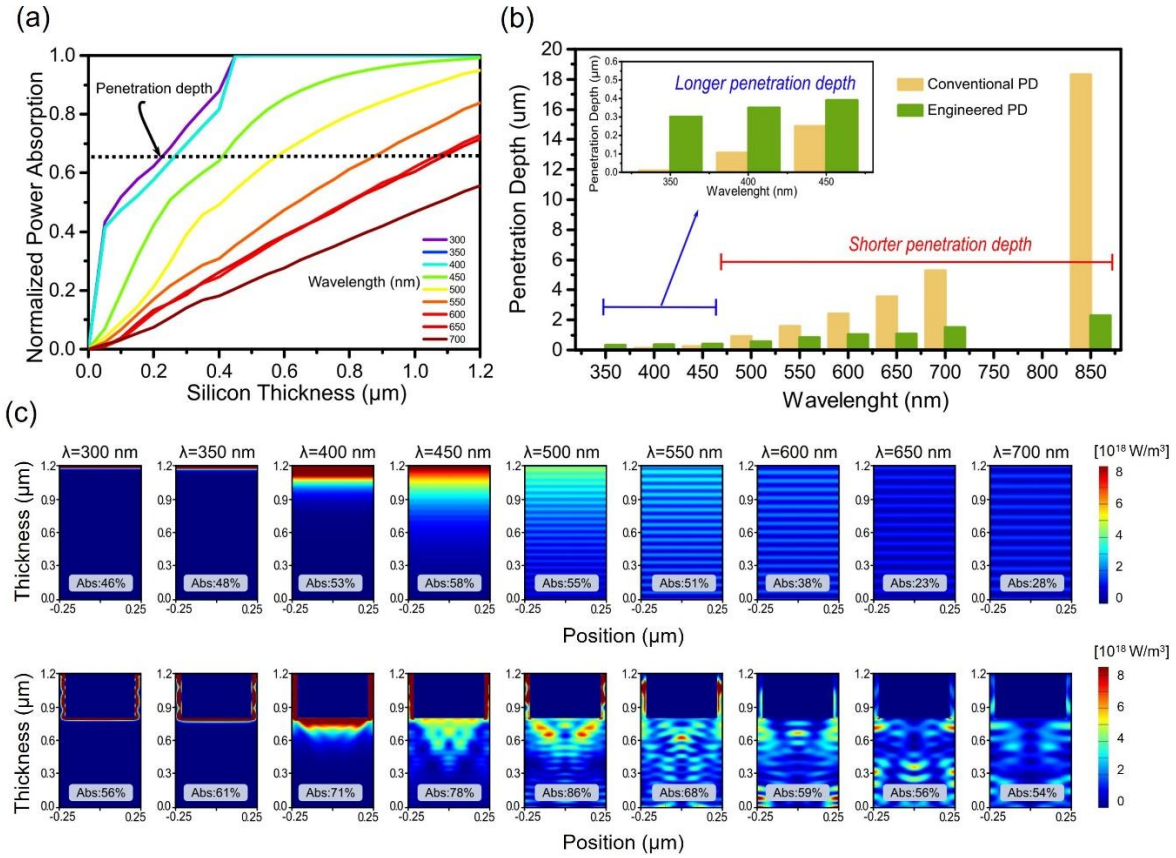


Fig. 6.8. (a) Penetration depth engineered on silicon for incident light wavelengths between 300 nm to 700 nm. (b) Comparison of penetration depth between conventional and engineered PDs. At wavelengths below 450 nm, the penetration depth is dramatically increased, reducing the loss of carriers by recombination, slow diffusion transport, and high excess noise multiplication. Above 500 nm wavelength, the penetration depth is reduced by more than 50%. At 850 nm the penetration depth is reduced from 18.3 μm to only 2.3 μm, an 87% reduction in the depth. (c) The power distribution of incident light at different wavelengths on conventional and photon-trapping photodiodes for nanoholes depth of 400 nm, a diameter of 480 nm, and a period of 500 nm.

6.3 Photon-trapping Si APDs/SPADs for biomedical imaging application

Enhancing photon detection efficiency and time resolution in photodetectors in the entire visible range is critical to improving the image quality of time-of-flight (TOF)-based imaging systems and fluorescence lifetime imaging (FLIM). In this section, we evaluate the gain, detection efficiency, and timing performance of avalanche photodiodes (APD) with photon-trapping nanostructures for photons with 450 nm and 850 nm wavelengths. At 850 nm wavelength, our photon trapping avalanche photodiodes showed 30 times higher gain, an increase from 16% to >60% enhanced

absorption efficiency, and a 50% reduction in the full width at half maximum (FWHM) pulse response time close to the breakdown voltage. At 450 nm wavelength, the external quantum efficiency increased from 54% to 82%, while the gain was enhanced more than 20-fold. Therefore, silicon APDs with photon-trapping structures exhibited a dramatic increase in absorption compared to control devices. Results suggest very thin devices with fast timing properties and high absorption between the near-ultraviolet and the near-infrared (NIR) region can be manufactured for high-speed applications in biomedical imaging. This study paves the way towards obtaining single photon detectors with photon trapping structures with gains above 106 for the entire visible range[3].

6.3.1 Optical/Electrical Simulations, Design and Fabrication

Photon-trapping nanostructures in silicon photodetectors have the potential to promote the initialization of avalanche by electrons, achieve higher multiplication gain values, and reduce the pulse time response, reducing the absorption in the highly doped regions, as illustrated in Fig. 6.8. Photon trapping structures were implemented in silicon photodetectors with 2.5 μm of thickness to study their effect on absorption, gain, and time response. The external quantum efficiency (EQE) and gain were measured at 450 nm and 850 nm wavelengths. Finite difference time domain (FDTD) simulations were used to understand the absorption profile in the semiconductor, while electrical simulations complemented them by studying the electric field profile. We developed a simulation package that allowed us to optimize the design of photon trapping structures to achieve up to 90% of absorption at 450 nm wavelength for a thin silicon layer of 1.2 μm. The combination of these results with an optimized doping profile is expected to contribute to the development of ultra-fast photodetectors with high gain and absorption efficiency.

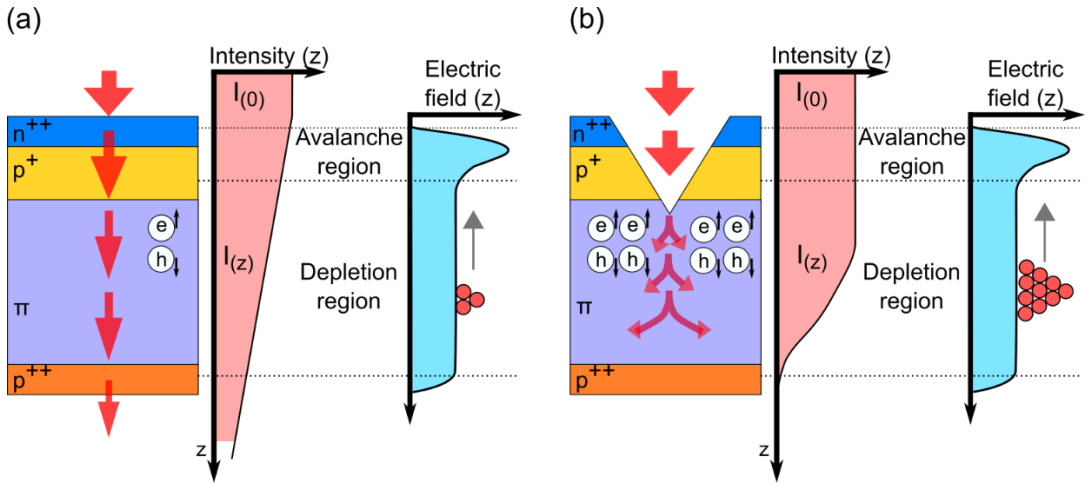


Fig. 6.9. Representation of the absorption and electric field profiles of two APD configurations. (a) Conventional APD (Control), and (b) Photon trapping APD (PT APD).

The simulated absorption profiles of control and PT PD are depicted in Fig. 6.10(a) and (b), respectively. At 850 nm wavelength, the control PD absorption was estimated to be 15%, as most of the input light was transmitted without interacting with the absorbing layer. The photon-trapping device exhibited a distinctly higher absorption of 61% due to the enhanced light-matter interactions. The absorption profile suggests that it is feasible to control the injection of carriers in the avalanche photodetector to achieve higher signal-to-noise (SNR) ratios by increasing the gain and suppressing the excess noise. Figure 3(c) shows the calculated power absorption accumulated over the absorbing layer of the control and the photon trapping PD in steps of 100 nm. The electric field profile corresponding to the doping of the PD demonstrated that the absorbing region was completely depleted [superimposed in Fig. 6 (c)]. A Uniform high electric field over the depleted region ensures an improvement of the amplification factor by raising the impact ionization within the absorbing region.

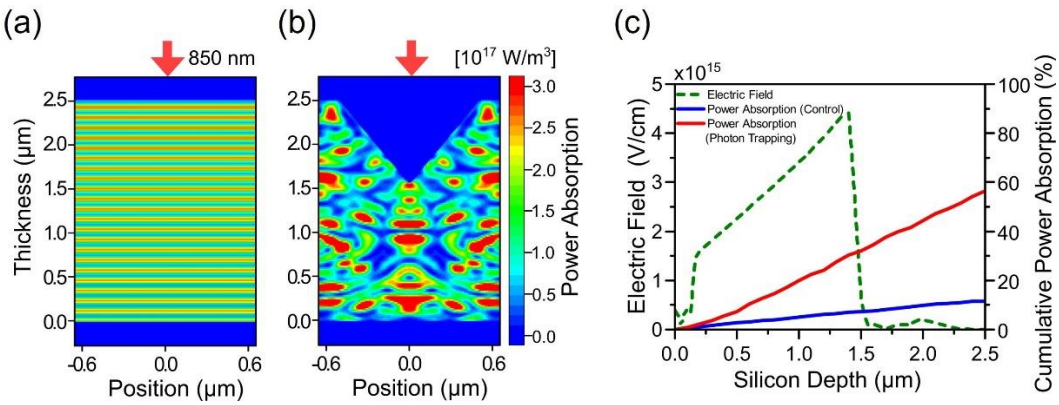


Fig. 6.10. Optical and electrical simulations in Si APD at 850 nm wavelength. Power absorption in (a) control Si PD and (b) PT-silicon PD. (c) Electric field profile of the fabricated device.

A silicon photodetector was fabricated in a mesa-type structure with epitaxial layers grown with a total thickness of 2.5 μm on top of a silicon oxide insulator (SOI) substrate. An array of inverted pyramid holes was etched on the surface of the PD, serving as the photon trapping structures (PT PDs) as shown in Fig. 6.11 (a) [right]. Two PDs with different periodicities (p) and diameters (d) were studied (configuration 1: p/d = 630/900 nm and configuration 2: p/d = 1200/1500 nm). A PD with the same design and without any etched structures was also fabricated as a reference, named the control PD [Fig. 6.11 (a), left]. The doping profile of the silicon PD is described in Fig. 6.11 (b). The doping profile of the fabricated device created a PIN structure. Based on the design considerations, the PIN structure included a 2 μm intrinsic Si layer that was sandwiched between two ultra-thin (~0.25 μm) highly doped n and p layers. However, the i-layer thickness decreased to ~1.5 μm after the growth process due to carrier diffusion from high-doped layers.

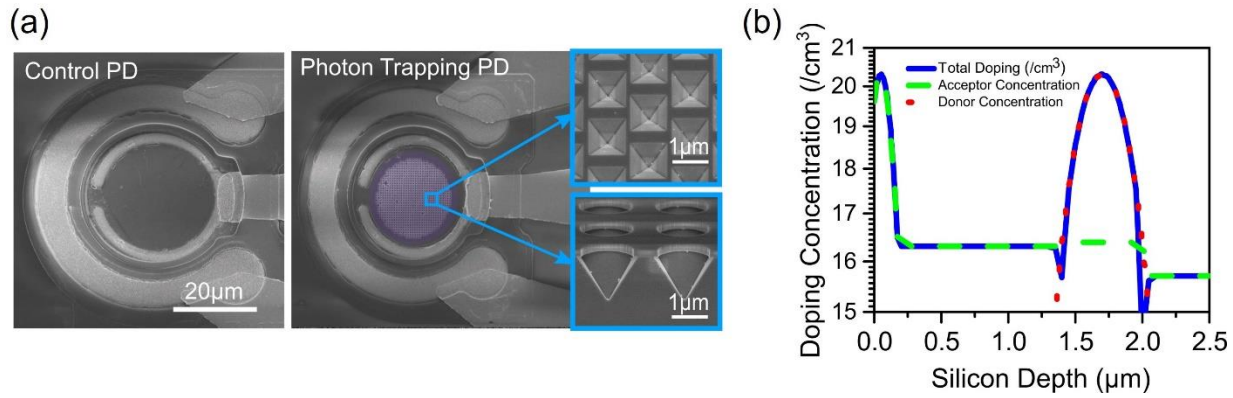


Fig. 6.11. (a) SEM image of control (left) and photon trapping (right) device. (b) The measured doping profile of the photodetectors.

6.3.2 Results and Discussion

6.3.2.1 Experimental gain at NIR (λ=850 nm) for inverted pyramid PT APDs/SPADs

Input light with a power of 8 µW at 850 nm wavelength was delivered to the surface of a photodetector with a diameter of 30 µm. The I-V curves shown in Fig. 6.12 (a) describes a higher current in the photon-trapping avalanche detector which was attributed to the enhanced absorption. The breakdown voltage in the control PD was measured as 34 V, whereas the photon trapping device showed a breakdown voltage at around 30 V. The multiplication gain (M) was calculated as $M = [I_{photo}(V)-I_{dark}(V)]/[I_{photo}(V_{ref})-I_{dark}(V_{ref})]$, where V_{ref} was taken at 10V. Multiple measurements were taken on the different devices on the same wafer, in order to consider the stochastic process of the avalanche process, obtaining a mean value < M > of 14.5 for the control PD and < M > of 554.6 for the photon trapping device [Fig. 6.12 (b)] with a standard deviation of ±0.6 and ±9.6, respectively. From the gain measurements, we can identify the three regimes of operation of these PDs. Up to 10 V the PDs present unity gain and hence considered PIN regime. Above 10 V and below the breakdown voltage, where the gain values increase by the factor M, is considered the APD regime. Above their breakdown voltage, the devices operated in the Geiger mode regime and hence considered single photon avalanche detector (SPAD) mode.

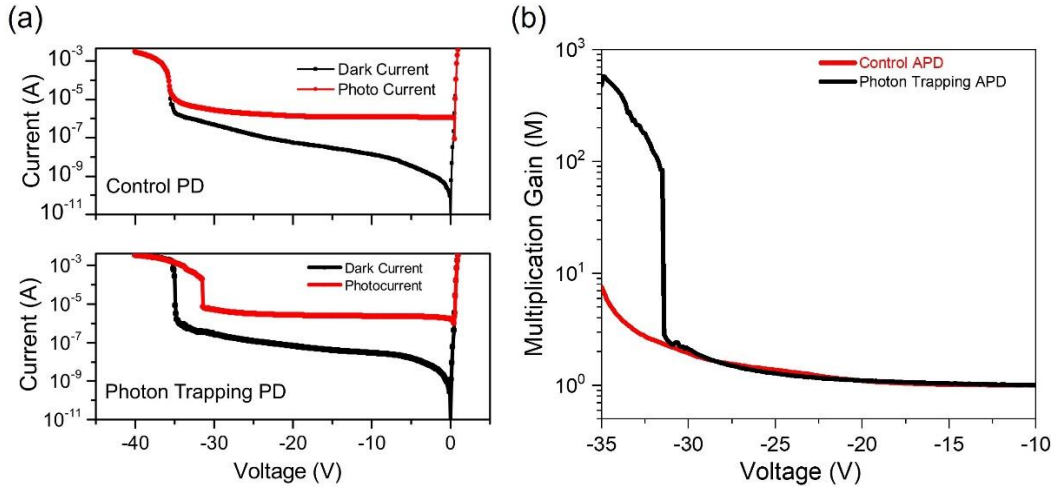


Fig. 6.12. Current-voltage and gain for Si APD. (a) I-V characteristics of control and photon trapping (PT) devices. (b) Multiplication gains of PT and control device.

6.3.2.2 Experimental gain at NIR (λ=450 nm) for inverted pyramid PT APDs/SPADs

In conventional silicon PD with a thickness of 2.5 µm, 60% of the light is absorbed, mostly close to the surface, while the remaining 40% is reflected. The implementation of the photon trapping structures reduces the reflection to 14% and the remaining 86% is absorbed [Fig. 6.13 (b)]. In addition to the higher absorption capabilities of photon-trapping silicon PDs, the multiplication gain was measured in the APDs with a laser diode emitting at 450 nm wavelength and a power of 30 µW. The bias voltage was swept from 1 to −34 V, in steps of 100 mV, for the devices with 30 µm diameter, to obtain the dark current and the photocurrent and calculate its gain. The control PD exhibited a gain of 24, while the PT PDs exhibited a gain factor of 157 and 524, for the 630 nm and 1300 nm diameter structures, respectively [Fig. 6.13 (c)]. The difference in gain observed can be attributed to the different light penetration depths in the PDs. While in the control PD the 450 nm-wavelength light is absorbed close to the surface, the deeper PT structure increased the penetration length, affecting the probability of electrons and holes generating an avalanche. The breakdown voltage also varies in the three devices. The PT PDs exhibit a breakdown voltage of 26–27 V, while the control PD required a voltage of 28 V. The variation in the breakdown voltage can be explained by the smaller net volume of the PT PD.

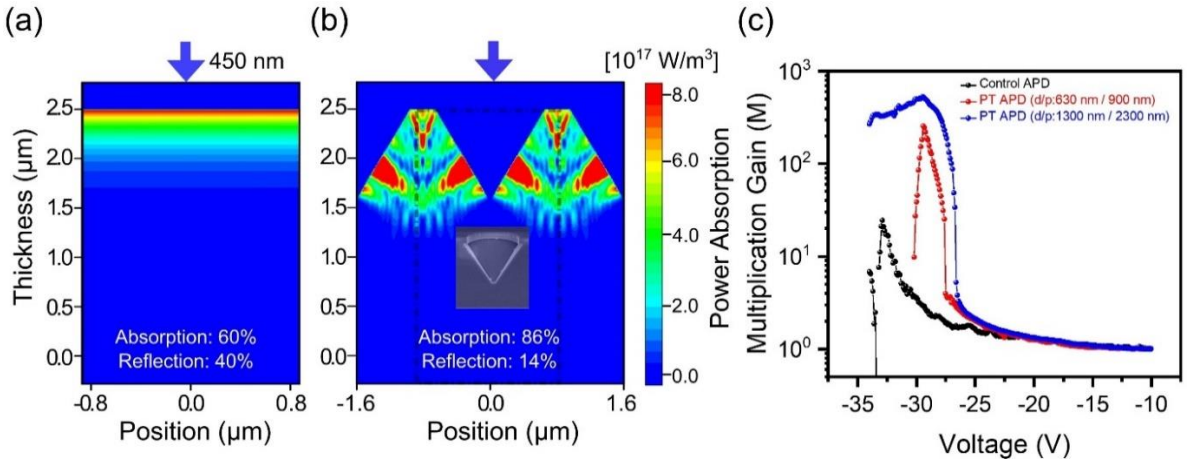


Fig. 6.13. FDTD simulations of 2.5 µm-thick APDs with input light of 450 nm for (a) a control APD and (b) a photon-trapping APD. The inset figure is an SEM image. (c) Experimental gain measurements of fabricated devices at 450 nm wavelength.

6.3.2.3 Designing Photon-trapping Single Photon APD (PT SPADs) at λ=450 nm

Optical and electrical simulations were performed to optimize the design of photon trapping structures, with the aim to design Single Photon Avalanche Photodetectors (PT SPADs) that could enable ultrafast operation in the shorter wavelengths (λ= 450 nm) of the visible range without compromising their sensitivity. A thin silicon thickness of 1.2 µm was chosen to achieve low jitter time. A conventional device (control) with such a thin layer would be able to absorb only 51% of optical power at 450 nm wavelength, with most of the light being absorbed in the first 300 nm of depth, as FDTD simulations show in fig. 6.14 (a). However, our results suggest that more than 90% of photon absorption can be achieved in such a thin layer with optimized photon-trapping structures when a proper diameter and period are implemented in the photodetectors. Figure 6.14 (b) shows the side and top view of the simulated PT SPAD suggesting a shift in the absorption with an enhancement peak at 400 nm depth just below the depth of the nanoholes. Herein, we have studied the impact of design variations in period, diameter, and depth of cylindrical holes through FDTD simulation.

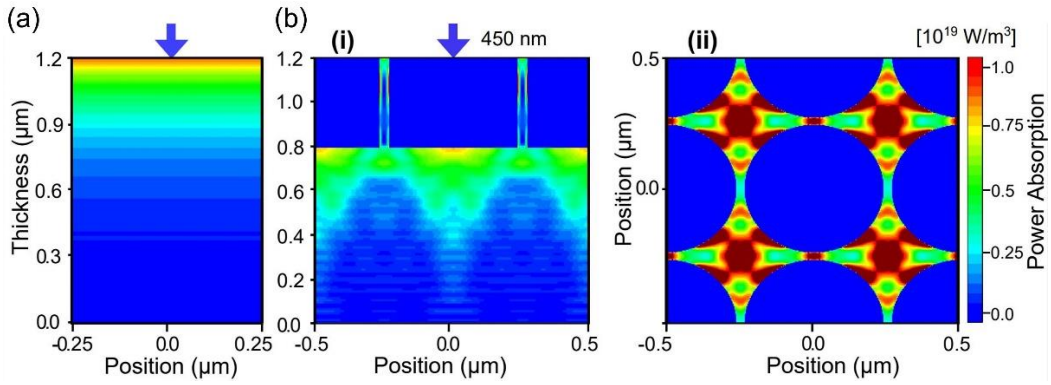


Fig. 6.14. Absorption control in photon trapping PD at 450 nm wavelength. Simulated power absorption profile of (a) control and (b) photon trapping PD with 1.2 µm thick silicon. Our photon-trapping PDs with such a thin absorber layer exhibit more than 90% absorption.

Such simulations allowed us to construct fig. 6.15 (a), where the expected absorption for different diameters and periods, with a depth of 400 nm is presented. As observed in fig. 6.15 (a), the absorption efficiency shows a higher enhancement when the diameter of PT nanoholes approaches the period length between them, with a maximum of 90% absorption. Figure 6.15 (b) shows the cumulative absorption obtained for the control (blue) and the PT-SPAD device (red), in steps of 50 nm. In the first 100 nm depth, the high absorption observed in the control PD is reduced to almost 50%. Then, between the 400 nm and 500 nm depth, the absorption of power in a PT SPAD is increased by 3 times, compared with the control SPAD. This illustrates a reduction in optical power absorption close to the surface with the enhancement of absorption deeper in the device. With a proper electric field profile (green) that allows to separate the absorption and the multiplication regions, more electrons can be injected into the multiplication region, promoting higher gain and lower amplification noise [Fig. 6.15 (b)]. The higher absorption efficiency achieved in the silicon-photon trapping APDs at visible and near-infrared wavelengths allows the designing of devices with thinner absorption layers. Such a reduction in thickness comes with a reduction of the breakdown voltage[3, 4]. The breakdown voltage of our fabricated device with 2.5 µm of thickness is around 30 V and electrical simulations performed on the device proposed with 1.2 µm of thickness, suggest a breakdown voltage of less than 20 V. We envision a reduced voltage below 10 V as a possibility in our devices with a thinner active layer.

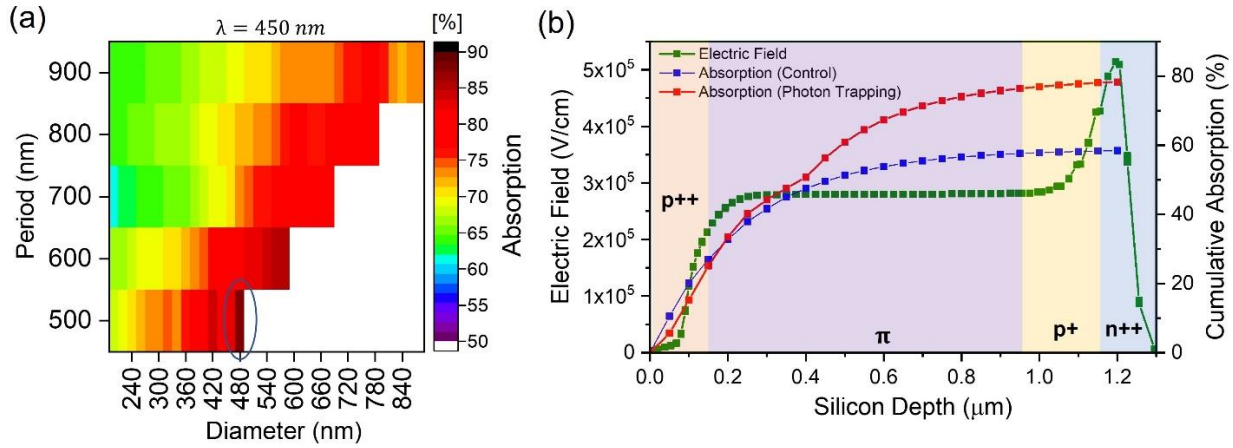


Fig. 6.15. (a) Influence of period and diameter of the photon trapping nanostructures in power absorption at 450 nm wavelength. (d) Cumulative absorption in control (blue) and PT (red) silicon SPAD. Overlap of electric field profile of a PD with a pπpn structure with the absorption of light for optical generation, for higher gain and lower noise avalanche-based PD.

An advantage of our photon trapping structures with respect to other absorption enhancement methods is its effect across a broad range of wavelengths, critical for biomedical imaging technologies [Figs. 6.16 (a), and (b)]. Figure 6.16 (a) shows the higher absorption obtained in photodetectors with photon-trapping structures from 400 nm to 800 nm. At 450 nm wavelength, the absorption increases as the hole diameter of the structure reach close to the period within the structures. Diverse photon-trapping structures can also be implemented, such as inverted pyramids or cylindrical holes. The simulated absorption of these structures reveals a higher absorption in the inverted pyramid profile from 400 nm to 600 nm wavelength [Fig. 6.16 (b)]. In addition, in this range of wavelengths, a more constant absorption value is observed in the inverted pyramid structure. Engineering photon-trapping structures in semiconductor-based photodetectors can benefit many biomedical applications that rely on the detection of optical photons with a broad distribution of wavelengths.

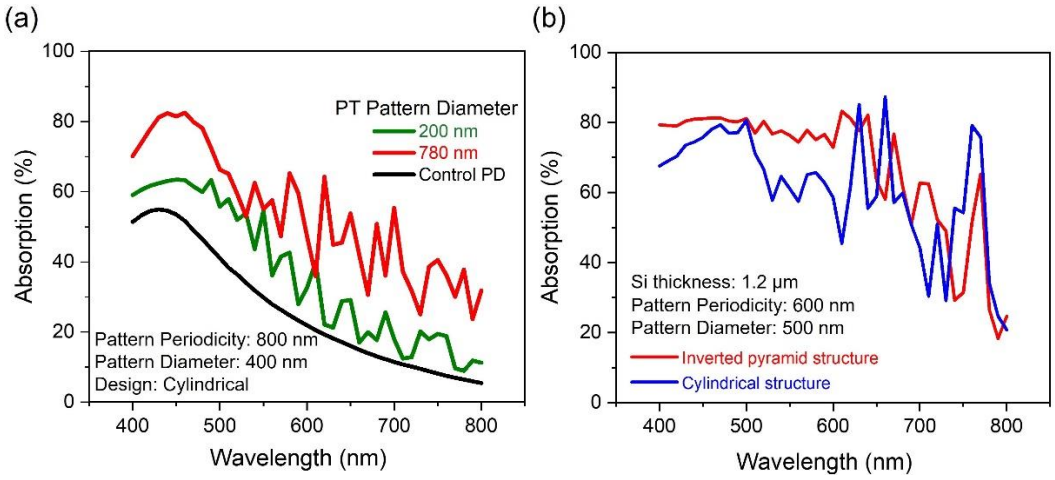


Fig. 6.16. (a) Influence of diameter in cylindrical photon trapping structure at a broadband range of wavelengths. (b) Comparison of absorption at a broadband range of wavelengths between cylindrical and inverted pyramid structure.

6.3.2.4 High-speed Characterization of the Si Photon-trapping (PT) APD/SPAD

The time response of the control and PT PDs was measured with a pico-second pulsed laser with 850 nm wavelength at the 3 regimens of operation: PIN (brown), APD (green) and SPAD (red) as can be seen in Fig. 6.17. At 35 V, the SPAD regime, PT PDs exhibited a decrease in the FWHM from 99 ps to 40 ps, as well as a faster decay (fall time) from 293 ps to 105 ps of the pulse response compared to the control PD. This can be attributed to the efficient delivery of the input light to the high electric field regions and a decrease of absorption in the highly doped regions, where diffusion is the dominant carrier transport method. Most of the photons absorbed in the doped n and p regions of the photodiodes do not contribute to the photocurrents or EQE due to a lack of electric field in the highly doped p–n contact regions. A small fraction of photogenerated carriers in the photodiode contact regions are collected by the external circuit via the carrier diffusion process and contribute to the overall EQE. For an illumination wavelength of 850 nm, ~1% of the light is absorbed in the top p region. However, when the top contact layer is thinned down from 200 nm to 100 nm, the percentage of absorbed light in the device's intrinsic region would increase by around 10% at shorter wavelengths such as 450 nm. Further thinning the top contact would augment the sheet resistance, contributing negatively to the bandwidth. We emphasize that the PT devices can inhibit surface reflection, absorb most photons, and exhibit reduced capacitance, contributing to higher absorption efficiency and high bandwidth.

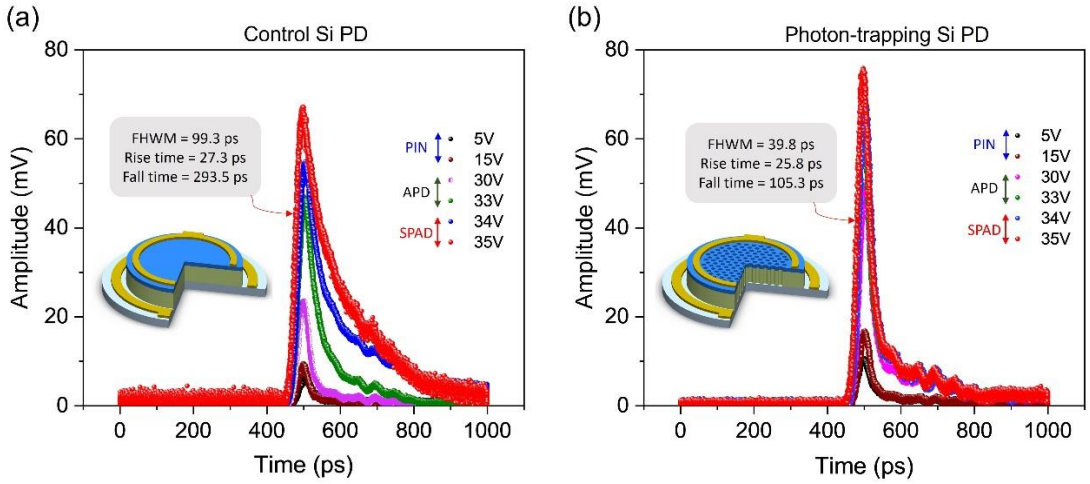


Fig. 6.17. Pulse time response for Si PD under the three regimes of operation PIN (brown) APD (green) and SPAD (red), for the (a) control and (b) Photon Trapping PD.

These devices also allow penetration of light to a much deeper level to maximize the gain, which is especially important for illumination with short wavelengths such as 450 nm. Junction capacitance and junction resistance, which form the device RC time constant, as well as the photogenerated carriers' transient time, are the main speed limiting factors in PDs. Photon-trapping structures offer a solution to reduce the junction capacitance that depends on the device area and the depletion layer thickness. They could improve the absorption coefficient of the absorbing layer up to seven times [5] at 850 nm, therefore, designing a small-area device with similar absorption to large-area flat devices is feasible. Moreover, we have demonstrated that our photon-trapping structures can reduce the capacitance by more than 50% due to the reduction of the surface area of the device [6]. Transient time can be improved by employing thin highly doped contact layers (n++ and p++ layers) that facilitate the generated fast carriers' transition to the outer circuit elements and reduce the slow carriers effect on device response.

6.4 Photon-trapping Si APDs/SPADs for LiDAR

Light trapping nanostructures implemented in silicon photodetectors demonstrate more than 500% improvement of quantum efficiency at 905nm wavelength, enabling their implementation for short-range, high-resolution, and low-cost light detection and ranging (LIDAR) systems, required in new data-driven applications such as robotics, augmented reality (AR), virtual reality (VR), agriculture and manufacturing. In these emerging applications, the cost, resolution, and power consumption of LIDAR systems are more critical parameters, and for that reason operating at a wavelength of 905 nm is more suitable than operating at 1550 nm. The use of silicon and the increase of sensitivity of photodetectors can allow using lower power levels of light while keeping the low cost due to the mature fabrication capabilities on silicon platforms in Si CMOS foundries.

6.4.1 Design, Results, and Discussion

6.4.1.1 Device Design

PIN silicon photodetector on an SOI substrate is fabricated using, where a 2 μm intrinsic layer is located between a p+ and n+ layer with 0.2 μm of thickness [fig. 6.18 (a)]. Photon trapping structures are funnel shape etched with a diameter of 800 nm and placed in a hexagonal lattice and a pattern periodicity of 1050 nm. Another photodetector is fabricated without any array of trapping structures and is used as a control device for comparison purposes.

6.4.1.2 Results and Discussion

6.4.1.2.1 Enhanced External Quantum Efficiency (EQE)

Figure. 6.18 (b) presents the EQE that is enhanced over the NIR spectrum (λ= 800-1100 nm). Particularly, at 905 nm where LIDAR systems operate, the Quantum efficiency is enhanced by employing photon-trapping nanoholes from 7.6% to 44.1% with a thin Si-absorbing 2 μm layer. This enhancement is achieved without an increase of the intrinsic layer that would reduce the time response of the photodetector, thus breaking the typical trade-off between sensitivity and bandwidth in photodetectors.

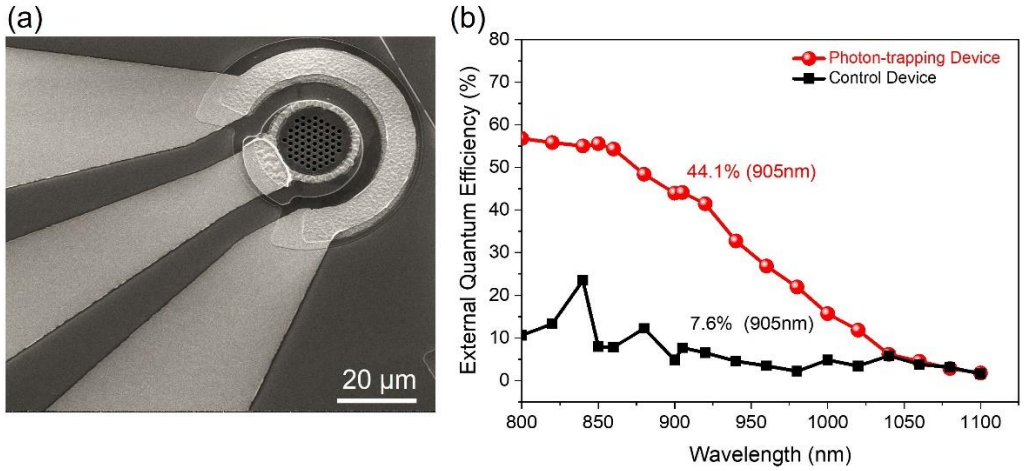


Fig. 6.18. (a) SEM image of photon-trapping PD. (b) EQE enhancement of PT PD at 905 nm, shows an EQE of 44.1% while the control device only presents 7.6%.

6.4.1.2.2 Time Response Enhancement, and Power Consumption Reduction in PT PD

The time response of the PD is measured at -10V in a PD with 80 μm of diameter. We have used a pulsed laser at 850 nm and with an input power of 10 μW, using a sampling scope with 20GHz

sampling capabilities. The full width half maximum (FWHM) of the output pulse response is measured as 51 ps while the FWHM is considerably lower than our control device which shows 113 ps as can be seen in fig. 6.19 (a). This reduction in the FWHM can be attributed to the reduction of the junction capacitance, obtained by the removal of material on the surface of the device.

Using the range equation for LIDAR as described in [7], made it possible to measure the distance range that these new photodetectors can potentially measure. The enhancement of quantum efficiency and different noise sources are considered, as well as beam propagation and reflectivity of the surface. Figure 6.19 (b) serves to illustrate the increment of distance measurement that a LIDAR can achieve with these new photodetectors. Hence, with the enhancement of quantum efficiency and high speed of operation, the range equation shows that LIDAR systems with lower light power levels and high resolution can be developed and massively implemented in areas such as robotics, AR, VR, agriculture, and manufacturing.

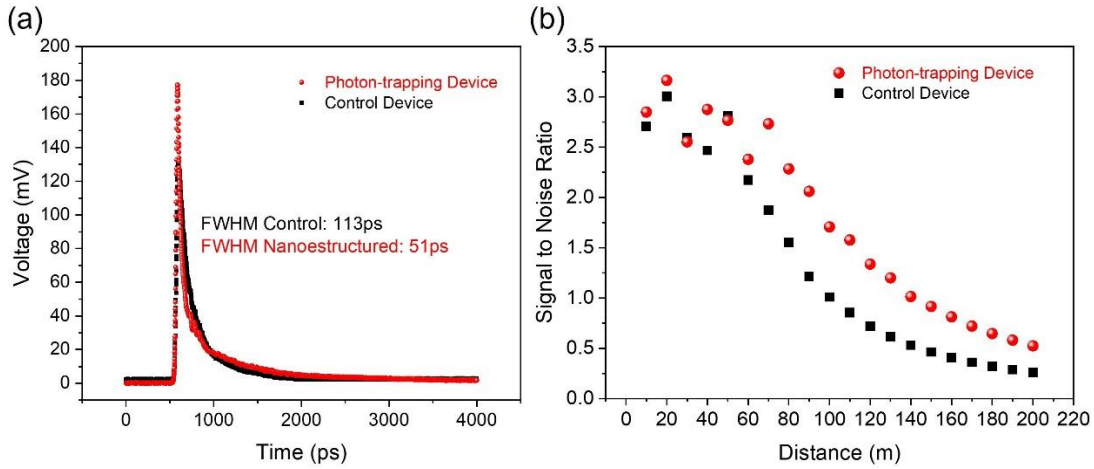


Fig. 6.19. (a) Pulse response of PT PD and control PD with 80 μm PD's diameter. The FWHM is reduced from 113 ps to 51 ps. (b) Calculation of Signal to Noise Ratio with respect to the distance of a LIDAR system, considering the enhancement of EQE. Lower laser power is required to measure the same distance as a system with control PD.

6.5 Design and fabrication of high-efficiency, low-power, and low-leak Si-avalanche photodiode (APD)

In this section, we designed a sub-10V Si-APD device using the ATLAS Silvaco TCAD simulation platform. In alignment with the designed doping profile, we epitaxially grow the APD stack on a silicon-on-insulator (SOI) wafer and fabricated the Si-APD device structures. To enhance the absorption efficiency in the device, we introduced photon-trapping micro-holes (PTMH) into the device. Finally, we present a detailed direct-current (DC) current-voltage (IV) characterization of the devices for a range of illumination wavelengths. We show an exceptionally low off-state current. Additionally, we show a tremendous increase in the quantum efficiency of the device by introducing the photon-trapping holes. We also show a drastic change in the multiplication gain with the illuminated laser power. Further, we show that control devices (without PTMH) are sensitive to the illumination direction which is significantly mitigated by introducing the PTMH. A low reverse-biased current, a sub-10V breakdown voltage, enhanced wavelength absorption, and CMOS compatibility of these Si-APD devices have the potential to detect ultra-low photon counts and can revolutionize the on-chip CMOS integration of the photonic devices.

6.5.1 Si APD Designs Integrated with Photon-trapping Micro-holes (PTMH)

An APD doping profile consists of a p^{++} (n^{++}) contact layer followed by an intrinsic π-layer and a p^{+}/n^{++} (n^{+}/p^{++}) multiplication junction is presented in fig. 6.20 (a). The thickness of the π-layer controls the fundamental limit of photon absorption efficiency in the device and the parasitic. The doping contrast at the p^{+}/n^{++} multiplication junction regulates the breakdown voltage of the APD. A demonstration of $e^{-} - h^{+}$ pair generation due to the illumination and multiplication of the generated carriers due to the high electric field is shown in fig. 6.20 (b). We engineered the APD doping profile to manipulate the electric field profile at the multiplication junction to trigger a low-voltage impact ionization (i.e., a low-voltage avalanche breakdown). The electric field (EF) required for Si to break down is $\sim 3 \times 10^{5}$V/cm [8, 9].

We simulate two doping variants for the APD (Case 1 and Case 2) to compare the EF profile at the multiplication junction. Figure. 6.20 (b) shows a 2D contour plot and a 1D cutline (extracted at the black dotted line) comparing the doping profiles in both Case 1 and Case 2 APDs. The doping contrast at the multiplication junction of Case 2 APD is sharper as compared to Case 1 APD. A 2D contour plot of the EF profile in Case 1 and a comparison of the EF profiles in both cases are shown in Fig. 6.20 (c). An increased doping contrast in Case 2 results in an increased EF at the multiplication junction. This increased EF translates to an early trigger of impact ionization (II) and avalanche breakdown. Finally, we have generated I-V profiles in both cases by enabling (blue trend) and disabling (black trend) the impact ionization (II) physics model in the simulation framework. A direct correlation between increased EF and reduced breakdown voltage is shown in Fig. 6.20 (d). It is to be noted that, the purpose of the simulation exercise is to estimate the breakdown voltage. Therefore, we have simulated the APD device structures under ideal conditions (i.e., there are no surface state traps present.)

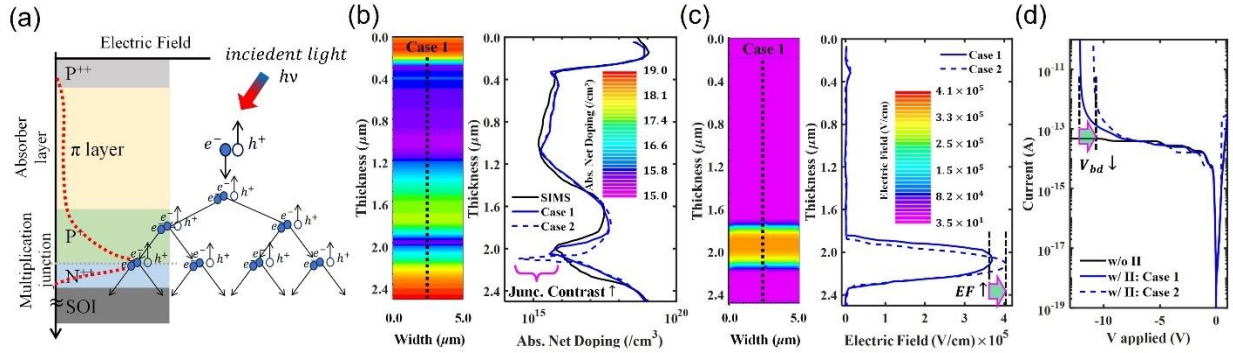


Fig. 6.20. (a) Schematic of the doping stack, an electric field profile, and a visual demonstration of the avalanche phenomenon in avalanche photodiodes. (b) Simulated 2D Contour plot of the doping profile for Case 1 and 1D Doping profile extracted at the black dotted cutline. In the 1D plot, the Case 1 doping scenario is compared against the Case 2 doping variant and the SIMS doping profile of the epitaxially grown APD stack used for the APD fabrication. The doping contrast at the multiplication junction is engineered to trigger an early impact ionization followed by an early avalanche breakdown. (c) A 2D Contour plot of the electric field profile in Case 1 Si-APD device, and a 1D electric field profile extracted at the black dotted cutline. The EF profile in Case 1 doping scenario is compared against that of in Case 2, to show an increase in the EF with an increase in the doping contract at the multiplication junction. (d) Simulated current-voltage of the Si-APD of the avalanche breakdown. An increase in the electric field at the multiplication junction results in a reduced breakdown voltage.

6.5.2 Si APD Fabrication Process

We epitaxially grew Si APD stack on an SOI wafer in alignment with the optimized doping profile. A secondary ion mass spectrometry (SIMS) imaging of the epitaxially grown stack doping profile of the device's layers is presented in Fig. 6.21 (b). Si APD fabrication process scheme is shown in fig. 6.21. The optical micrograph of the fabricated devices is shown in Fig. 6.22 (a). The die consists of devices with diameters varying from 25-500 µm. The diameter and the periodicity of the PTMH vary from 600–1500 nm and 900–3000 nm respectively. Inset of Fig. 6.22(a) shows a microscopic image of the devices with varying PTMH diameter and periodicity selectively reflecting certain wavelengths from the microscopic white light. Figure 6.22 (b) shows an enlarged 500 µm size device with PTMH, a 150× magnified microscopic image, and the inset showing a scanning electron microscopic (SEM) image of the PTMH array.

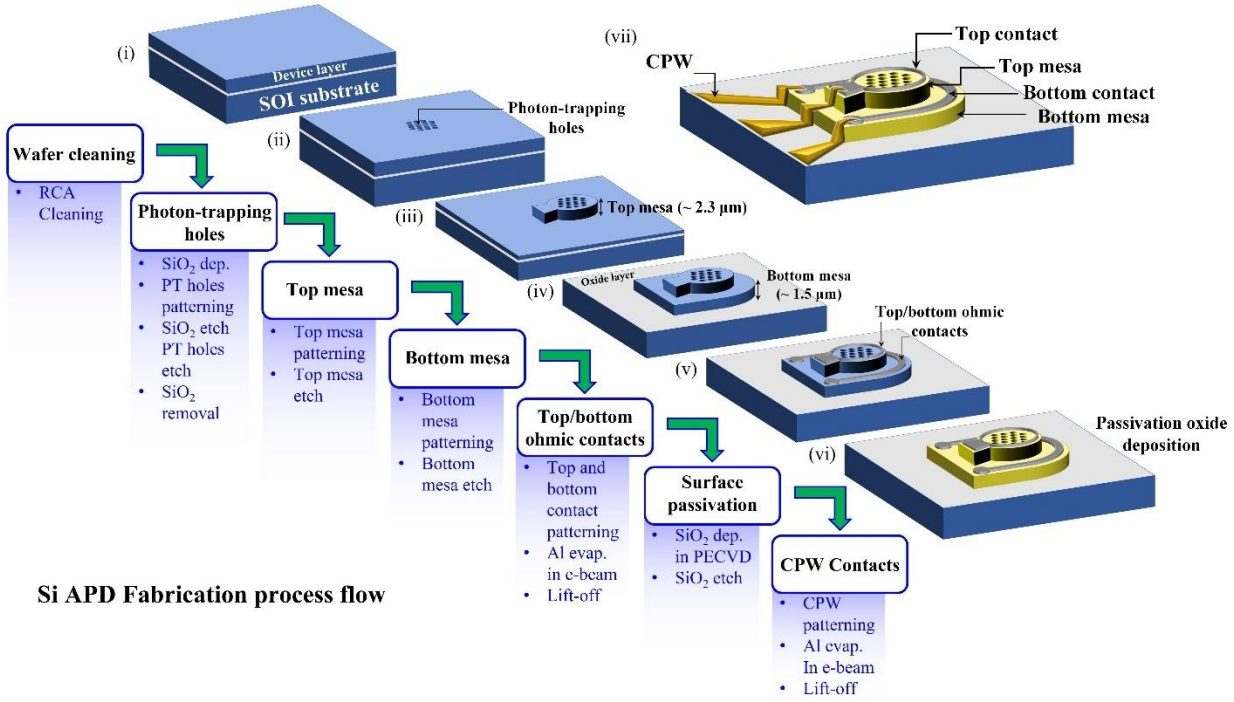


Fig. 6.21. CMOS-compatible fabrication processes are used to fabricate Si-APD devices. The photon-trapping micro-holes (PTMH) are patterned using Stepper optical lithography system. The mesa and the PTMH surfaces are passivated using SiO_2 coating to reduce the off-state leakage current. A coplanar-waveguide (CPW) is incorporated for the characterizing high-speed performance of the Si APD.

6.5.3 Results and Discussion

6.5.3.1 Current-voltage Characteristics

Figure. 6.22 (c) presents Si APD IV characterization for PTMH (device diameter = 500 µm; PTMH diameter = 600 nm; periodicity = 900 nm). A low reverse-biased current and an eventual impact-ionization-induced breakdown represent the APD characteristics. The inset of the figure plots a linear scale IV profile in the dark and under illumination. The wavelength sweep varies from 640 nm to 1100 nm. The laser power is maintained at 10 µW during the entire wavelength sweep. A gradual decrease in the current with an increase in the wavelength is accredited to the reduced absorption coefficient at longer wavelengths in silicon. Aligned with the expectation, the Si-APD shows a sub-10V breakdown (~ 8.0 V). Figure. 6.22 (d) presents the multiplication gain (M) of the APD at 1 µW and 10 µW laser power for 850 nm illumination wavelength. The multiplication gain is calculated at unity gain voltage ($V_{M=1} = -1$ V) and using $M = (I_{photo} - I_{dark})/(I_{photo}(V_{M=1}) - I_{dark}(V_{M=1}))$ expression [10]. The gain, M increases rigorously with reduced laser power. An enormous amount of $e^- - h^+$ pair generation at a high laser power causes excessive carrier-carrier scattering which results in a compromised carrier multiplication. A significant increase in the M at low laser power makes these APDs suitable for low-photon detection applications. The inset of Fig. 6.22 (d) shows the gain versus wavelength trend calculated from Fig. 6.22 (c). A reduced carrier-carrier scattering resulting from a reduced generation has resulted in an enormous increase in the gain at longer wavelengths.

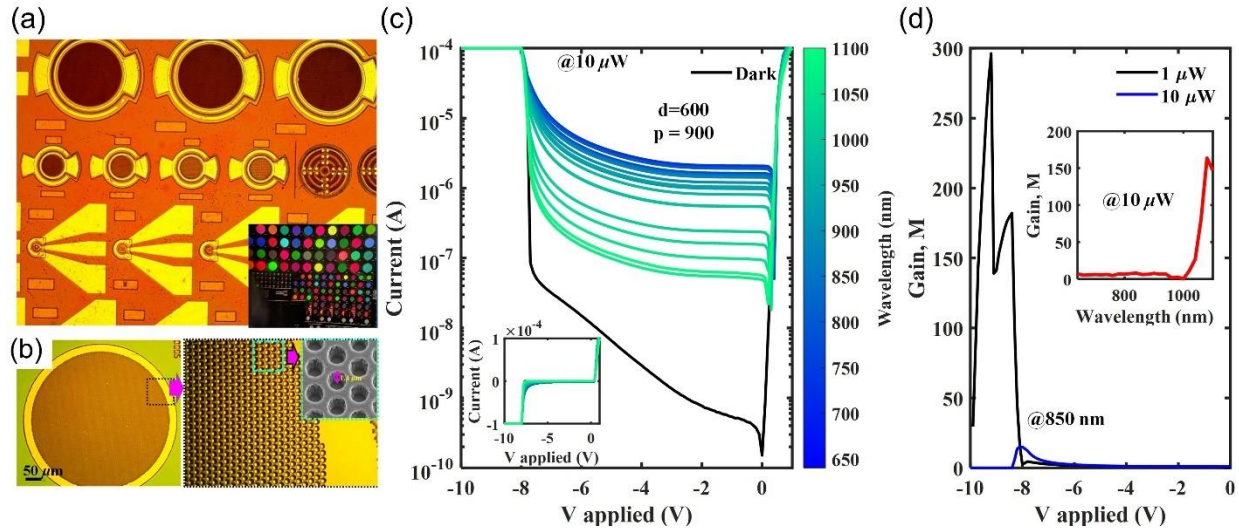


Fig. 6.22. (a) Micrograph image of the fabricated Si APDs, the inset shows a microscopic image captured while illuminating the white light over the die shows a variation of light reflection response. (b) Microscopic image of the zoomed hexagonal lattice photon-trapping design, the inset shows an SEM image of PTMH. (c) The dark and illumination DC I-V characteristics measured (at a fixed laser power = 10 μW) for with-PTMH Si-APD (d = 600 nm; p = 900 nm), the inset shows the linear result. (d) The multiplication gains in the device extracted at -1 V unity gain voltage. The multiplication gain increases at lower illumination power due to a reduced carrier-carrier scattering. The inset in (d) shows the M extracted from (c) as a function of illumination wavelength. A rapid increase in the gain at longer wavelengths is attributed to reduced carrier-carrier scattering due to low carrier generation.

6.5.3.2 EQE enhancement with Photon-trapping Micro-holes (PTMH)

Figure. 6.23 (a) presents the dark current of control (planar) Si APDs with device diameters ranging from 500-25 μm. The dark current at pre-breakdown bias scales from 20 nA to 30 pA with the diameter scaling. The 25 μm and 50 μm diameter devices show dark currents as low as ~30 pA which is expected to reduce further as the dark current is reaching the systemic noise floor. Figure. 6.23 (b) shows the impact of PTMH on the dark current and flat APD dark current is included for comparison purposes. Due to surface passivation, the impact of PTMH-induced surface states is negligible on the dark current and an equivalent dark current of ~30 pA is achieved even after introducing the PTMH array.

We show a comparison of the external quantum efficiency (EQE) for a flat device (without PTMH) against the device with PTMH in fig. 6.23 (c). A hexagonal lattice arrangement for the PTMH array is considered (PTMH diameter = 600 nm; periodicity = 900 nm) as shown in the inset of fig. 6.23

(c). The flat device shows a maximum of 25% EQE (black curve) at 700 nm wavelength and drops rapidly at longer wavelengths. We observe an oscillatory pattern in the EQE of the flat device. The oscillation EQE is due to the resonance of certain wavelengths in the Si active layer sandwiched between the air and the SiO_2 as Air/Si/SiO_2 where SiO_2 layer act as a back reflector [11]. As the refractive index of Si (n_{Si}) is greater than that of the air (n_{air}) and the SiO_2 (n_{SiO2}), i.e., $n_{air} < n_{Si} > n_{SiO2}$ which causes cavity effect[11]. Due to this cavity effect, certain wavelengths get trapped in the Si and result in enhanced EQE. Thereafter, we show ~ 5× enhancement in the EQE at 850 nm with the introduction of PTMH. The PTMH works as a waveguide and allows lateral propagation by bending the light almost 90°[3, 5, 6, 10, 12]. This bending can be attributed to the diffraction of incident light at the corners and edges of the PTMH as the feature size of the holes are comparable to that of the illumination wavelength.36 Lateral propagation of the incident light increases the path length of the light inside the absorber layer, therefore, increases the absorption.

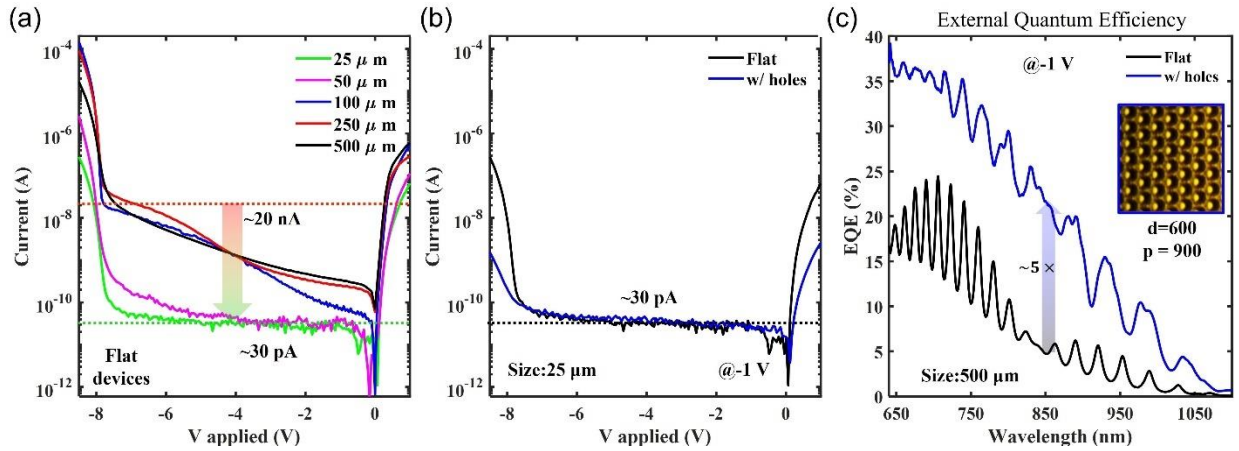


Fig. 6.23. (a) Dark current of the flat APD device with device diameter scaling. The dark current scales aptly with the device size. (b) Impact of PTMH on the dark current of 25 μW size device. The SiO_2 -based dangling bond passivation reduces the surface state and results in comparable dark current in both flat and with-PTMH devices. (c) The EQE shows ~5× enhancement by introducing the PTMH structures into the flat device.

6.5.3.3 EQE Incidence Angle Dependency

In this section, we have investigated the angle of incidence sensitivity on the EQE. Figure. 6.24 (a) demonstrates the path-length change from l_1 to l_2 for $\theta_{i,1}$ and $\theta_{i,2}$ angles of incidence. The

presence of PTMH creates a perturbation in the EM wave travel path and disrupts the resonance phenomenon as shown in Fig. 6.24 (b).

We measured the EQE of a flat device at 45° and 30° angles of incidence. Figure 6.25 (a-b) show EQE trends for a flat device. We observe prominent oscillation in both cases due to the resonance at certain wavelengths. The wavelengths that satisfy Equation 6.1 result in standing wave formation, i.e., undergo resonance [13].

$$\lambda_n = \frac{2l_n}{n} \ (where\ n = 1, 2, 3, \dots) \tag{6.1}$$

$$l_m = path - length = \frac{T_{Si}}{\cos(\theta_{i,m})} \ (where\ n = 1, 2, 3, \dots)$$

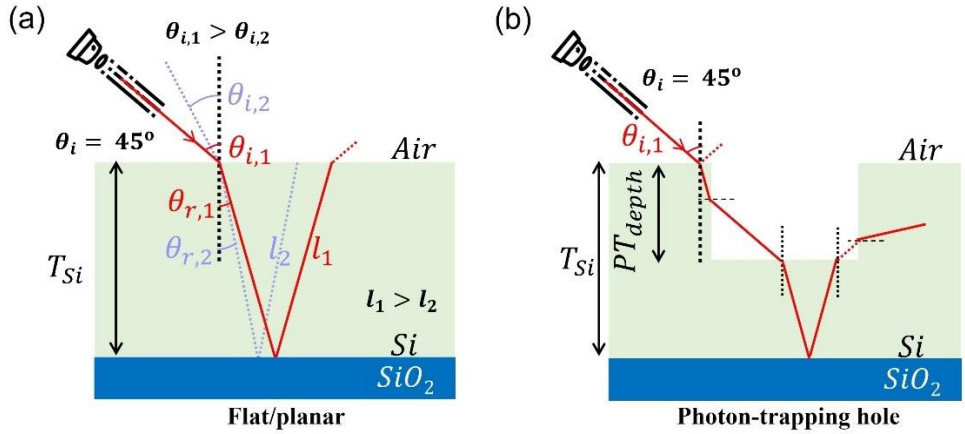


Fig. 6.24. (a) shows a schematic of the EM wave refraction while entering the Si region bounded by air and SiO_2 at two different angles of incidence ($\theta_{i,1}$>$\theta_{i,2}$) to show path-length modulation (l_1>l_2). This path-length modulation leads to a systematic shift in the oscillatory ΔEQE profile as shown in the inset of 6.23 (b). (b) The presence of PTMH perturbs the smooth resonance process and results in the dilution of oscillations and prominent incidence angle dependency as highlighted in the inset of 6.23(d)

The estimated wavelength points expected to show resonance are calculated using Equation 6.1 and are plotted in Fig. 6.25 (a) and (b) using asterisks (*). The inset of Fig. 6.25 (b) plots the ΔEQE highlighting a systematic right shift in the oscillating EQE profile with angles of incidence change from 45° to 30°. Figure 6.25 (c) and (d) show the EQE profile of a with-PTMH device 45° and 30° angles of incidence. The systematic shift in the oscillating EQE profile present in the flat device has been diluted with the introduction of PTMH. The ΔEQE profiles at both 45° and 30° angles of incidence for with-PTMH device is shown in the inset of Fig. 6.25 (d). The prominent shift that was

evident in the ΔEQE of the flat devices is indistinguishable in the with-PTMH device. A significant drop in the EQE in flat device for 30° angle of incidence near 700 nm wavelength (marked with a green dotted line in Fig. 6.25 (b)) has a residual effect on the EQE of with-PTMH device as well (marked in Fig. 6.25 (d) with a green dotted line). Adding PTMH interrupts the resonance phenomenon and resolves the incidence angle dependency of the EQE profile.

The presented device shows an avalanche breakdown at ~8.0 V. The introduction of the PTMH array results 5× enhancement in the EQE superseding the fundamental absorption limit of 0.8 µm thick π-layer (Calculated as ~5% [14]). The EQE of the device is compared against the literature at a fixed illumination wavelength of 850 nm. A proportionate reduction in the EQE from 39% to 22.5 % is due to a significant reduction in the π-layer thickness from 2.0 µm to 0.8 µm. Finally, we have compared the multiplication gain (M) of the device. The multiplication gain is comparable to table 6.1 at 850 nm wavelength, whereas the P_{off} shows tremendous improvement from 2.8 µW/mm^2 to 0.41 µW/mm^2. Overall device performance shows notable improvement in comparison to state-of-the-art literature.

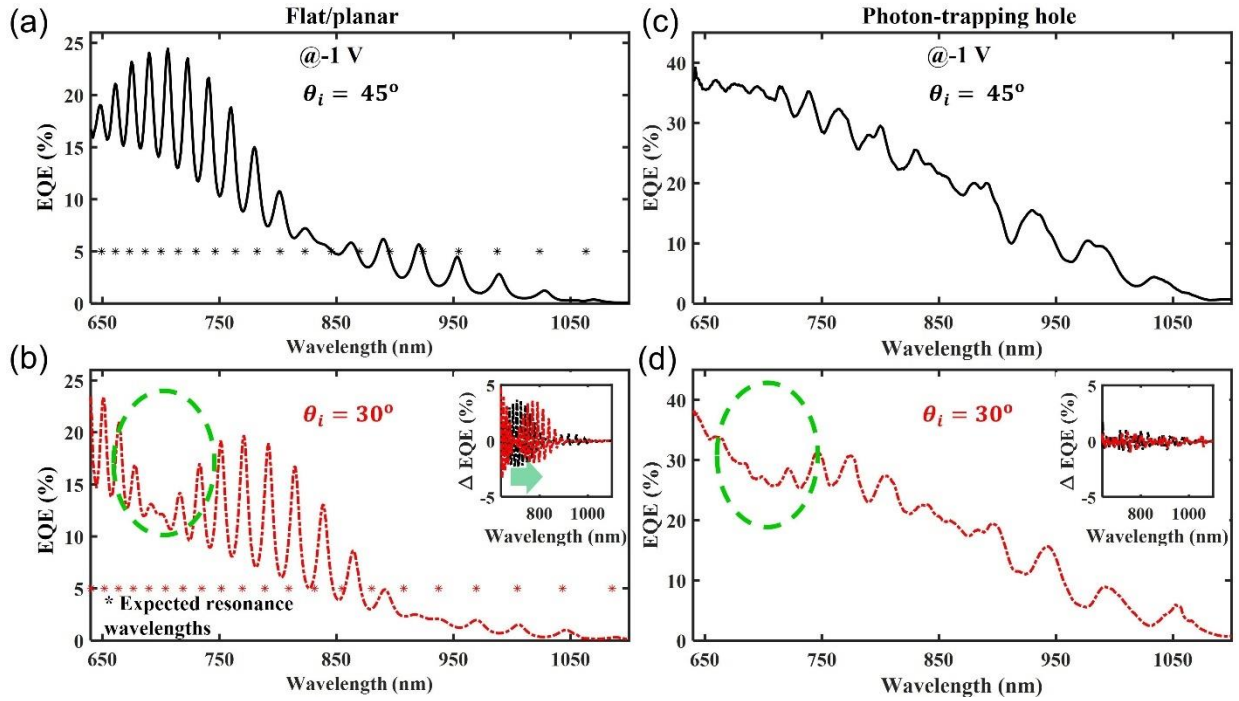


Fig. 6.25. The EQE profile as a function of wavelength captured at 45° and 30° angle of incidences of the laser used to illuminate the flat and with-PTMH devices. (a-b) Shows oscillatory EQE profile captured

for the flat device and the asterisks in (a) and (b) marking the possible resonance wavelengths mathematically calculated for 45^{o} and 30^{o} incidence angles. The EQE of the device with PTMH at (c) 45^{o} (d) 30^{o} angles of incidence. The presence of PTMH perturbs the smooth resonance process as shown in fig. 6.22 (b) results in the dilution of oscillations and prominent incidence angle dependency as highlighted in the inset of (d). The drop in the EQE near the 700 nm wavelength range in (d) marked with a green dotted line is a residual effect of the prominent drop present near the 700 nm wavelength in (b) as marked.

6.6 Computational Imaging and Spectroscopy on-chip Enabled by Photon-trapping Si APDs

Optical spectrometers are widely used scientific equipment with many applications involving material characterization, chemical analysis, disease diagnostics, surveillance, etc. Emerging applications in biomedical and communication fields have boosted research in the miniaturization of spectrometers[15]. Recently, reconstruction-based spectrometers have gained popularity for their compact size, easy maneuverability, and versatile utility. These devices exploit the superior computational capabilities of recent computers to reconstruct hyperspectral images using detectors with distinct responsivity to different wavelengths. In this section, we present CMOS-compatible reconstruction-based on-chip spectrometer pixels capable of spectrally resolving the visible spectrum with 1 nm spectral resolution maintaining high accuracy (>95 %) and low footprint (8 μm × 8 μm), all without the use of any additional filters. A single spectrometer pixel is formed by an array of silicon photodiodes, each having a distinct absorption spectrum due to their integrated nanostructures, this allows us to computationally reconstruct the hyperspectral image. To achieve distinct responsivity, we utilize optimized photon-trapping nanostructures photodiodes with different dimensions and shapes that modify the coupling of light at different wavelengths which can reflect a unique response footprint. This also reduces the spectrometer pixel footprint (comparable to conventional camera pixels), thus improving spatial resolution. This miniaturized spectrometer can be utilized for real-time in-situ biomedical applications such as Fluorescence Lifetime Imaging Microscopy (FLIM), pulse oximetry, disease diagnostics, and surgical guidance[16].

6.6.1 Unique Optical Responses Enabled by Photon-trapping Si APD

Photon-trapping nanostructures are basically integrated nanoholes or nanopillars embedded on top of the active layer of the detectors that can modulate the light-matter interaction. These subwavelength structures can interact with light and change their propagation direction from a vertical orientation to a lateral orientation by allowing only lateral propagation modes to exist in the semiconductor. Since light interacts with mostly subwavelength structures, we can design nanostructures with distinct sizes and shapes such that they would interact differently with different wavelengths. Thus, this allows us to create photodiodes that would have unique responsivity to light over a specific wavelength range.

6.6.2 Photon-trapping Si APD Training Process

First, we need to characterize our Si photodiodes and learn their behaviors in response to different illumination conditions. Therefore, we need to obtain photon-trapping Si APDs (with a variety of optimized designs) quantum efficiency over the visible spectrum from 400 nm to 1100 nm wavelength range and record the estimated photocurrent of the detectors. The recorded photocurrent is assigned for every specific photodiode in the wavelength range and the input light spectrum. For the training sample, the peak amplitudes varied from 400 nm to 1100 nm, and the ranges are measured in Full-Width-Half-Maximum (FWHM). These training data were selected as we are focusing on biomedical applications (400-700 nm) which deal with spectrally broader signals in the visible wavelength spectrum.

6.6.3 Reconstruction Process

When the light of an unknown spectrum is illuminated onto the reconstruction-based spectrometer, the different photodiodes generate different photocurrent amplitudes that are recorded by the device. These photocurrents are then reconstructed using the known photocurrent outputs that were previously recorded during the training procedure of the device. So, we calculate the linear coefficient of the known photocurrent samples by matrix multiplication.

Then, these linear coefficients are used to estimate the unknown input light spectrum by multiplying them to the known light spectra. The reconstruction process is illustrated in Fig. 6.26.

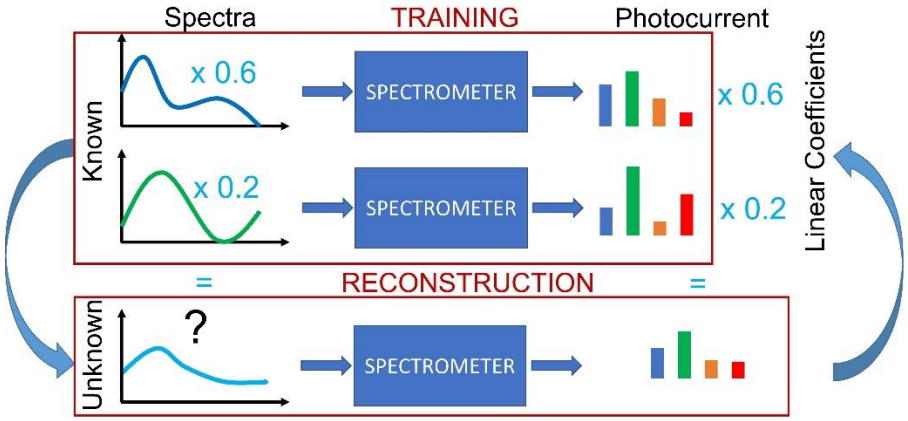


Fig. 6.26. Demonstration of a reconstruction algorithm for our detector-only spectrometer. We train our spectrometer with known spectra and record their respective photocurrent. The output photocurrent from an unknown spectrum is used to find the linear coefficients of the known photocurrent using matrix multiplication techniques. The same coefficients are then used to estimate the unknown spectrum by multiplying the known spectra with the linear coefficients.

6.6.4 Spectral Response Engineering using Nanostructures

We use Lumerical FDTD simulations to optimize the optical absorption of a variety of photon-trapping designs that varied in nanohole diameter (d) and periodicity (p). Figure. 6.27 shows the absorption spectra for a silicon photodiode with an integrated hole structure with varying diameters and periodicity ranging from 350 nm to 600 nm at 50 nm intervals. For a fixed periodicity, larger hole diameters have higher hole density allowing fewer vertical modes of propagation, this improves the coupling ratio of the guided lateral modes and thus the increase in absorption. However, to maintain enough silicon between the holes for adequate absorption, we keep a minimum hole-to-hole separation of 100 nm. When the hole diameter and periodicity are of the same order as the wavelength, we observe higher lateral modes of propagation with a few vertical modes. So, we observe absorption peaks at the circulated regions. This way, we can engineer higher absorption at desired wavelengths. Hence, we can now design micro/nanohole arrays to enhance absorption at specific wavelengths, allowing us to engineer unique absorption features.

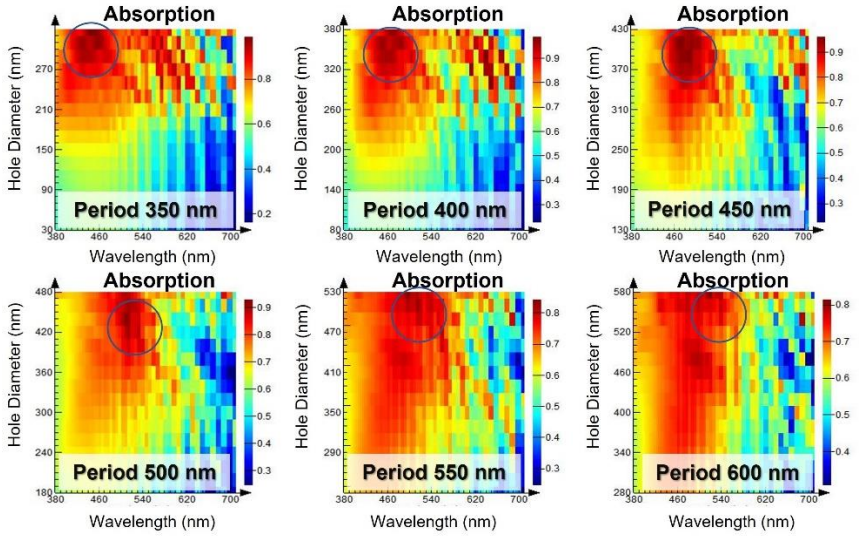


Fig. 6.27. FDTD simulations for optimizing photon-trapping design (diameter, and periods) vs. incident wavelengths. The highest optical absorption is circulated.

Next, we used FDTD simulations to generate the quantum efficiencies of the photodiodes with different nanostructures and superimposed them with the experimentally measured EQE as shown in fig. 6.28. Here the quantum efficiencies are demonstrated for the respective nanostructured photodiodes over a wavelength range from 450 nm to 1050 nm. As can be seen in Fig. 6.28, the darker color bar indicates the higher quantum efficiency which offers an optimization road map (PT patterns) for creating a unique optical response. The top view of the respective nanostructured photodiode is shown in the inset of each subfigure. The results show that photon-trapping nanostructure parameters such as (diameter/periodicity) can modulate the light propagation and thus impact their quantum efficiencies. Most of the profiles have a similar pattern arising from the intrinsic absorption characteristics of silicon. However, the nanostructures contribute to peaks and valleys at different wavelengths which help to create the distinctive features of the photodiodes necessary for reconstruction-based spectroscopy. The uniqueness of these profiles generally contributes to a better performance in the reconstruction-based spectrometer. Increasing hole diameter leads to an increase in the absorption for fixed periodicity (Coupling to lateral mode increases). While absorption peaks at different wavelengths when the

periodicity and hole diameter are close to the incident wavelengths. One important thing to note is that the maximum quantum efficiency achieved in such photodiodes is about 80% over the wavelength range from 400 nm to 700 nm. It is expected as the rest of the light is mostly reflected from the top surface of the detector. The transmittance is low for shorter wavelengths, and it increases with increasing wavelengths as observed in any conventional silicon photodiode. This explains the quantum efficiency dropping off at longer wavelengths.

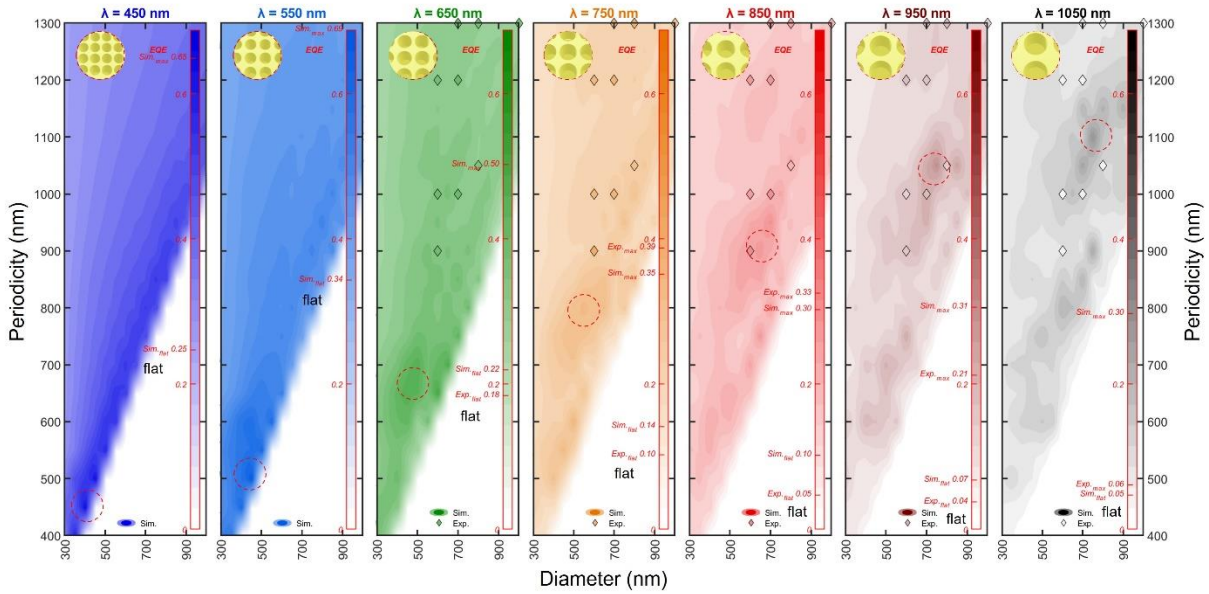


Fig. 6.27. Spectral response engineering utilized by PT nanostructures (calculated EQE and experimentally measured)

Figure. 6.28 shows SEM images of the fabricated photon-trapping designs such as cylindrical holes, funnel holes, and inverted pyramids (diameter (d)/periodicity (p)). These structures are patterned in a square and hexagonal lattice fashioned. The optical responses of such designs varied according to the incident of the wavelength which offers unique and wavelength-selective silicon avalanche photodiodes with controlled wide spectral gain by integrating photon-trapping microstructures. Chapter 4 discusses the fabricated designs and their responses.

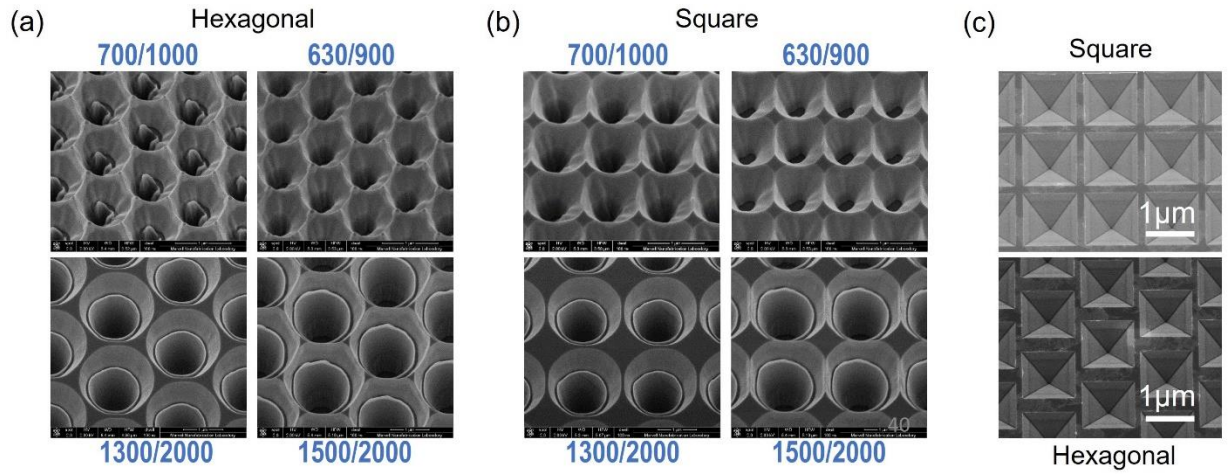


Fig. 6.28. SEM of the nanohole array etched in Silicon APD. (a) Funnel holes in a hexagonal pattern (diameter (d/p) periodicity). (b) Funnel holes in a square pattern. (c) Inverted pyramid in a square and a hexagonal pattern.

Different fabricated dimensions of photon-trapping holes create unique responsivity in the absorption spectra can be seen in Fig. 6.29 (a). Photon-trapping hole diameters were kept at 1000 nm while PT periodicity varied from 1300 nm to 3000 nm. The EQE experimental results show the unique responsivity features of our fabricated devices generated due to different PT hole structures with a thin absorbing layer ~ 1 μm. The major benefit of this approach is that it does not involve complicated material growth or hybrid integration. Moreover, we can monolithically integrate the structures in a single tape-out with CMOS compatibility.

Fig. 6.29 (b) shows a microscopic image of the devices with varying PT diameter and periodicity selectively reflecting certain wavelengths from the white microscopic light. This preferential reflection of certain wavelengths from the devices has the potential to devise an on-chip spectrometer.

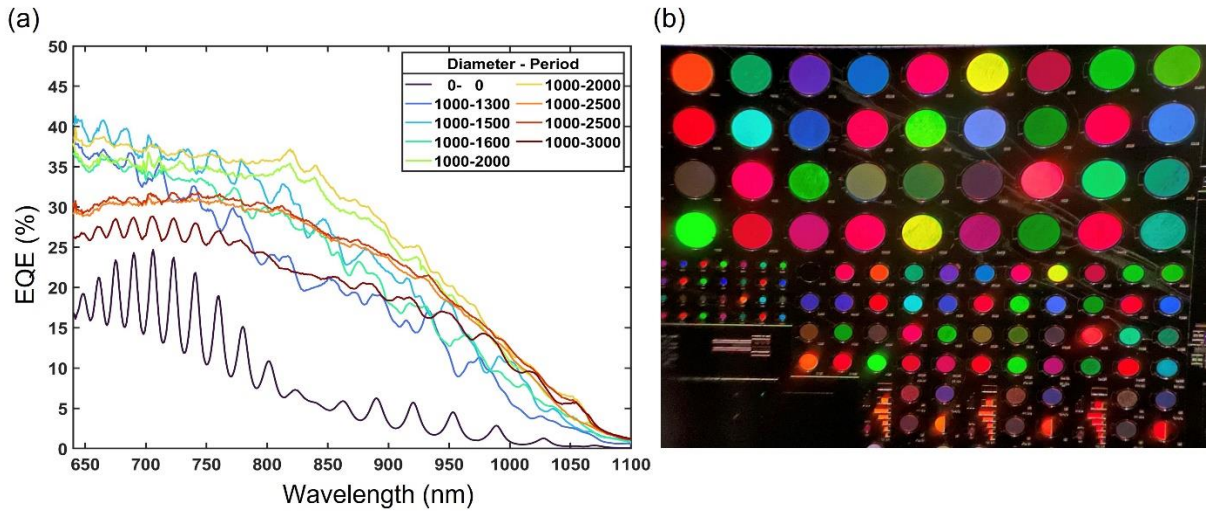


Fig. 6.29. Experimental demonstration of Si APD. (a) EQE unique responses of several Si photon-trapping (PT) APD with a fixed diameter (1000 nm), and varying periodicity compared to a control Si APD (0-0). (b) A microscopic image of the fabricated Si PT APD with varying diameter and periodicity selectively reflecting certain wavelengths from the white microscopic light.

References

[1] J. C. Campbell, "Recent advances in avalanche photodiodes," *Journal of Lightwave Technology,* vol. 34, no. 2, pp. 278-285, 2016.

[2] M. Ghioni, A. Gulinatti, I. Rech, F. Zappa, and S. Cova, "Progress in silicon single-photon avalanche diodes," *IEEE Journal of selected topics in quantum electronics,* vol. 13, no. 4, pp. 852-862, 2007.

[3] C. Bartolo-Perez *et al.*, "Avalanche photodetectors with photon trapping structures for biomedical imaging applications," *Optics Express,* vol. 29, no. 12, pp. 19024-19033, 2021.

[4] C.-K. Tseng, K.-H. Chen, W.-T. Chen, M.-C. M. Lee, and N. Na, "A high-speed and low-breakdown-voltage silicon avalanche photodetector," *IEEE Photonics Technology Letters,* vol. 26, no. 6, pp. 591-594, 2014.

[5] S. Ghandiparsi *et al.*, "High-speed high-efficiency photon-trapping broadband silicon PIN photodiodes for short-reach optical interconnects in data centers," *Journal of Lightwave Technology,* vol. 37, no. 23, pp. 5748-5755, 2019.

[6] C. Bartolo-Perez *et al.*, "Maximizing Absorption in Photon-Trapping Ultrafast Silicon Photodetectors," *Advanced Photonics Research,* vol. 2, no. 6, p. 2000190, 2021.

[7] R. D. Richmond and S. C. Cain, *Direct-detection LADAR systems*. SPIE Press Bellingham, 2010.

[8] K. McKay and K. McAfee, "Electron multiplication in silicon and germanium," *Physical Review,* vol. 91, no. 5, p. 1079, 1953.

[9] B. G. Streetman and S. Banerjee, *Solid state electronic devices*. Pearson/Prentice Hall Upper Saddle River, 2006.

[10] C. Bartolo-Perez *et al.*, "Engineering the gain and bandwidth in avalanche photodetectors," *Optics Express,* vol. 30, no. 10, pp. 16873-16882, 2022.

[11] M. K. Emsley, O. Dosunmu, and M. Unlu, "Silicon substrates with buried distributed Bragg reflectors for resonant cavity-enhanced optoelectronics," *IEEE Journal of Selected Topics in Quantum Electronics,* vol. 8, no. 4, pp. 948-955, 2002.

[12] Y. Gao *et al.*, "Photon-trapping microstructures enable high-speed high-efficiency silicon photodiodes," *Nature Photonics,* vol. 11, no. 5, pp. 301-308, 2017.
[13] F. T. Ulaby, E. Michielssen, and U. Ravaioli, *Fundamentals of applied electromagnetics 6e*. Prentice Hall, 2001.
[14] R. Saive, "Light trapping in thin silicon solar cells: A review on fundamentals and technologies," *Progress in Photovoltaics: Research and Applications,* vol. 29, no. 10, pp. 1125-1137, 2021.
[15] Z. Yang, T. Albrow-Owen, W. Cai, and T. Hasan, "Miniaturization of optical spectrometers," *Science,* vol. 371, no. 6528, p. eabe0722, 2021.
[16] A. Ahamad *et al.*, "Smart nanophotonics silicon spectrometer array for hyperspectral imaging," in *CLEO: Science and Innovations*, 2020: Optical Society of America, p. STh3M. 2.

Chapter 7 Achieving the optical performance equivalent of group III-V photodetectors on the silicon platform

7.1 lateral Si photodetectors (PDs)

Silicon inherently exhibits a weaker absorption coefficient in comparison to group III-V compound semiconductors [1][2]. The absorption in Si shows a dramatic reduction in the near-infrared (NIR) wavelength spectrum—a wavelength spectrum range essential to plenty of aforementioned optoelectronic applications. Owing to its weak absorption, Si-based photonic devices demand a thick substrate layer to fully utilize the illuminated optical stimuli, e.g., for 95% photon absorption of 850 nm wavelength, a ~50 μm thick Si layer is required [3]. Despite an enhanced absorption in such a thick Si absorption layer, a long transit time of the generated electron-hole pair and its inherent low carrier mobilities result in only sub-par photodetectors that do not comply with the performance requirements of the emerging photonic systems. In contrast with Si, the most commonly used III-V compounds such as GaAs and InP exhibit 15× and 40× higher absorption, respectively, at a wavelength of 850 nm [1]. GaAs show ~90% absorption of 850 nm incident wavelength in merely a 2.5 μm thick layer. Attributing to its higher absorption coefficient and exceptionally high carrier mobilities [4], GaAs-based photodetectors exceed the performance expectations for the current and emerging optoelectronic systems. Such exceptional performance helps the GaAs, and their alloys thrive as the mainstream materials for numerous emerging photonic applications. However, a CMOS incompatibility in the fabrication process of such devices calls for a tedious and costly hybrid integration with CMOS electronics. Recently, despite its sub-par performance, foundries have introduced Si-based optoelectronic integrated circuits (OEIC) in the CMOS infrastructure [5][6], as a trade-off between performance and the manufacturing/integration cost. Therefore, innovative techniques to enhance light-matter interaction are crucial to designing photodetectors with thinner Si film.

In this chapter, an experimental demonstration of performance enhancement of Si- photodetector by incorporating photon-trapping (PT) nanostructures is discussed. We have fabricated metal-semiconductor-metal (MSM) photodetectors (PDs) on a 1 μm thin silicon layer and integrated periodic photon-trapping hole arrays. A schematic of control (no nanoholes) PD, and PT PD are shown in Fig. 7.1. We have utilized CMOS-compatible processes to fabricate the photodetectors. To present a fair comparison, we have fabricated two sets of devices, with and without photon-trapping hole array. These hole arrays assist in diverting normally incident beams of light almost orthogonally and facilitate a lateral propagation of light. Such engineered surface profiling efficiently guides and effectively slows down the propagating light beam and results in a dramatic improvement in absorption efficiency. We demonstrate remarkable enhancement of 80%, 85%, and 65% in the absorption efficiency in the photon-trapping-equipped photodetector for the NIR wavelength spectrum at 800, 850, and 905 nm, respectively. Further, we show a ~20% reduction in the device capacitance due to a reduced effective device volume of photon-trapping-equipped Si photodetectors that can further result in an ultrafast performance due to the reduction in RC time constant. Furthermore, with the help of finite-difference time-domain (FDTD) simulations, we have shown that most of the propagating modes in Si with photon trapping structures exhibit lower optical group velocity compared to that of conventional Si layer without photon-trapping structures. This contributes to an enhanced light-matter interaction ensuring a higher absorption. This enhancement in the absorption is shown to be comparable to that of GaAs absorption. We have also shown that an equivalent performance enhancement can be achieved with 30 nm and 100 nm thin Si layers. The performance of such ultrathin Si-based photo-trapping-equipped photodetectors are intriguingly encouraging to fabricate ultrafast photodetectors in the existing CMOS foundry framework.

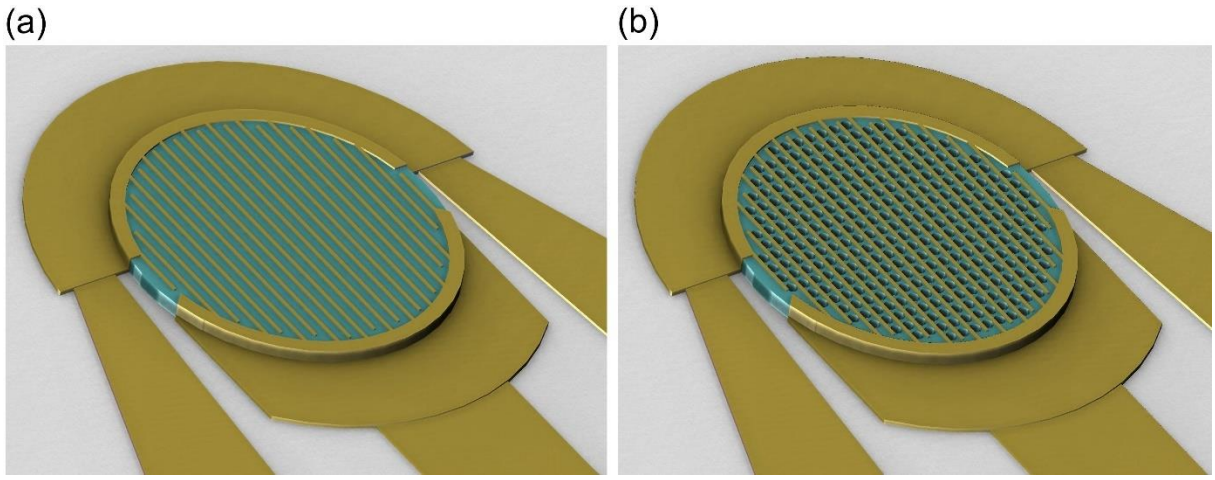


Fig. 7.1. Schematic of Si MSM fabricated photodetectors devices. (a) Control (planar/no nanoholes) PD, (b) Photon-trapping Si PD.

7.2 Optical simulation

A 3D finite-difference time-domain (FDTD) optical simulation was utilized to rigorously solve Maxwell's curl equations to calculate the electromagnetic (EM) fields within the photodetectors. The simulations were performed for the array of cylindrical holes of 700 nm diameter with a 1000 nm period as well as 1000 nm diameter with a 1300 nm in Si slab of 1000 nm thin on SiO_2 substrate. The depth of the holes was assumed to be 1000 nm. Furthermore, the optical absorption in Si was approximated by the Lorentz model with parameters fitted to the data at the range of around 850 nm wavelength. In FDTD, the incident pulse had a Gaussian-shaped spectrum between 600 to 1200 nm, spatially it is a plane wave. The averaged amplitude vs. wavelengths of the signal that were reflected and transmitted at the bottom and the sides were detected using Fourier transform. Then the reflected (R) and transmitted (T) power normalized to the input source were calculated. The absorption (A) was calculated as A = 1- R -T. Boundary conditions in the direction of light propagation were assumed to be Perfectly Matched Layers (PML). Periodical boundary conditions were considered for the other directions around the simulation area. Nanoholes diameter, periodicity, depth, and sidewalls profile play a main role to optimize the PDs designs. Figure. 7.2. shows the effect of coupling phenomena for small and

large holes (nanohole's diameter closer to the targeted incident wavelength) at different incident angles of light on the photon absorption in Si photon-trapping photodetectors.

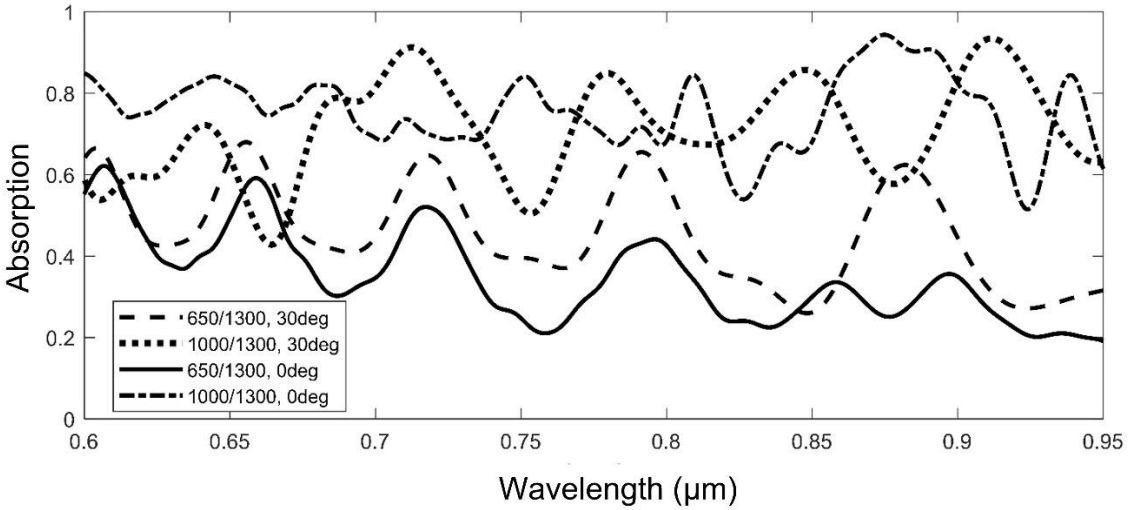


Fig. 7.2. Photon absorption in photodetectors with small (650/1300) and large holes (1000/1300) under different illumination angles.

Optical absorption of designed Al interdigitated metals that covers the photodetectors is simulated as can be seen in Fig. 7.3. As the absorption (A) was calculated from A = 1- R -T, the results show extremely low optical absorption of Al interdigitated metals in photon trapping Si PDs. Also, the optical reflection is extremely low in photon trapping PDs compared to the control PDs due the existence of the nanoholes.

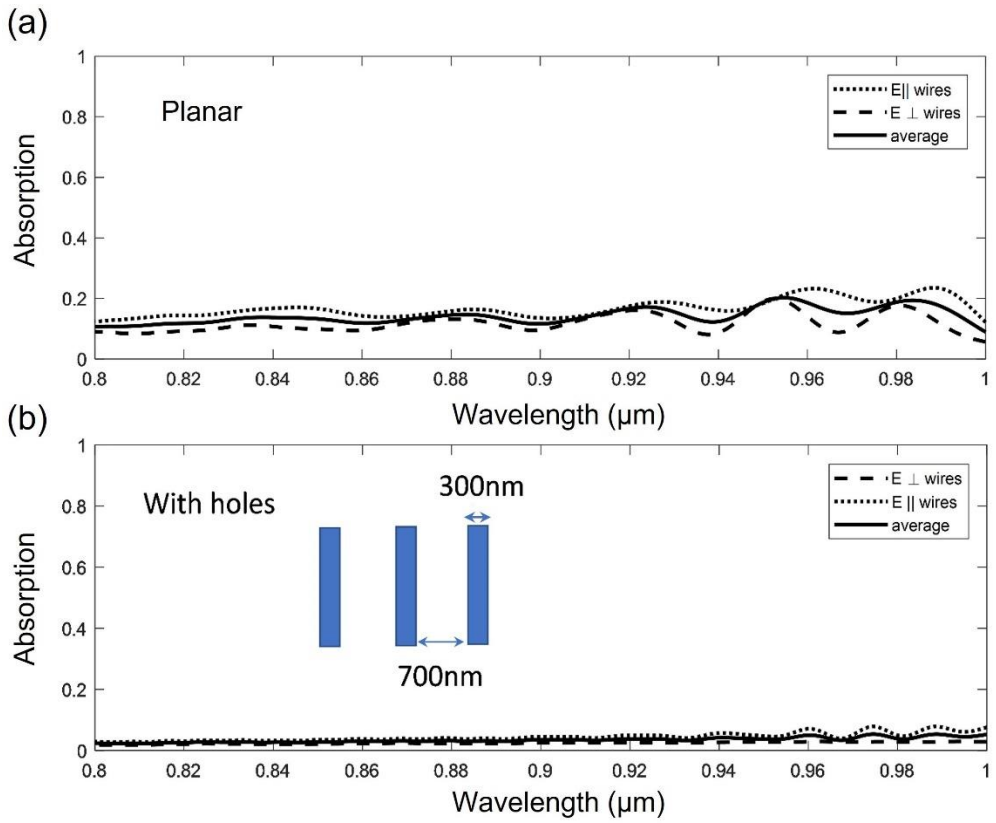


Fig. 7.3. Optical absorption of the aluminum interdigitated metals. (a) Optical absorption of Al interdigitated metals in control (planar) PD, (b) Extremely low optical absorption of Al interdigitated metals in photon trapping Si PD.

The cross-sectional simulation structure is schematically shown in Fig. 7.4 (a). A thin Si absorber is assumed to be prepared on an SOI substrate. The photon trapping photodetector is simulated for absorptions in wavelengths ranging from 600 nm to 1100 nm as presented in Fig. 7.4 (b). A photodetectors with a planar surface is also simulated as a reference. The red and blue curves are simulated absorption spectra of photon trapping photodetectors for normally incident light and incident light averaged between ±10° angles, respectively. The photon trapping photodetectors exhibit distinctly higher absorption in comparison with the control counterpart.

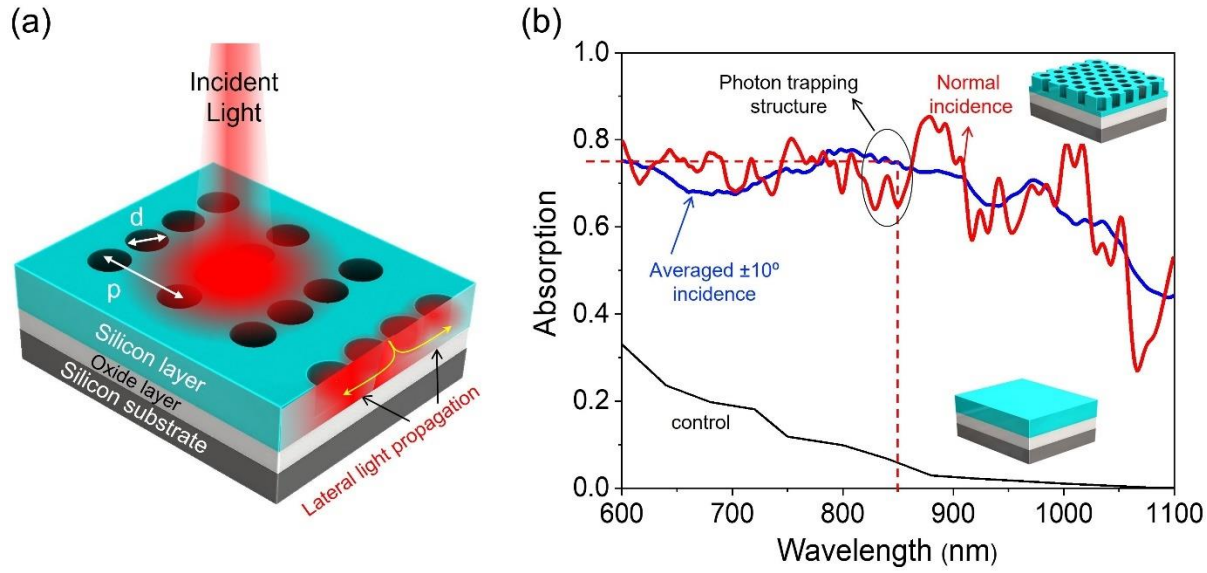


Fig. 7.4. (a) Schematic of silicon slab on silicon-on-insulator (SOI) integrated with cylindrical photon-trapping nanoholes. (b) A comparison of simulated absorption of photon-trapping and planar) Si PD, where red and blue curves are simulated absorption spectra for normally incident light and averaged among ±10° angles, respectively.

The FDTD simulated structure has 1 µm Si thin device layer on 1 µm SiO_2 layer. Hexagonally unit cell cylindrical nanoholes with diameter/period (d/p) 700/1000 nm are positioned between Al interdigitated metals to increase the light absorption in Si with enhanced lateral light propagation in all directions. Coupling modes of control PD and PD integrated with nanoholes arrays are shown in Fig. 7.5 (a) and (b), respectively. In the control PD, photons do not experience perpendicular bending and continue to propagate in the vertical orientation and be reflected back from the bottom Si-SiO_2 interface. FDTD simulations exhibit optical coupling and the creation of lateral modes, increasing the interaction of light with the Si, instead of simply passing through the silicon layer in the PT PDs [Fig. 7.5 (b)]. Hence, the same absorption in a thin layer of Si with photon trapping PD can be obtained as a thick layer which allows a shorter transit time for the carriers generated in the photodetectors.

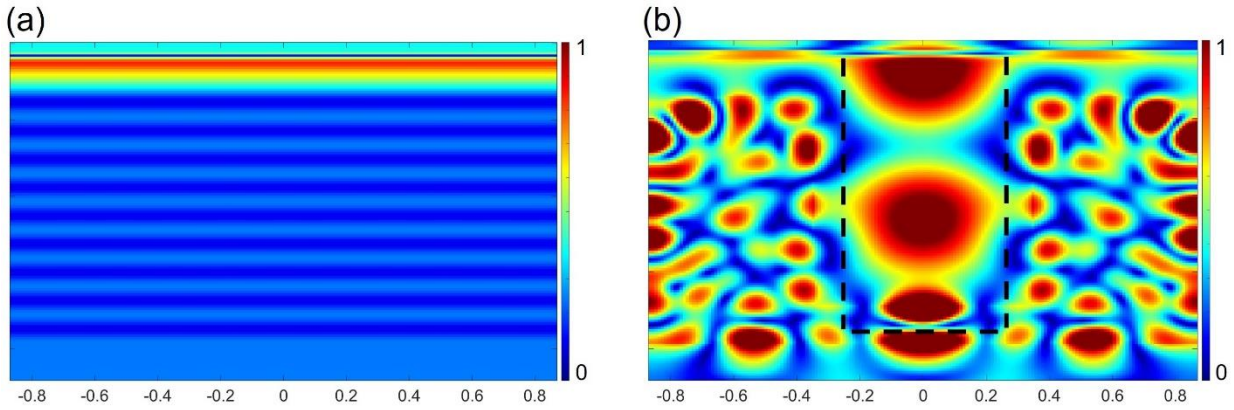


Fig. 7.5. FDTD optical simulation for light coupling in (**a**) Control and (**b**) Photon-trapping Si photodetectors on SOI.

7.3 Device design, fabrication, and processing

7.3.1 Design and fabrication of photodetectors

The Si absorber layer (*p*-type) with a thickness of 1000 nm was epitaxially grown on a silicon-on-insulator (SOI) substrate. The SOI wafer has a 1000 nm buried oxide layer (BOX), where the active layer was epitaxially grown with a resistivity of 14-22 ohm-cm. Next, the native oxide was removed by cleaning the surface of the Si with buffered oxide etching (BOE) (6:1) process. The flow chart of the fabrication process is shown in Fig. 7.6, (a) Epitaxially grown p-type 1000 nm thick silicon on SiO_2 SOI wafer. (SOI wafer substrate: Gray (SiO_2), epitaxially grown Si: Turquoise (Si)). The native oxide of the wafer is cleaned by the buffered oxide etching BOE (6:1) process. (b) Photon-trapping holes patterning using DUV photolithography and DRIE holes etching. (c) Mesa etches to the substrate layer (SiO_2). (d) 100 nm thick, and 300 nm width interdigitated aluminum (Al) metals sputtered and lift-off to form Schottky contact: Gold (interdigitated Schottky contact). (e) Coplanar waveguide metal deposition (CPW: Gold). The detailed process steps are described in the following section.

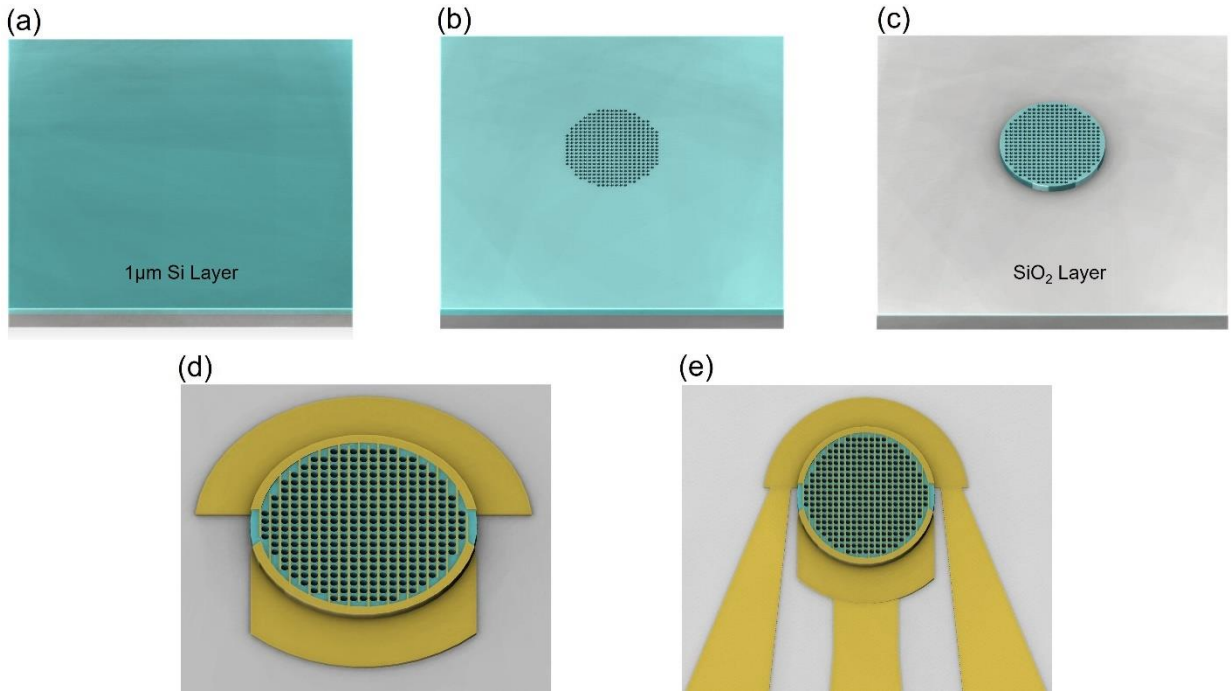


Fig. 7.6. Flow chart of the fabrication process of Si metal-semiconductor-metal photon-trapping photodetector devices.

7.3.1.1 Photon-trapping nanoholes formation

Right after the wafer cleaning, nano/sub-micron photon trapping (PT) hole arrays were patterned using a stepper lithography system. In the stepper system, we can adjust the focus of the ultraviolet (UV) light to shrink the features present on the mask plate and enables nano/sub-micron feature patterning. Next, PT hole arrays were etched in a reactive ion etching (RIE) process as can be seen in Fig. 7.7. Fluorine-based chemistry was utilized to etch holes in the silicon. The fabricated PT structures possess a period, diameter, and hole depth of 1300, 1000, and 600 nm, respectively.

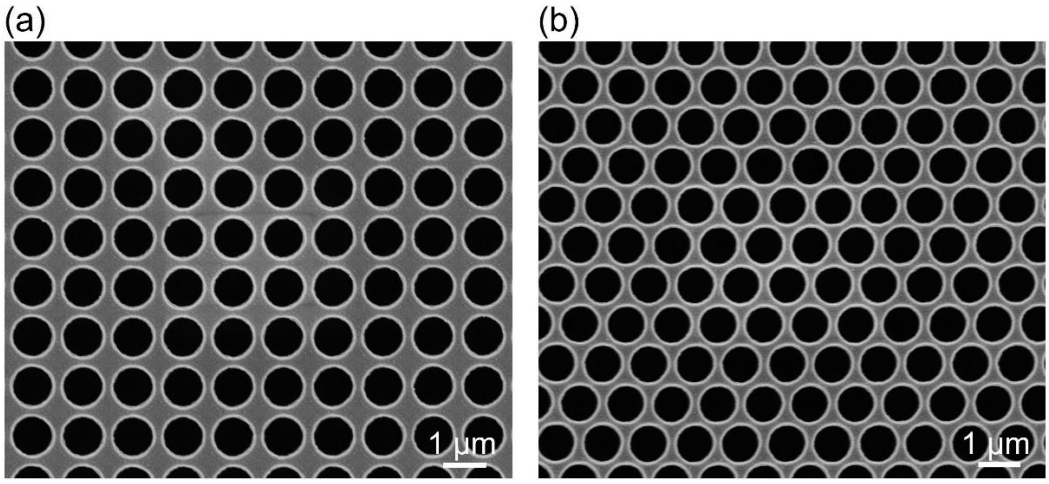


Fig. 7.7. SEM images of fabricated nanoholes. (a) nanoholes formation in square unit cell lattice, (b) nanoholes formation in hexagonal unit cell lattice.

7.3.1.2 Mesa isolation

In this process step, the top and the bottom mesa structures of the photodetector were patterned. The top mesa was defined followed by the bottom mesa in alignment with the previously patterned PT structures by utilizing the stepper and RIE system. Patterning the top mesa exposes the bottom contact layer on the stack, whereas the bottom mesa patterning isolates the photodetectors from the neighboring devices.

7.3.1.3 Contacts metallization

In the next step, the Si substrate was cleaned with BOE (6:1) to remove the native oxide before the metal deposition. The interdigitated aluminum (Al) fingers with a thickness of 100 nm and width of 300 nm were sputtered on the Si in an RF sputter system. Uniform Schottky contacts were prepared by lifting off the sputtered Al as can be depicted in Fig. 7.8.

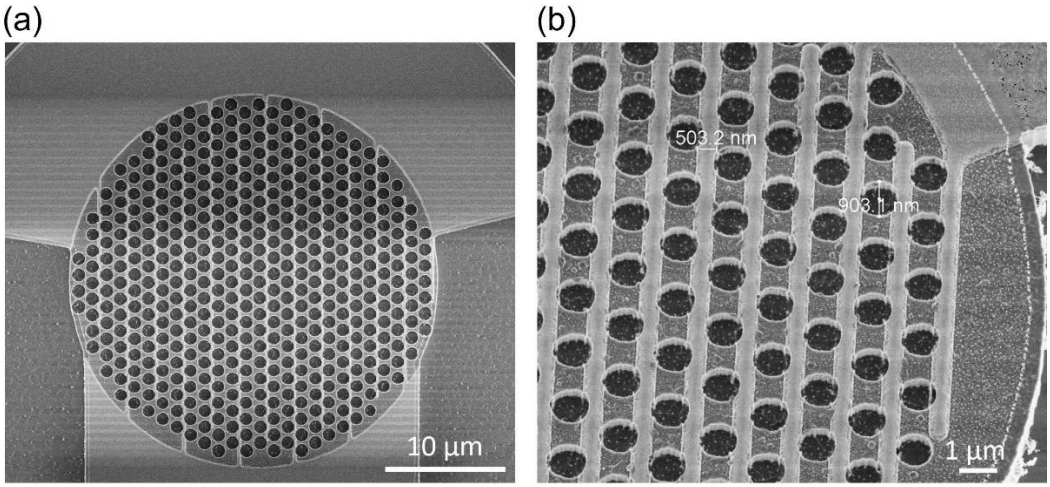


Fig. 7.8. SEM images of mesa isolation and interdigitated contacts metallization. (a) contacts and interdigitated metallization. (b) A focused SEM image of the PD's active region with photon-trapping holes. Al interdigitated contacts are seen in between holes.

7.3.1.4 Co-planar waveguide patterning

After the metallization, the sample was patterned for co-planar waveguide contact. In this step, about 300 nm of Al layer was deposited followed by a lift-off process to create coplanar waveguides (CPW), which utilizes for the high-speed transport of the electrical pulse converted from a picosecond (ps) pulsed laser by the fabricated photodetectors as can be seen in Fig. 7.9.

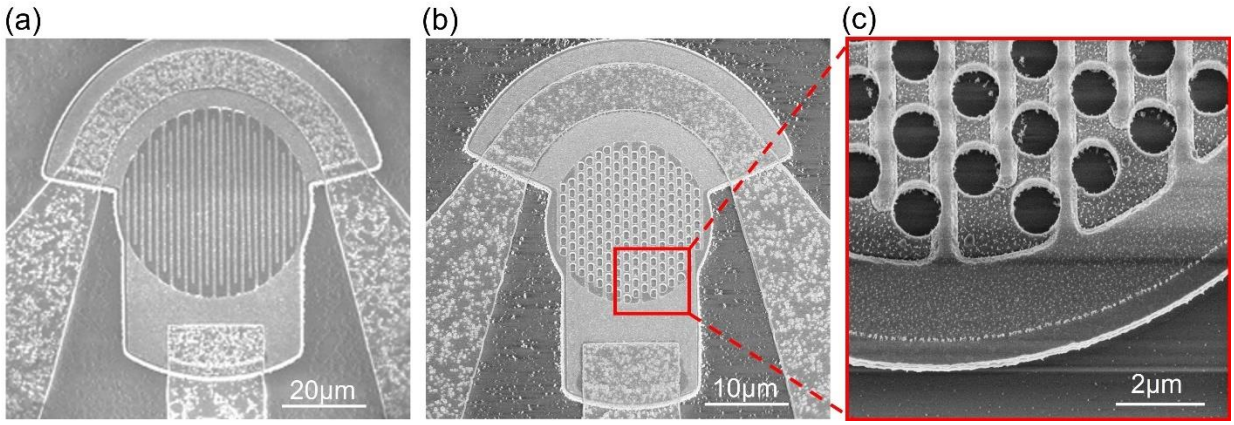


Fig. 7.9. SEM images for the fabricated Si photodetectors. (a) control PD with CPW. (b) photon-trapping PD with CPW. (c) A focused SEM image of circular shape holes in a hexagonal lattice formation.

7.3.1.5 Passivation

passivation process step is conducted after completing the fabrication of the devices. To passivate the surface states created on the sidewalls of the holes and mesa, 2% HF was used

for 3 seconds with HF:H_2O, 1:100 ratio. The hydrogen ion present in the solution attaches itself to the surfaces and neutralizes the active surface state. This passivation process reduces the dark state leakage current.

7.3.1.6 Nanoholes structures' unique reflection response

A firsthand confirmation of the wavelength selectivity of these photon trapping holes is evident from the different color spectrums revealed during microscopic imaging for different devices with different nanoholes diameter (d), and Periodicity (p) as can be depicted in Fig. 7.10. Each design of the fabricated photodetector have a unique absorption and reflection spectrum. These unique responses can be utilized in many optoelectronics applications accordingly.

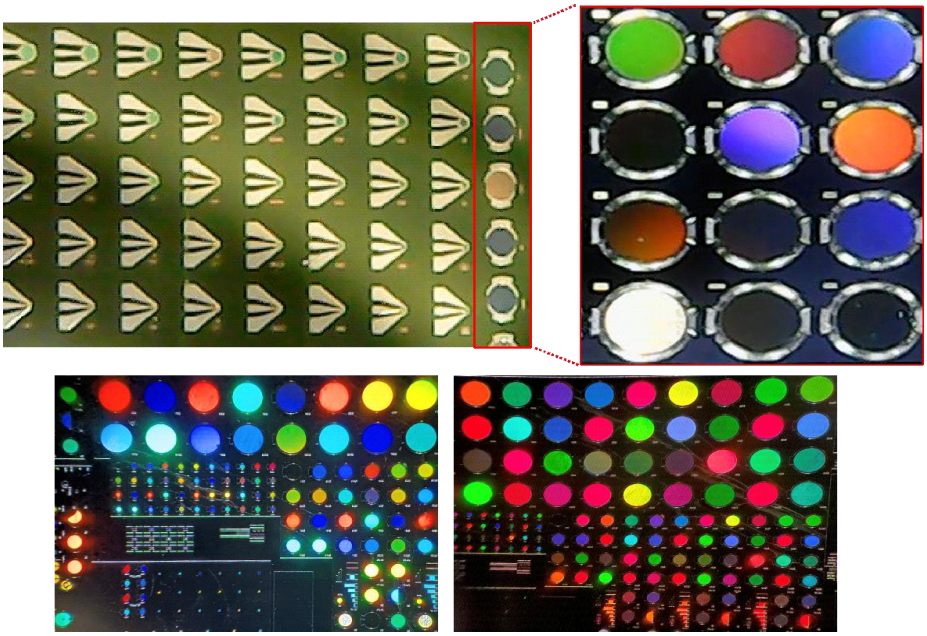


Fig. 7.10. Optical images of the fabricated photodetectors. Optical microscopy images of fabricated devices with various mesa sizes, different photon trapping structures with varying hole diameters (d), and periodicities (p) (Left Top). The change in emission color from the surface of the devices indicates wavelength-dependent photosensitivity for varying device diameter, d, and p (All other images).

7.4 Results and Discussion

7.4.1 Exceeding optical absorption efficiency of thin GaAs

The geometry is optimized for the lattice structure, diameter, period, and depth of the photon trapping holes that are filled with air. The cross-sectional structure is schematically shown in Fig.

7.11 (a), as the photon trapping cylindrical hole arrays allow lateral propagation by bending the incident light, resulting in an enhanced photon absorption in Si. CMOS-compatible processes have been utilized to fabricate the photodetectors. The devices are fabricated on a silicon on-insulator (SOI) substrate with a 1 μm thin active Si layer, a.k.a., the absorber layer. Figure. 7.11 (b) showcases the optical microscopy images of the fabricated photodetectors for a range of hole diameter (d), and periodicity (p) of holes.

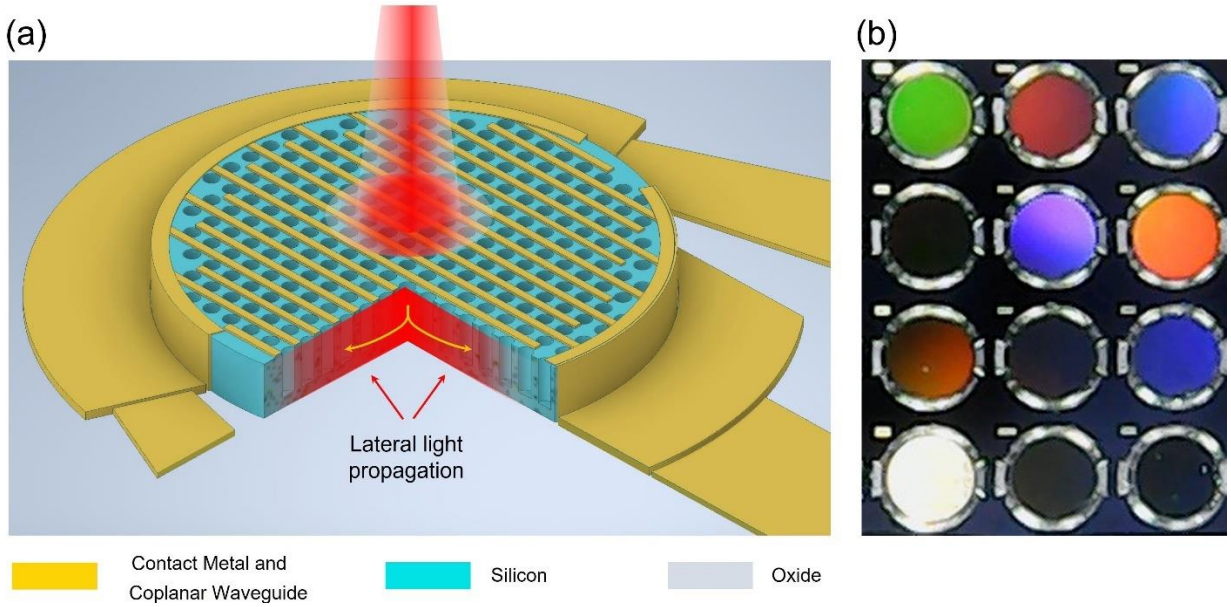


Fig. 7.11. (a) A Schematic of the photon-trapping silicon photodetector. (b) Optical microscopy images of the photon-trapping photodetectors, The change in emission color from the surface of the devices indicates wavelength-dependent photosensitivity for varying device diameter, d, and p.

Utilizing the Bouguer-Beer-Lambert law and considering surface reflection losses [7][8], an effective absorption coefficient (α_{eff}), defined in Equation (7.1), is estimated to quantify the enhancement in photon absorption of the fabricated devices with photon-trapping designs.

$$\alpha_{\text{eff}}(\lambda) = -\frac{1}{d_{Si}}\left[\ln\left(\frac{1-QE_{meas}(\lambda)}{1-R_{meas}(\lambda)}\right)\right] \quad (7.1)$$

Where d_{Si} is the thickness of the Si active layer of the photodetector, and QE_{meas}, and R_{meas} are the experimentally measured quantum efficiency and surface reflection of the devices respectively.

The measured surface reflections for the planar devices without anti-reflection coating range from 15 –25%, whereas the surface reflections in the case of photon trapping photodetectors show a notable reduction and are measured to be 10 – 12% for illumination wavelengths ranging from 800 to 905 nm. Using the experimental results and Equation (7.1), the α_{eff} of the Si photon-trapping photosensors is estimated as a function of incident wavelengths. The estimated α_{eff} of the photon-trapping thin Si photodetectors is compared against the absorption coefficient of the bulk Si, and other potential photosensitive semiconductors such as Ge, InGaAs, and GaAs [9][10] as shown in fig. 7.12. The enhancement factor of the thin 1 μm thin photon-trapping Si photodetectors is not only higher than that of the bulk Si but also exceeds the absorption coefficient of GaAs over a broad near infrared (NIR) wavelength spectrum and becomes comparable to the absorption coefficients of Ge and InGaAs. Quantitatively, in the photon-trapping hole-array equipped photodetectors with the measured quantum efficiencies of 80, 84, 86, and 68% at 800, 840, 850, and 905 nm respectively, α_{eff} is determined to be approximately 27467, 31797, 39713, and 14938 cm^{-1}. The α_{eff} determined at 850 nm is more than 70× and about 4× higher than the intrinsic absorption coefficient of Si (535 cm^{-1}) and GaAs (10,035 cm^{-1}) [10], respectively. Hence, the effective absorption coefficient of the fabricated photon-trapping photodetectors exceeded the intrinsic absorption coefficient of GaAs in the NIR wavelength region.

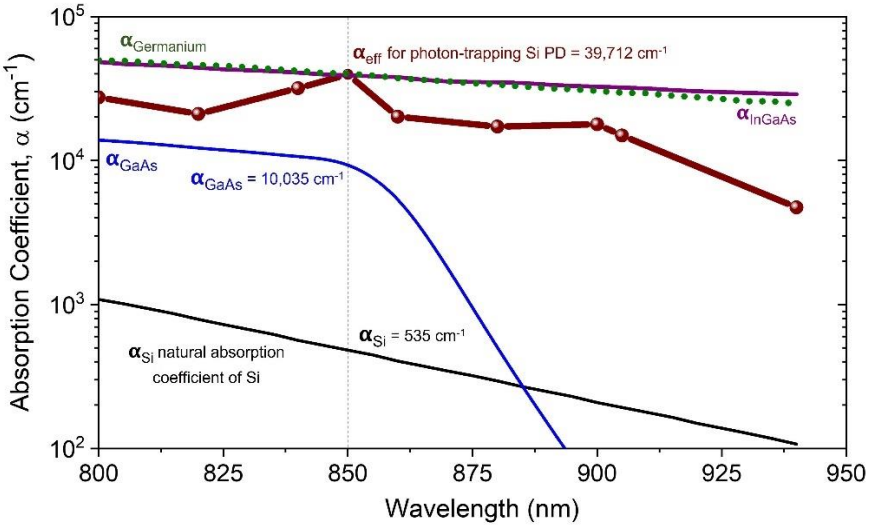


Fig. 7.12. Experimental demonstration of absorption enhancement in Si that exceeds the intrinsic absorption limit of GaAs. The absorption coefficient of engineered photodetectors shows an increase of 20× at 850 nm wavelength compared to bulk Si, exceeds the intrinsic absorption coefficient of GaAs, and approaches the values of the intrinsic absorption coefficient of Ge and InGaAs.

7.4.2 EQE of the fabricated Si photodetectors

The external quantum efficiency (EQE) which is the essential performance metric to quantify the optical sensitivity of the fabricated photodetectors has been studies in this section. The measured QE of photon-trapping photodetectors for incident wavelengths ranging from 800 to 905 nm is shown in Fig. 7.13 (a). A comparison for QEs of control (planar) and photon-trapping photodetector is exhibited accordingly. EQEs over 80% are observed experimentally in the photon-trapping photodetectors for the incident wavelengths below 860 nm. Owing to Si's inherent optical material properties, the absorption decreases above 860 nm wavelength, with a minimum value as low as 68% at 905 nm. However, compared to the photodetectors with a planar surface, the absorption efficiency is increased by >550% in photon-trapping photodetectors at 850 nm wavelength. The corresponding responsivities of the photon-trapping devices exhibit over 500 mA/W as shown in Fig. 7.13 (b). Besides, the minimum enhancement of quantum efficiency in all the fabricated photon-trapping photodetectors compared to the control devices is at least more than 280% for the wavelength spectrum between 800 and 905 nm. The measured quantum efficiencies also exhibit an excellent agreement with simulated quantum efficiencies in both control and photon trapping devices as depicted in Fig. 7.13 (a). Such a high absorption enhancement directly results from the generation of optical modes propagating laterally due to the integrated photon trapping nanoholes.

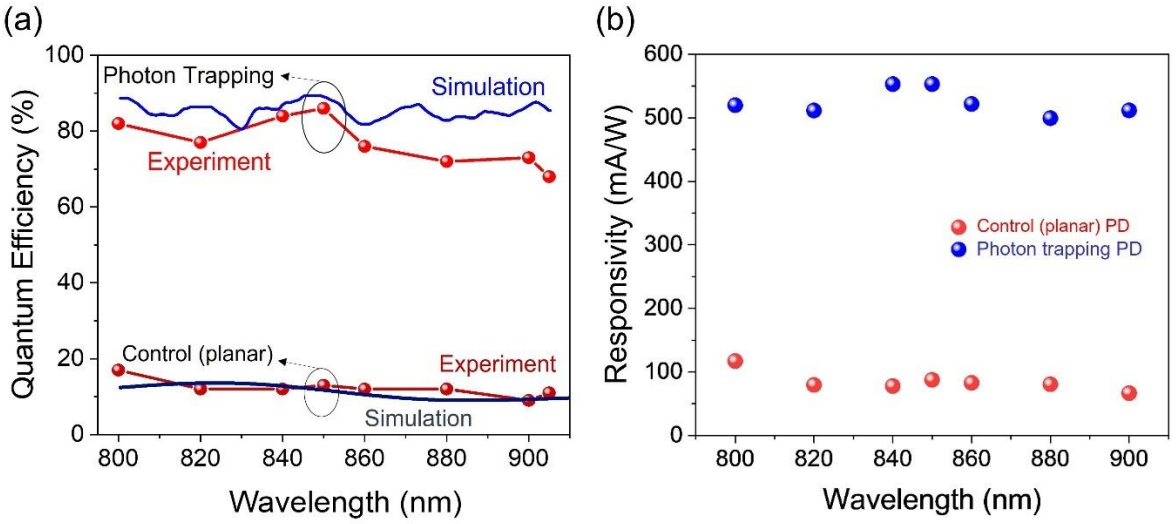


Fig. 7.13. (a) The measured quantum efficiencies of the devices have an excellent agreement with FDTD simulation in both planar and photon-trapping devices. (b) Responsivity of the fabricated photodetectors.

Intriguingly, we also observed that the enhanced absorption coefficient of our fabricated devices effectively exceeds the $4n^2$ limit, as can be seen in Fig. 7.14., where n is the refractive index of silicon at the corresponding wavelengths. Nevertheless, this discussion doesn't claim that it exceeds the light trapping geometrical limit of $4n^2$ [3][11], since a collimated laser beam was used for device illumination. In contrast, an isotropic and incoherent light source is commonly used in solar cell characterization. For the case of a collimated beam, the geometrical limit is adjusted by $4n^2/(\sin\theta)^2$, where θ is the angle between the light source and a plane perpendicular to the surface [12]. We further noticed that the absorption enhancement of our devices could reach a maximum up to $70n^2$ limit at 850 nm of incident wavelength [Fig. 7.14]. Further investigation correlating the illumination angle of the collimated beams and absorption enhancement will help understand if the light trapping geometrical limit can be overcome.

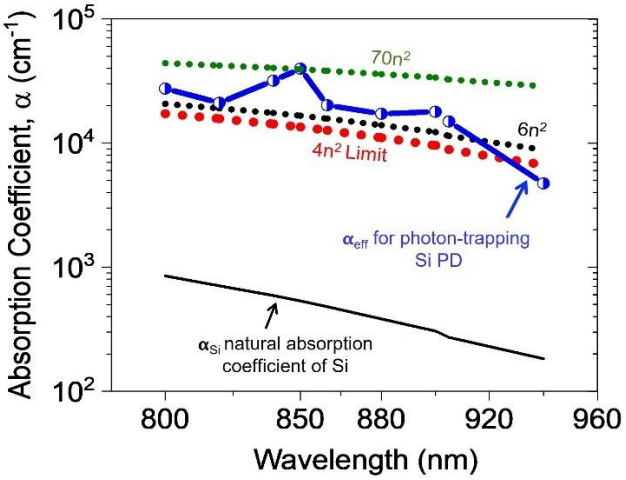


Fig. 7.14. The maximum enhanced absorption coefficient obtained from the most optimized fabricated photon trapping photodetectors exceeded $70n^2$, where n is the refractive index of the material. The devices were measured by a collimated beam, which does not allow to directly compare this absorption coefficient with the geometrical light-trapping limit of $4n^2$.

7.4.3 Utilizing photon trapping structures for capacitance reduction and ultra-fast Si PDs operation

Photon trapping photodetectors exhibit reduced capacitance compared to the planar counterpart due to reduced surface areas caused by the photon-trapping structures, as experimentally characterized and depicted in Fig. 7.15., leading to enhance bandwidth in the device. Such reduction in capacitance can further strengthen the ultrafast response of the devices caused by the thin absorption layer. Detailed discussion on capacitance reduction and ultra-fast operation in Si photodetectors are discussed in chapter 4.

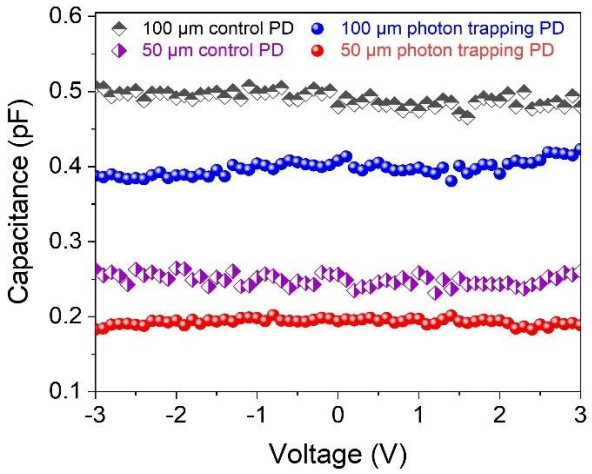


Fig. 7.15. Photon-trapping photodetectors exhibit reduced capacitance compared to their planar (control) counterpart, enhancing the ultrafast photoresponse capability of the device.

7.4.4 Si Photon trapping photodetectors ultra-fast characterization

A pulsed laser with ~15 ps pulse width and a repetition rate of 70 MHz was used to conduct ultra-fast measurements on a microwave probe station. A photodetector with a diameter of 50 μm was tested with a microwave probe and the light beam was aligned with a translational stage to maximize the photocurrent. The electrical pulses were collected by a 20-GHz sampling scope. The PD under test was DC biased using a 25-GHz bias-T.

Figure. 7.16. shows measured ultra-fast pulse responses of PDs with (blue spheres) and without (red circles) photon-trapping. Figures. 7.16. (a) and (b) show normalized pulse responses at 3 V and 10 V applied bias, respectively. The illumination wavelength of pulse light is 850 nm. Si MSM photodetectors with holes maintain their speed performance while dramatically increasing EQE.

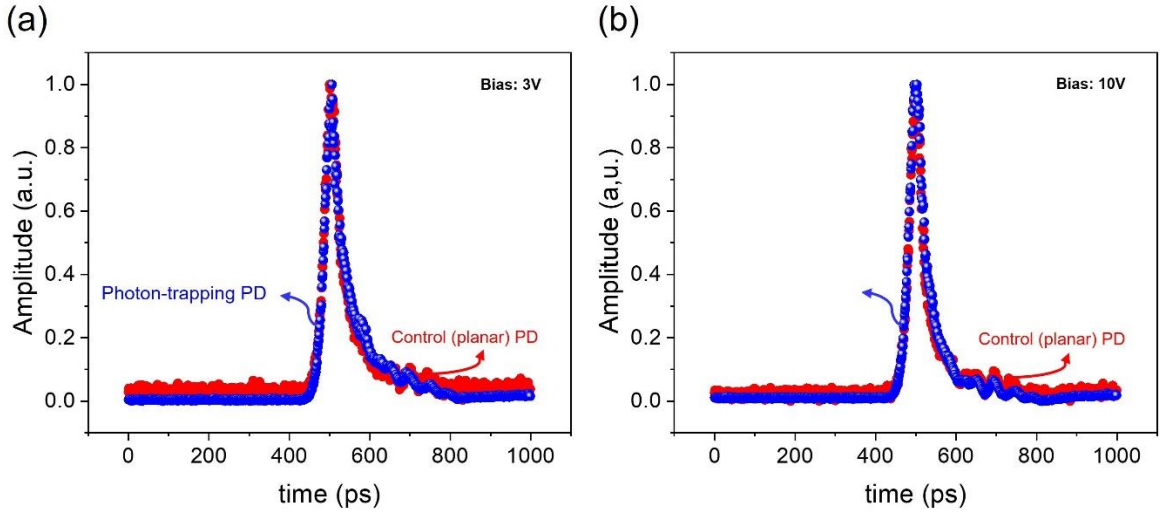


Fig. 7.16. Normalized RF pulse responses at (a) 3 V and (b) 10 V applied bias. The illumination wavelength of pulse light is 850 nm.

Considering the 22 ps FWHM response for the 20-GHz sampling oscilloscope, and the optical laser pulse width of ~16-15 ps (Fig. 7.17), the actual response of the device was estimated to be 33ps (3V) and 28ps (10V) at 850 nm based on Equation (7.2)

$$\tau_{meas} = \sqrt{\tau_{actual}^2 + \tau_{scope}^2 + \tau_{optical}^2} \quad (7.2)$$

where τ_{meas}, τ_{actual}, τ_{scope} and $\tau_{optical}$ are the measured, actual, oscilloscope, and laser optical pulse widths in time domain[13]. This is acceptable for Gaussian pulses and is a valid approximation for our actual measurements.

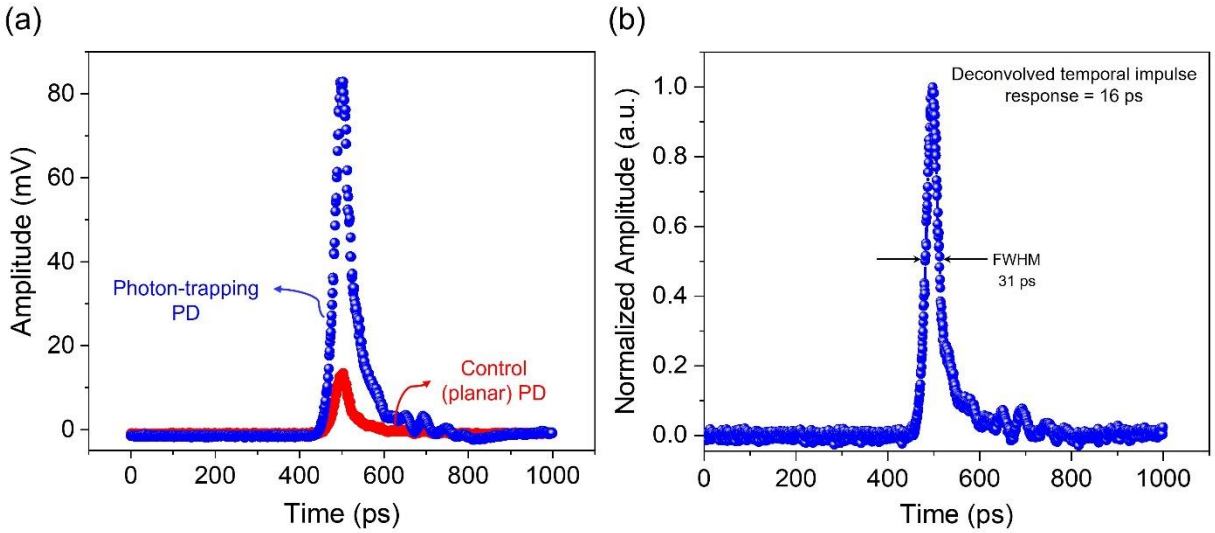


Fig. 7.17. (a) Measured ultra-fast pulse response at 10V bias from PDs with (blue) and without (red) holes. (b) Ultra-fast time response of 31 ps in full width at half maximum (FWHM). The actual time response of the device is approximated to be ~16 ps by considering 22 ps and 15 ps FWHM response for the 20 GHz sampling oscilloscope and optical laser pulse width, respectively.

Such ultra-fast time response coupled with broadband very high absorption efficiency exhibited by ultrathin Si helps overcome the bandwidth-absorption trade-off faced by the ultra-fast photodetector community. This work, thus, is very relevant to the design and fabrication of extremely fast and highly sensitive integrated photodetectors using modern CMOS foundry processes that currently use ultrathin Si of similar thickness.

7.4.5 Performance prediction for ultrathin photon-trapping Si photodetectors

The photon-trapping structures facilitate absorption enhancement through guided lateral modes for a broad range of NIR wavelengths. Figure. 7.18 (a) and (b) represent the calculated Poynting vector in the photon-trapping silicon slab with 1 μm thickness on the x-z and x-y planes. The figure demonstrates how an ensemble of integrated holes induces a change in the direction of the propagating photons from vertical to lateral orientation in Si films. Laterally oriented Poynting

vectors form vortex-like circulation patterns around the sidewalls of the cylindrical holes, resulting in guided light propagation parallel to the photodetector surface for a prolonged time and enabling absorption in Si with high efficiency. Notably, the guided lateral modes in the Si active layer are also facilitated by the front and the back air/Si and Si/oxide layer interfaces, where the oxide layer of the SOI acts as a back reflector. It should be explicitly mentioned here that the oxide layer significantly facilitates the high absorption of photons in the active layer[14].

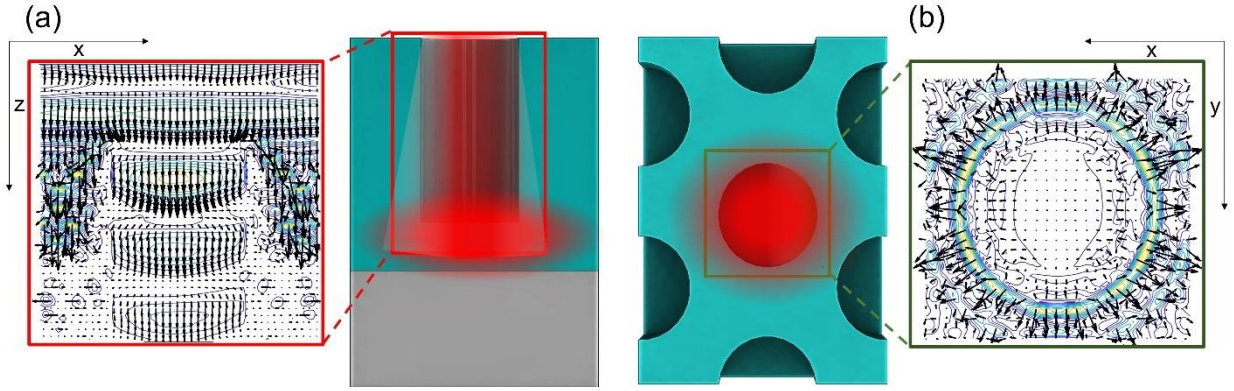


Fig. 7.18. (a) x-z (cross-section) and (b) x-y (top-view), planes showing that the vectors originated from the hole and moved laterally to the silicon sidewalls, where the photons are absorbed.

Leaping on the experimental demonstration of extraordinary enhancement in the performance of photon-trapping photodetectors fabricated on 1 μm thin Si, optical simulations are performed by an FDTD method for 1 μm thin Si. Photon-trapping structure is simulated for absorption in the wavelengths ranging from 800 to 1100 nm as presented in Fig. 7.19 (a).

To study and analyze the photon absorption limits of ultra-thin Si films used in modern CMOS processes, we further explored the absorption efficiency of 30 and 100 nm ultra-thin Si films integrated with and without photon-trapping structures, as depicted in Fig. 7.19 (b). Similar to the Si film with 1 μm thickness, photon-trapping ultra-thin Si film exhibits dramatically higher absorption efficiency than the planar Si film. This also proves that such enhancement in absorption is a direct consequence of enhanced light-matter interaction. More than 21% and 8% absorption efficiencies are observed at 850 nm illumination wavelength in Si with 100 and 30 nm absorption thickness, respectively. By contrast, the absorption efficiency is less than 1% for such

ultrathin planar Si, as depicted in Fig. 7.19 (b). The estimated α_{eff} for 100 and 30 nm Si layers are 23,572 and 27,794 cm^{-1}, respectively, which are significantly higher than the intrinsic absorption limit of GaAs at 850 nm wavelength.

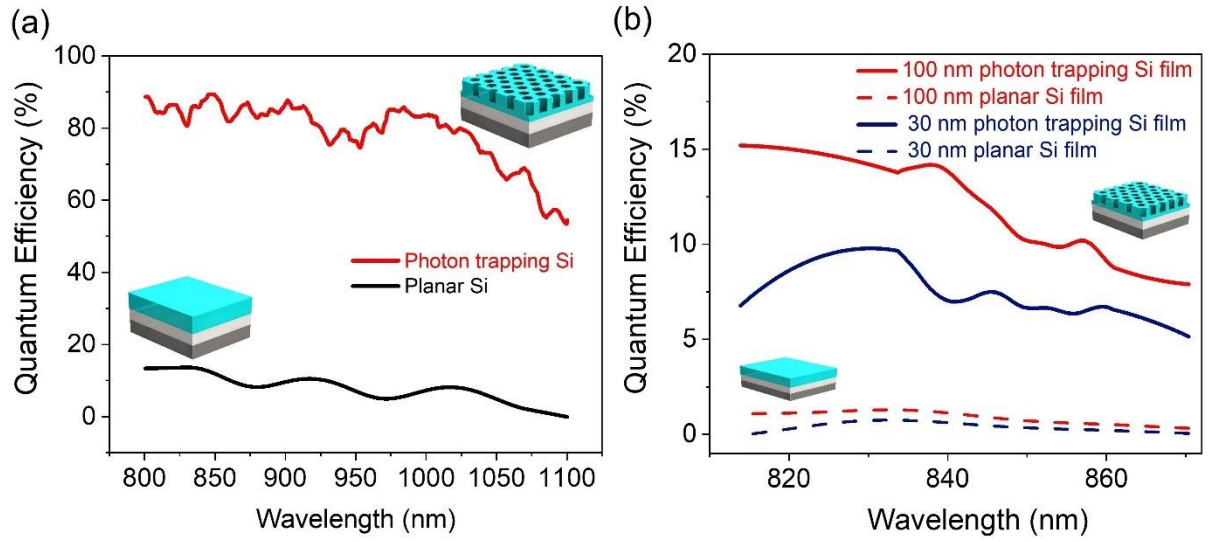


Fig. 7.19. (a) A comparison of simulated absorption of photon-trapping and planar structures demonstrates absorption efficiency in photon-trapping silicon around 90% in 1 μm thickness. (b) Theoretical demonstration of enhanced absorption characteristics in ultra-thin (100 nm and 30 nm) silicon film integrated with photon-trapping structures.

7.4.6 The influence of the size of the holes on the formation of lateral optical modes and the corresponding field distribution

Based on the experimental and simulation observations, photon-trapping structures effectively supporting lateral modes and efficient coupling of light are essential for the optimum enhancement of absorption efficiency. The eigenmodes of the micro-hole array determine the propagation of photons in the lateral direction. The calculated band structures and allowable available eigenmodes with small holes ($d = 100\,nm, p = 1000\,nm, and\ thickness, dSi = 1000\,nm$) and large holes (diameter similar to the incident wavelength) ($d = 700\,nm, p = 1000\,nm, and\ thickness, dSi = 1000\,nm$) are shown in figs. 7.20 (a), 4(b), for the lateral light propagation in a thin film with an array of holes with the period, p, and the hole size, d. The band structure is calculated using the standard technique that converts Maxwell's equations from (r, t) space into (k,ω) space by solving the number of wavevectors $k = mp$, where m is an integer

number. The eigenmodes in the array were calculated at wavelengths near 850 nm, while the ratio of hole diameter and period of the photon-trapping photodetectors is assumed to be $d/p \approx 0.7$ to make it consistent with the fabricated devices. The number of eigenmodes for the hole-array structures increases with an increasing value of p/λ, where p/λ is larger than unity.

Figures 7.20 (a) and (b) illustrate the relationship between lateral wavevector k and the incident wavelength for a hole size of 100 and 700 nm, respectively, under TE and TM polarizations. The solid curves represent the solutions for ΓX and ΓM directions, whereas the dots represent the areas between those directions. It is noticeable that the larger holes pronounce curves with a smaller slope, which corresponds to a smaller group velocity. The next question is the coupling into the array. When significant lateral field components are generated in the cylindrical coordinates for a hole with a specific dimension, the solutions of the wave vectors using Bessel functions can be given as:

$k_0 = \frac{2\pi}{\lambda}$, $q_1^2 = k_0^2 - \beta^2$, $and\ q_2^2 = \varepsilon k_0^2 - \beta^2$, where k_0 is the wave vector for a given frequency in the vacuum, ε is the dielectric constant of silicon, and β is the propagation constant. When the solution to the Bessel function q^2 is k_c, the lateral wave vectors are coupled with eigenmodes. The cross of the solution $k = k_c$ or $k = 0$ with the eigenmodes pronounces the modes that propagate laterally and can be absorbed in the material. It should be noted that the Bessel function was solved for a single hole, and it is expected that a similar characteristic can be achieved for an array of holes. For the small holes, we have the solutions only for the finite number of the eigenmodes with $k = 0$, which corresponds to the guided modes in photonic crystals. Such structures exhibit sharp spikes in the absorption, as shown in Fig. 7.21 (a). However, a continuous solution can be found in the large holey structures for the wavelengths ranging from 800 to 1000 nm, leading to a distinctly higher light absorption than in small holes, as depicted in Fig. 7.21 (a). Hence, the larger holey structures exhibit a good light coupling phenomenon due to the relationship between the k vector and the eigenmodes.

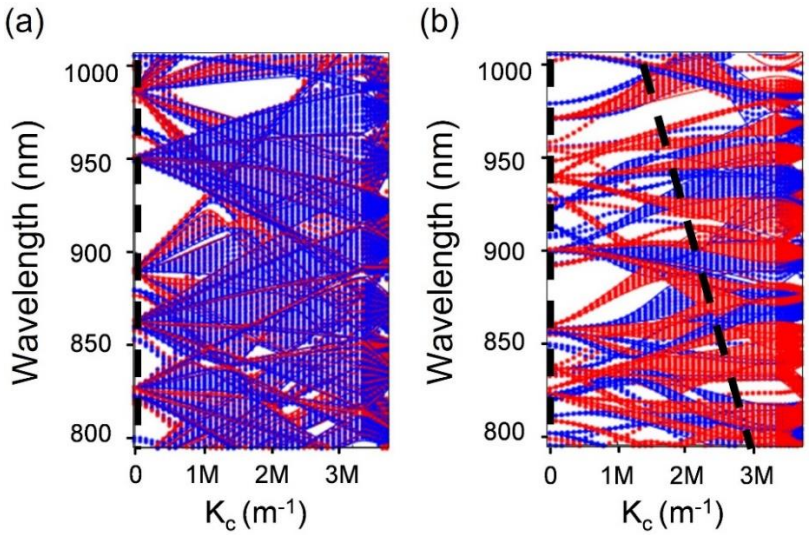


Fig. 7.20. Calculated band structure of silicon film with (a) small holes $(d = 100\,nm, p = 1000\,nm, and\ thickness, dSi = 1000\,nm)$ and (b) large holes $(d = 700\,nm, p = 1000\,nm, and\ thickness, dSi = 1000\,nm)$. Red curves represent TE and blue curves represent TM modes. Slanted dash lines are solutions for kc that couple into the lateral propagation for a vertically illuminating light source. Small hole structures exhibit solutions only for the finite number of the eigenmodes with $k = 0$ (vertical dashed line), while large hole structures essentially have both solutions $k = k_c\ and\ k = 0$ (vertical and slanted dash lines) with the eigenmodes, pronouncing enhanced coupling phenomena and laterally propagated optical modes.

Next, the influence of the size of the holes on the formation of lateral optical modes and the corresponding field distribution is studied. Coupling phenomena are only observed in the photon-trapping structures, as presented previously in Fig. 7.5 (b). Low coupling phenomena are observed for the devices with hole sizes smaller than half the wavelength as shown in Fig. 7.21 (b), where photons cannot efficiently couple within the absorber layer. However, for the hole size comparable with the incident wavelength, the light can couple into the holes and leak out through the sides of the hole, as illustrated in Fig. 7.21 (c). The incident photons also reflect from the surface of photodetectors when the hole diameter is smaller than the incident wavelength, which is not the case for our most efficient fabricated devices. The hole diameters of our most optimized fabricated devices are comparable to the incident wavelength, similar to the one shown in Fig. 7.21 (c). In photodetectors with larger holes, photons accumulate in the x-z plane around the hole after coupling into laterally propagating modes and eventually getting completely absorbed there. Furthermore, the vertically illuminated light refracts at $atan(n)$ angle from the boundary

conditions, increasing light absorption in the active layer. Finally, the oxide layer of the SOI wafer underneath the sensors further contributes to the enhanced photon absorption by reflecting the photons in the direction of the device surface. The influence of coupling for smaller and bigger holes at different incident angles is also studied on the photon absorption as provided in the Fig. 7.2. photodetectors with larger holes $(d/p{\sim}0.77)$ exhibit noticeably higher light absorption irrespective of incident angles than devices with smaller holes. However, when illuminated with photons of longer wavelengths, a relatively higher photon absorption is obtained for the incident angle of 30° compared with 0° in both small and larger holes.

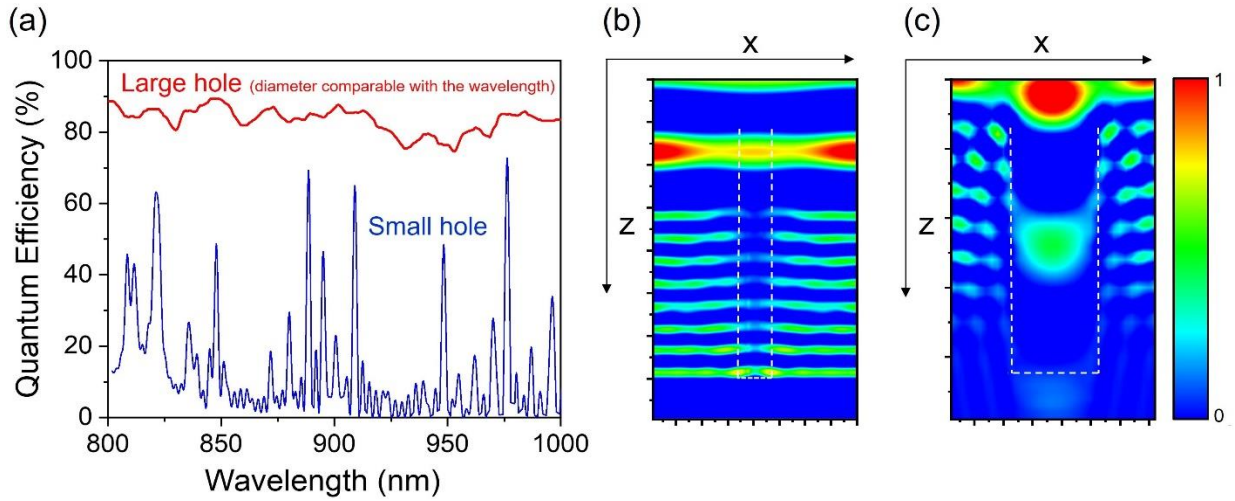
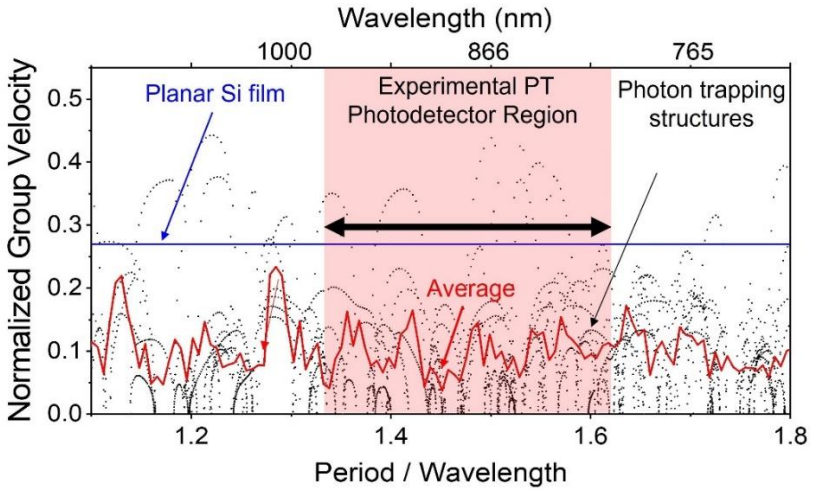


Fig. 7.21. (a) Calculated optical absorption in silicon with a small hole $(d = 100\,nm, p = 1000\,nm, and\ thickness, dSi = 1000\,nm)$ compared with the absorption of the large hole $(d = 700\,nm, p = 1000\,nm, and\ thickness, dSi = 1000\,nm)$. (b,c) FDTD simulations exhibit optical coupling and the creation of lateral modes. Low coupling and photonic bandgap phenomena are observed for the hole size smaller than the half-wavelength (b). Larger holes that are comparable to the wavelengths of the incident photons facilitate a higher number of optical modes and enhanced lateral propagation of light (c).

7.4.7 Reduced group velocity in photon-trapping silicon (slow light) and enhanced optical coupling to lateral modes contribute to enhanced photon absorption

Slow light with reduced group velocity increases absorption efficiency due to the augmented light-matter interactions. The group velocity was calculated from the band diagram as $u_g = d\omega/dk$ under TE polarization modes, as presented in Fig. 7.22. The group velocity in bulk Si was

calculated as c/n, where c is the light velocity and n is the refractive index of Si at 850 nm. The normalized frequency of our experimental structures is between 1.3 to 1.6. Herein, the group velocity in most modes for the normalized frequency between 1.3- 1.6 is significantly lower than the group velocity of light in bulk Si. The average group velocity for the modes was also calculated, as shown by the red line, indicating a conspicuously lower average group velocity of the photon trapping structures compared to that of Si without such surface structures.



7.22. Reduced group velocity in photon-trapping silicon (slow light) and enhanced optical coupling to lateral modes contribute to enhanced photon absorption. The normalized frequency (period/wavelength) pronouncing between ~1.3 - 1.6 is significantly lower than the light group velocity in the bulk Si (blue line). The red curve is an averaged group velocity for Si photon trapping structures which exhibits a distinctly lower value in our fabricated devices.

Light trapping surface structures have been demonstrated to be capable of enabling enhanced optical density of states (DOS) with light enhancement beyond the ray optic limit [15][16], the DOS was also calculated as an integral over the wavevector for a given frequency, $\rho(\omega) = \int \{\frac{d^d k}{(2\pi)^d}\} \delta(E - E(k)), d \; and \; E$ are differential dimension and energy, respectively. For the 2D photonic crystals, DOS could be approximated as $\rho_{2D}(\omega) = 4\epsilon\omega/\pi c^2$ [12]. The DOS of the photon trapping photodetectors is found to be higher than the photodetectors with planar surfaces, as provided in Fig. 7.23. The photodetectors with micro-hole periods shorter than the incident wavelengths exhibit noticeably low DOS compared to the periods comparable to and slightly

longer than the wavelengths. The designed and fabricated photodetectors closely match with the shaded area on the right half of Fig. 7.23 exhibiting high DOS for the frequencies higher than 1.0 (periods are comparable to or slightly longer than the incident wavelengths). Nevertheless, the region with high values of p/λ needs more Fourier components, and the maximum peaks of the DOS are not as pronounced as expected, while there is a constant increase of the optical mode density with p/λ. We conclude that observed absorption enhancement in Si is a combined effect of slow light with reduced group velocity, the enhanced photonic DOS, lateral propagation of a large number of optical modes, and efficient coupling of incident photons to the photon-trapping structures integrated on the Si surface. The cumulative impacts of the aforementioned processes help Si enhance light absorption by more than 20x and exceed the intrinsic absorption limit of GaAs.

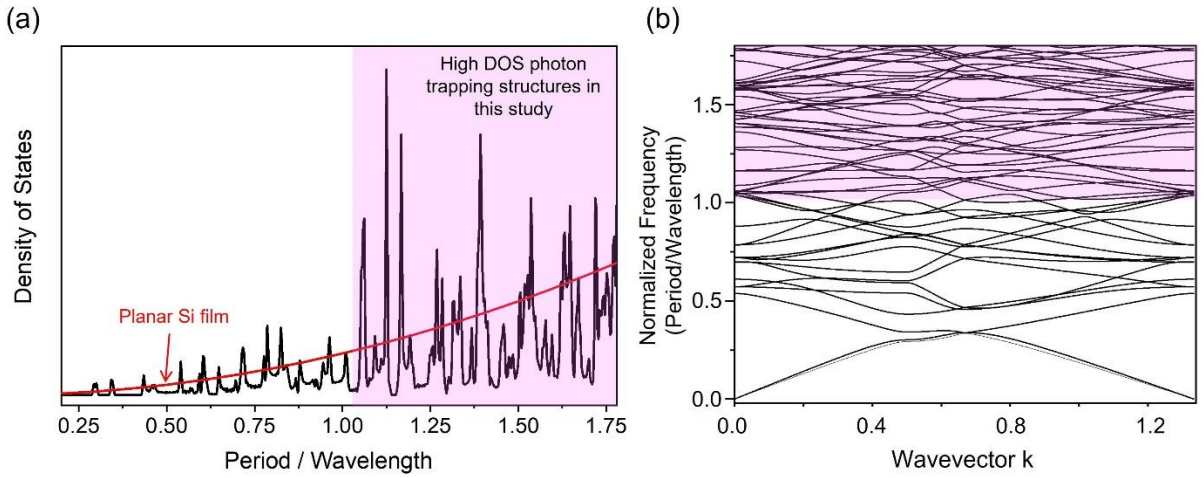


Fig. 7.23. High density of states (DOS) in photon trapping photodetectors. (a) High peaks in the DOS are observed for frequency (period/wavelength) points higher than (shaded region). The red line shows the DOS for the planar devices. (b) Normalized energy band structure of photon-trapping photodetectors with a hole diameter and period ratio $(d/p)\ of$ 0.7.

References

[1] V. S. Vavilov, “Handbook on the physical properties of Ge, Si, GaAs and InP byA Dargys and J Kundrotas,” *Uspekhi Fiz. Nauk*, vol. 166, no. 7, pp. 807–808, 1996.

[2] C. Schinke *et al.*, “Uncertainty analysis for the coefficient of band-to-band absorption of crystalline silicon,” *AIP Adv.*, vol. 5, no. 6, p. 67168, 2015.

[3] T. O. M. Tiedje, E. L. I. Yablonovitch, G. D. Cody, and B. G. Brooks, “Limiting efficiency of silicon solar cells,” *IEEE Trans. Electron Devices*, vol. 31, no. 5, pp. 711–716, 1984.

[4] Y. U. Peter and M. Cardona, *Fundamentals of semiconductors: physics and materials properties*. Springer Science \& Business Media, 2010.

[5] Z. Zhou, B. Yin, and J. Michel, “On-chip light sources for silicon photonics,” *Light Sci. \& Appl.*, vol. 4, no. 11, pp. e358--e358, 2015.

[6] M. Veldhorst, H. G. J. Eenink, C.-H. Yang, and A. S. Dzurak, “Silicon CMOS architecture for a spin-based quantum computer,” *Nat. Commun.*, vol. 8, no. 1, pp. 1–8, 2017.

[7] T. G. Mayerhöfer, S. Pahlow, and J. Popp, “The Bouguer-Beer-Lambert law: Shining light on the obscure,” *ChemPhysChem*, vol. 21, no. 18, pp. 2029–2046, 2020.

[8] A. Beer, *Grundriss des photometrischen Calcüles: mit in den Text eingedruckten Holzschnitten*. Vieweg, 1854.

[9] S. Adachi, “Optical dispersion relations for GaP, GaAs, GaSb, InP, InAs, InSb, Al x Ga1- x As, and In1- x Ga x As y P1- y,” *J. Appl. Phys.*, vol. 66, no. 12, pp. 6030–6040, 1989.

[10] E. D. Palik, *Handbook of optical constants of solids*, vol. 3. Academic press, 1998.

[11] E. Yablonovitch and G. D. Cody, “Intensity enhancement in textured optical sheets for solar cells,” *IEEE Trans. Electron Devices*, vol. 29, no. 2, pp. 300–305, 1982.

[12] K. X. Wang, Z. Yu, V. Liu, A. Raman, Y. Cui, and S. Fan, “Light trapping in photonic crystals,” *Energy \& Environ. Sci.*, vol. 7, no. 8, pp. 2725–2738, 2014.

[13] K. Rush, S. Draving, and J. Kerley, “Characterizing high-speed oscilloscopes,” *Ieee Spectr.*, vol. 27, no. 9, pp. 38–39, 1990.

[14] C. Bartolo-Perez *et al.*, “Maximizing Absorption in Photon-Trapping Ultrafast Silicon Photodetectors,” *Adv. Photonics Res.*, vol. 2, no. 6, p. 2000190, 2021.

[15] S. Mokkapati and K. R. Catchpole, “Nanophotonic light trapping in solar cells,” *J. Appl. Phys.*, vol. 112, no. 10, p. 101101, 2012.

[16] D. M. Callahan, J. N. Munday, and H. A. Atwater, “Solar cell light trapping beyond the ray optic limit,” *Nano Lett.*, vol. 12, no. 1, pp. 214–218, 2012.

[17] S. Yokogawa *et al.*, “IR sensitivity enhancement of CMOS Image Sensor with diffractive light trapping pixels,” *Sci. Rep.*, vol. 7, no. 1, pp. 1–9, 2017.

[18] B. J. Park *et al.*, “Deep trench isolation for crosstalk suppression in active pixel sensors with 1.7 $μ$m pixel pitch,” *Jpn. J. Appl. Phys.*, vol. 46, no. 4S, p. 2454, 2007.

[19] A. Tournier *et al.*, “Pixel-to-pixel isolation by deep trench technology: Application to CMOS image sensor,” in *Proc. Int. Image Sensor Workshop*, 2011, pp. 12–15.

[20] E. P. Devine *et al.*, “Single microhole per pixel in CMOS image sensors with enhanced optical sensitivity in near-infrared,” *IEEE Sens. J.*, vol. 21, no. 9, pp. 10556–10562, 2021.

[21] A. Taflove, S. C. Hagness, and M. Piket-May, “Computational electromagnetics: the finite-difference time-domain method,” *Electr. Eng. Handb.*, vol. 3, pp. 629–670, 2005.

[22] M. I. Hossain *et al.*, “Perovskite color detectors: Approaching the efficiency limit,” *ACS Appl. Mater. \& interfaces*, vol. 12, no. 42, pp. 47831–47839, 2020.

[23] B. E. Bayer, “Color imaging array.” Google Patents, 1976.

[24] C. Park and M. G. Kang, “Color restoration of RGBN multispectral filter array sensor images based on spectral decomposition,” *Sensors*, vol. 16, no. 5, p. 719, 2016.

[25] Y. Gao *et al.*, “Photon-trapping microstructures enable high-speed high-efficiency silicon photodiodes,” *Nat. Photonics*, vol. 11, no. 5, pp. 301–308, 2017.

[26] Y. Gao *et al.*, “High speed surface illuminated Si photodiode using microstructured holes for absorption enhancements at 900--1000 nm wavelength,” *ACS Photonics*, vol. 4, no. 8, pp. 2053–2060, 2017.

[27] I. Oshiyama *et al.*, “Near-infrared sensitivity enhancement of a back-illuminated complementary metal oxide semiconductor image sensor with a pyramid surface for diffraction structure,” in *2017 IEEE International Electron Devices Meeting (IEDM)*, 2017, pp. 14–16.

[28] C.-F. Han, J.-M. Chiou, and J.-F. Lin, “Deep trench isolation and inverted pyramid array structures used to enhance optical efficiency of photodiode in CMOS image sensor via simulations,” *Sensors*, vol. 20, no. 11, p. 3062, 2020.

[29] H. Cansizoglu *et al.*, “Surface-illuminated photon-trapping high-speed Ge-on-Si photodiodes with improved efficiency up to 1700 nm,” *Photonics Res.*, vol. 6, no. 7, pp. 734–742, 2018.

[30] S. Ghandiparsi *et al.*, “Up to 1700nm broadband high-efficiency surface-illuminated Ge/Si photodiode with microhole array,” in *Integrated Photonics Research, Silicon and Nanophotonics*, 2019, pp. IT3A--3.

[31] Y. Horie *et al.*, “Visible wavelength color filters using dielectric subwavelength gratings for backside-illuminated CMOS image sensor technologies,” *Nano Lett.*, vol. 17, no. 5, pp. 3159–3164, 2017.

[32] M. Oehme *et al.*, “Backside Illuminated ‘Ge-on-Si’ NIR Camera,” *IEEE Sens. J.*, vol. 21, no. 17, pp. 18696–18705, 2021.

[33] A. Abedin, “Germanium layer transfer and device fabrication for monolithic 3D integration,” KTH Royal Institute of Technology, 2021.

[34] F. Schäffler, “High-mobility Si and Ge structures,” *Semicond. Sci. Technol.*, vol. 12, no. 12, p. 1515, 199

Chapter 8 Single Microhole per Pixel in CMOS Image Sensor with Enhanced Optical Sensitivity in visible to Near-Infrared (NIR) spectrum

8.1 Optimizing Si CMOS image sensor with a single microhole per pixel in the NIR

The optimization of silicon photodiode-based CMOS sensors with backside-illumination for 300–1000 nm wavelength range is studied. It is demonstrated that a single hole on a photodiode increases the optical efficiency of the pixel in near-infrared wavelengths. A hole with optimal dimensions enhanced optical absorption by 60% for a 3 μm thick Si photodiode, which is 4 orders better than that for comparable flat photodiodes. The results show that there is an optimal size and depth of the hole that exhibits maximal absorption in blue, green, red, and infrared. Crosstalk is successfully reduced by employing thin trenches between pixels of 1.12 μm^2 in size.

8.1.1 Device Design

For this study, the stacked low-noise structure similar to the one proposed by Sony Corporation is considered [1, 2], which is back-side illuminated and layered over a chip with signal processing circuits. Besides just improving the chip size, stacking technology also improves the dark characteristics (such as noise and white pixels), by optimizing the sensor process independently. Several designs are compared for the optimization purposes: flat (planar) pixel with no surface photon-trapping structure pixel with an inverted pyramid, cylindrical, and crossed rectangular holes per pixel as can be seen in fig. 8.1. The deep trench structure [3, 4] with Si-SiO_2 interface is used as a barrier against electron diffusion and assists in confining light within the pixels by acting as a reflector. The pixels designs are 1.12 μm^2 in size and 3 μm deep pixels with trenches of 150 nm width and 2.5 μm depth that showed a reasonable reduction in crosstalk [5]. Pixels designs dimensions were varied for the cylindrical holes, inverted pyramid holes, and crossed rectangular holes to determine their optimal parameters. The CMOS image sensor model includes

red, green, and blue filters with a thickness of 900 nm, lenses, antireflection coating, and a 3 μm thick Si on SOI substrate, and micro-lens with a radius of 1 μm and a thickness of 500 nm. The wavelength of the normal plane wave source varied in the range of 300 and 1100 nm.

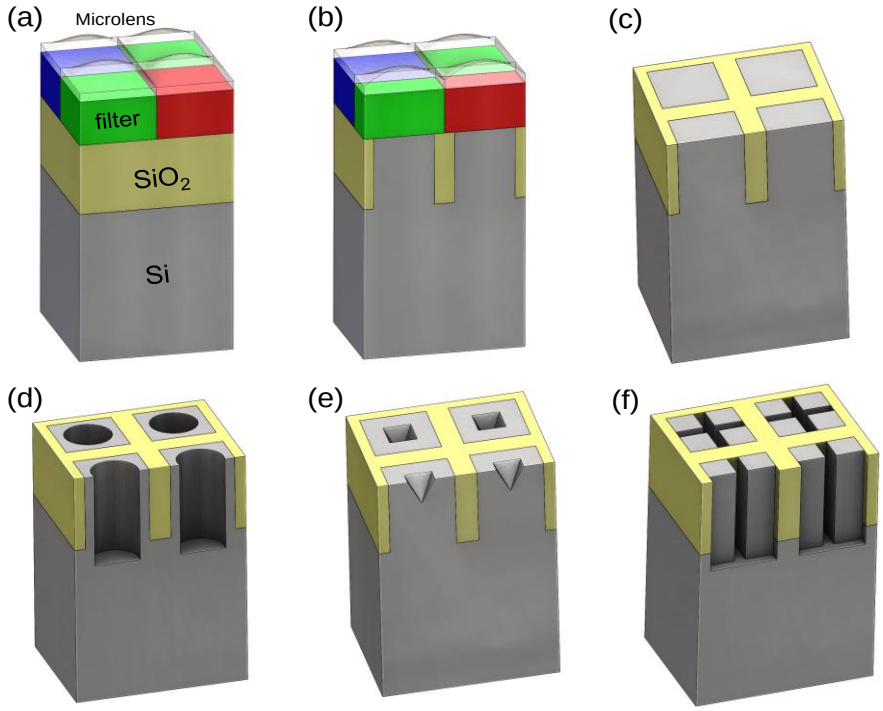


Fig. 8.1. Schematic diagram of CMOS image pixels: (a,b) View of the pixels with micro lenses, color filters, and Deep Trench Isolation (DTI). (c) Cross-section view of the image pixels (without the micro lens and color filter) showing conventional planar image pixel. (d) cylindrical holes per image pixel (e) Inverted pyramid per image pixel. (f) Cross trenches per image pixel. DTI separation between the pixels is also shown (yellow coded).

8.2 Optical simulation methodology

Finite Difference Time Domain (FDTD) Lumerical tool [6] is used to solve Maxwell's curl equations for the unit cell of Bayer array, where Bloch boundary conditions around the cell and Perfectly Matched Layer (PML) in the direction normal to the surface were considered. The single hole can couple light into the parallel to-the-interface modes. Next, we analyzed the array of the holes and coupling of the parallel to the interface modes into the guided resonant modes. These resonant modes or the leaky modes theoretically leads to the increase in optical absorption. The hole parameter optimization was done based on the theoretical calculation.

8.2.1 Results and discussion

The optical efficiency (OE) is given by the Poynting vector normal to the surface (P) measured around the cells:

$$OE = \frac{P_{in} - P_{out}}{P_{incident}} \quad (8.1)$$

Where $P_{incident}$ is the Poynting vector of the incident light calculated above the lenses and filters. We assume that the quantum efficiency is proportional to the optical efficiency [7].

8.2.2 Bayer Filter Transmittance

Bayer filter array with a commonly used color filter array is modeled as (Red, Green, Green, Blue) RGGB [Fig. 8.1 (a,b)] [8]. The pixels are modeled with a Bayer array with a commonly used color filter parameters as can be found in table 8.1 [2, 5, 8, 9]. The filter's spectral response is presented in Fig. 8.2. For the simulation setups, the transmittance of the pigment filters with 900 nm thickness is used [10]. The maximum optical efficiency for the Bayer filter is determined by its transmittance [Fig. 8.2]. For these simulations, they are OE_{blue} = 80% at 440 nm, OE_{green} = 65% at 550 nm, and OE_{red} = 85% at 650 nm, and transparent in the near infrared.

λ (nm)	Blue		Green		Red	
	n	k	n	k	n	k
300	1.55	0.055	1.62	0.4	1.54	0.415
400	1.54	0.07	1.6	0.5	1.54	0.325
500	1.54	0.215	1.58	0.405	1.53	0.155
600	1.54	0.8	1.57	0.05	1.53	0.048
700	1.53	0.45	1.57	0.11	1.52	0.033
800	1.53	0.455	1.57	0.105	1.52	0.375
900	1.52	0.465	1.56	0.09	1.52	0.0185
> 1000	1.52	0.39	1.56	0.055	1.52	0.015

Table 8.1. Filters parameters

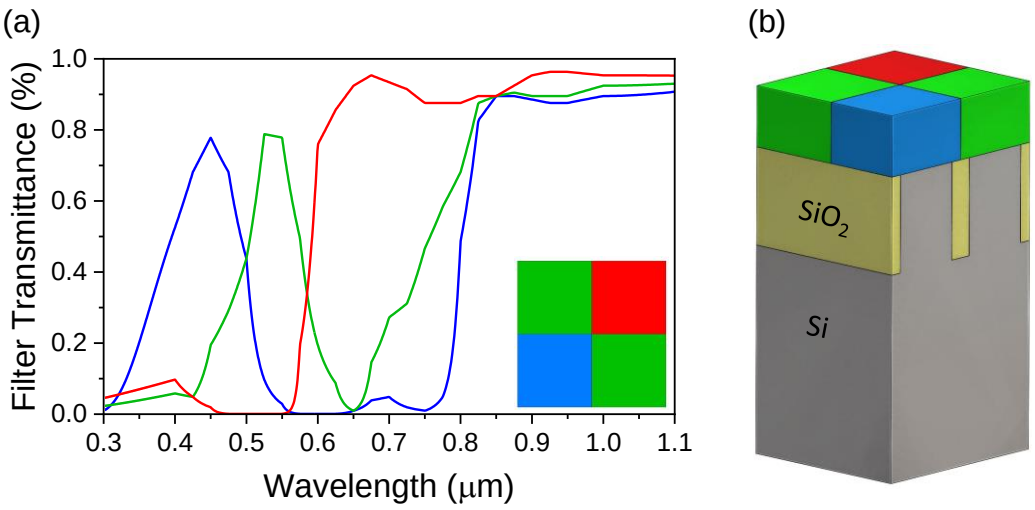


Fig. 8.2. Bayer filter transmittance. (a) Simulated spectral response of Bayer filter. (b) Planar pixel with Bayer color filters.

8.2.3 Optical optimization of cylindrical, inverted pyramid and crossed rectangular photon trapping structure

The pixels are optimized through varying the micromoles size, profile, and depth. The diameter of the cylindrical holes was chosen to be 700 nm since it was demonstrated to be optimal previously in [5, 11, 12] and varied their depths. Inverted pyramid dimensions are correlated to the fabrication process, so only the length of the opening sides is varied. The crossed rectangular hole is composed of two, overlapping rectangular holes that are crossed in the center and positioned to reach the trenches on each side, therefore, the width and the depth of the rectangular holes are varied. The optimization results of the micromoles are shown in Fig. 8.3 and 8.4 for the 850 and 940 nm wavelengths. All pixels, blue, green, and red have the same OE in infrared. The results in Fig. 8.3 (a) show the OE for different hole depths for the cylindrical holes with diameters of 700 nm. The optimal depth for the cylindrical holes is found to be around 2 μm. The variation of the depth shows that OE in infrared increases with the depth and stabilizes after 2 μm. The OE in blue also increases up to a depth of 2 μm but begins to decrease after that. This could be explained by how the maximum absorption corresponds to a resonant behavior that happens at the smaller size for the smaller wavelength. A similar variation on the inverted pyramid

side length indicates that the optimal side length is close to 700-800 nm for each pyramid edge as can be seen in Fig. 8.3 (b). The pyramid size optimizations show that increasing size produces better absorption for the near-infrared and reduces the absorption for the blue pixels. The optimal side length of 700 nm results in a balance between the OE of the blue and the near-infrared wavelengths. The crossed rectangular holes' depth and width are also optimized.

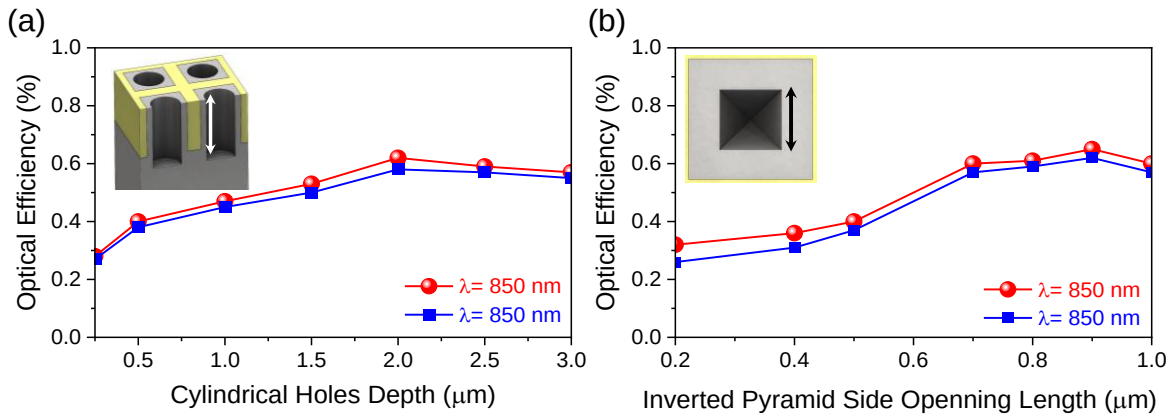


Fig. 8.3. Optical optimization. (a) Optical efficiency vs. cylindrical holes depth. (b) Optical efficiency vs. inverted pyramid side opening length.

Figure. 8.4 shows that the optimal depth for the crossed rectangular holes is about 2.2 μm and 2.5 μm, with a width of 250 nm. It is about the same as for cylindrical holes. The impact of the rectangular holes' width on OE is almost the same over the range from 150-400 nm [Fig. 8.3 (b)], the optimal width is about 200- 300 nm for the depth of 2.5 μm nm. The OE of such image sensors calculated for a longer wavelength of 940 nm are encouraging and reach over 50%, while for wavelengths longer than 1 μm, the OE rapidly decreases. Microholes provide smaller reflection for reasons similar to the Lambertian reflector [13]. It supports trapping the light in Si and bending the normal incident light into lateral modes, as is numerically and experimentally shown in chapters 4, 6, and 7 [11, 12, 14, 15]. While a guided resonant mode can be completely absorbed, high absorption can still be achieved with leaky modes that can propagate in the device long enough to be mostly absorbed.

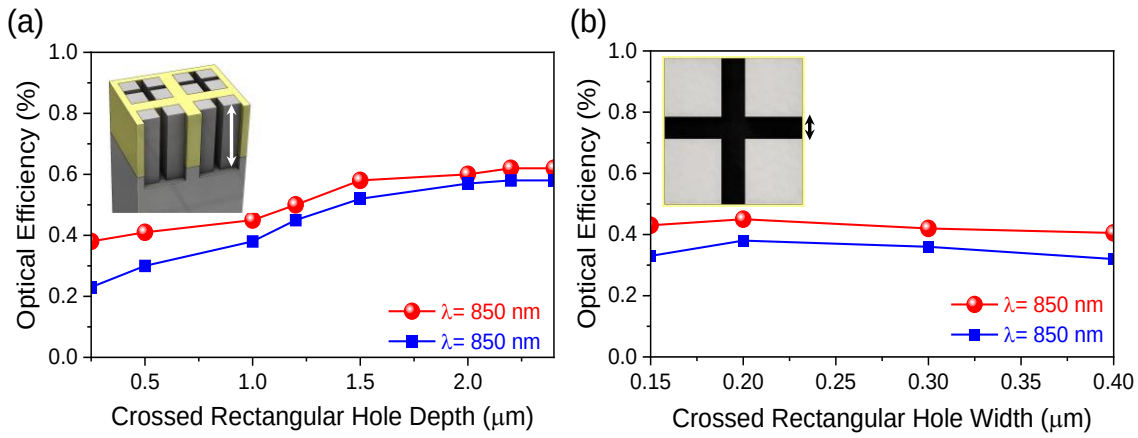


Fig. 8.4. Optical optimization. (a) Optical efficiency vs. crossed rectangular hole depth. (b) Optical efficiency vs. crossed rectangular hole width.

8.2.4 Improved Optical Sensitivity in Near-Infrared for cylindrical, inverted pyramid, and crossed rectangular hole per pixel

The optical sensitivity profile of flat/planar (no photon-trapping structure on the surface) pixels is shown in Fig. 8.5 (a) Such flat pixels are studied here as a reference. The optimized results for the cylindrical holes, inverted pyramids, and crossed rectangular holes are shown in Fig. 8.5 and 8.6.

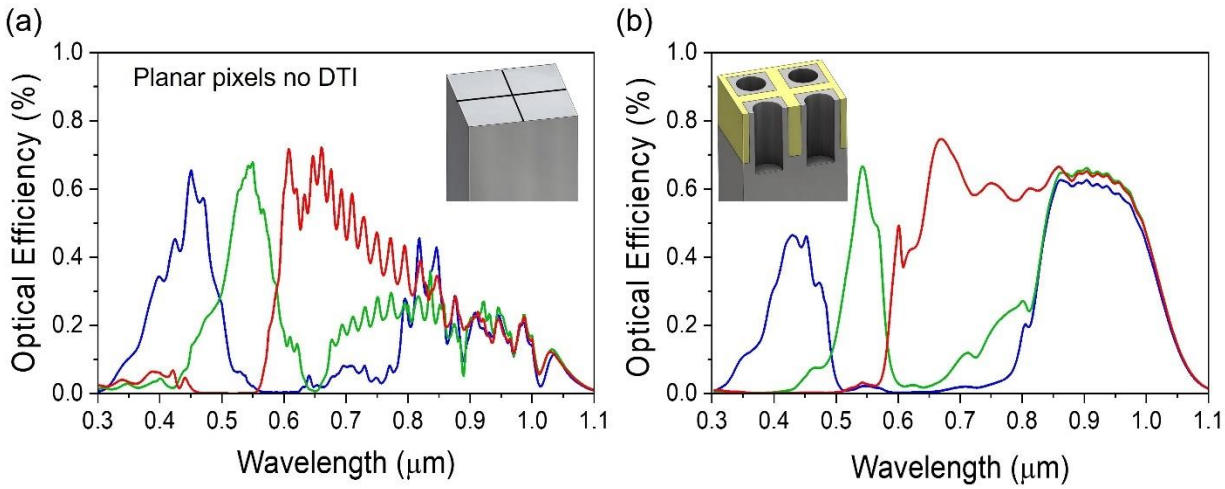


Fig. 8.5. (a) Optical efficiency for planar pixels without deep trench isolation (DTI). (b) Optical efficiency for cylindrical hole per pixel with DTI.

All the microstructures increase the absorption in the pixels for blue, green, and red with higher enhancement in the green and red wavelength spectrum. Despite enhancing the OE, the

integration of holes in the sensors can increase the crosstalk between pixels. The crosstalk in the visible region is smaller than the near-infrared owing to the inherent material properties of the crystalline silicon. Hence, the color separation in the blue and green region is better than the green and red region, as it is expected to obtain a better color separation and low color error there. However, as we can see in these figures, the crosstalk was effectively reduced by the implementation of trenches without any decrease in the OE compared to that exhibited by the flat pixels.

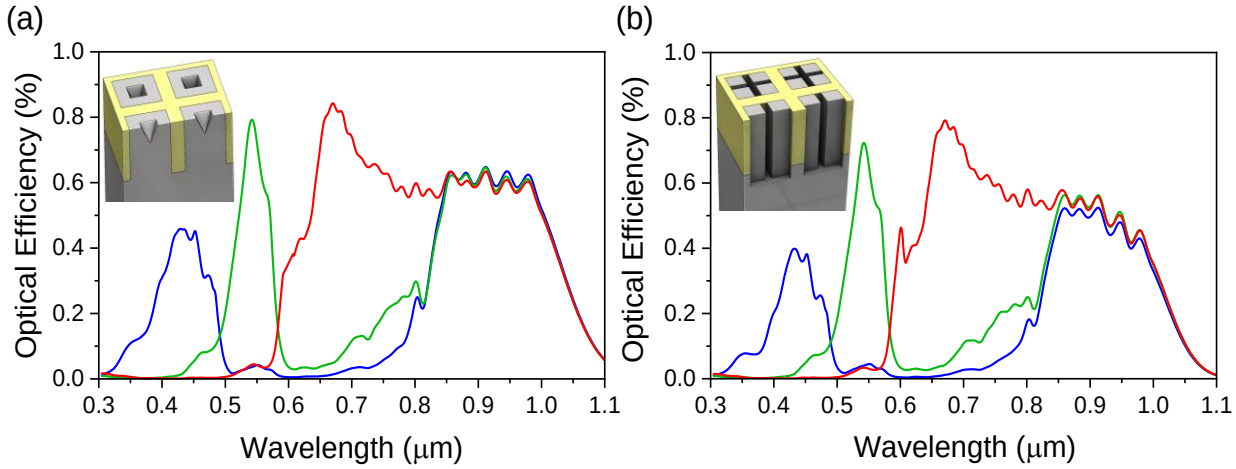


Fig. 8.6. (a) Optical efficiency for inverted pyramid design per pixel with DTI. (b) Optical efficiency for crossed rectangular hole per pixel with DTI.

In the near-infrared wavelengths, the OE of the 3 μm thin Si CMOS image sensors for the designed geometries is higher than 60%. The optimized structures, diameters, profiles, and depths for a single-hole per pixel provides insight for designing enhanced, optically sensitive image sensors in near-infrared. However, single-hole pixel has increased crosstalk; however, implementing trenches with dimensions of 250 nm width and 2.5 μm depth between pixels efficiently reduces the crosstalk to the normal level. The introduction of deep trench isolation (DTI) concept will be further optimized and discussed in the next section.

8.3 Single microhole per pixel in Si CMOS image with Enhanced Optical Sensitivity in Near-Infrared and reduced crosstalk

Single hole per pixel in Si CMOS image sensor increases the optical efficiency of the pixel. In near-infrared wavelengths, the enhancement allows 70% absorption in a 3 μm thick Si. It is 4× better than that for the flat/planar pixel. A comparison of different shapes and sizes of single hole and hole arrays are studied in this section. Optimum size and shape in single hole-based pixels contribute to stronger enhancement of optical efficiencies. The crosstalk is successfully reduced by employing trenches between pixels. The optimized dimensions of the trenches to achieve minimal pixel separation for 1.12 μm^2 pixels.

8.3.1 Device design and optical simulation

Si CMOS image sensor model includes lenses, red, green, and blue Bayer filters with a thickness of 900 nm, antireflection coating, and a 3 μm thick Si on a SOI substrate as illustrated in Fig. 8.2. A micro-lens with a radius and thickness of 1 μm and 500 nm is also considered on the top of each sensor. Additionally, different shapes and sizes of holes were considered as photon-trapping structures to enhance the absorption efficiency or optical efficiency (OE) of the sensors, where trenches filled with silicon oxide (SiO_2) are considered. Herein, several designs are compared: flat/planar conventional pixel without surface photon-trapping structure including microlens and Bayer filters [Fig. 8.7 (a)], an array of holes with 400 × 400 nm inverted pyramids [Fig. 8.7 (b)], pixel with a single inverted pyramid of 900 × 900 nm [Fig. 8.7 (c)], a funnel hole with a diameter of 900 nm [Fig. 8.7 (c)] and a cylindrical hole with a diameter and depth of 800 nm and 2 μm, respectively [Fig. 8.7 (d)]. Figure. 8.7 (e) present a schematic of a PT design with an angle of 60-degree wall that merges with 800 nm diameter and 2 μm deep cylindrical hole. A plane wave source was considered with normal incidence to the surface for the wavelengths ranging between 300 and 1100 nm. The Finite Difference Time Domain (FDTD) [6] provided by the Lumerical software package was used to solve Maxwell's curl equations numerically for the unit cell of the Bayer array [Fig. 8.7].

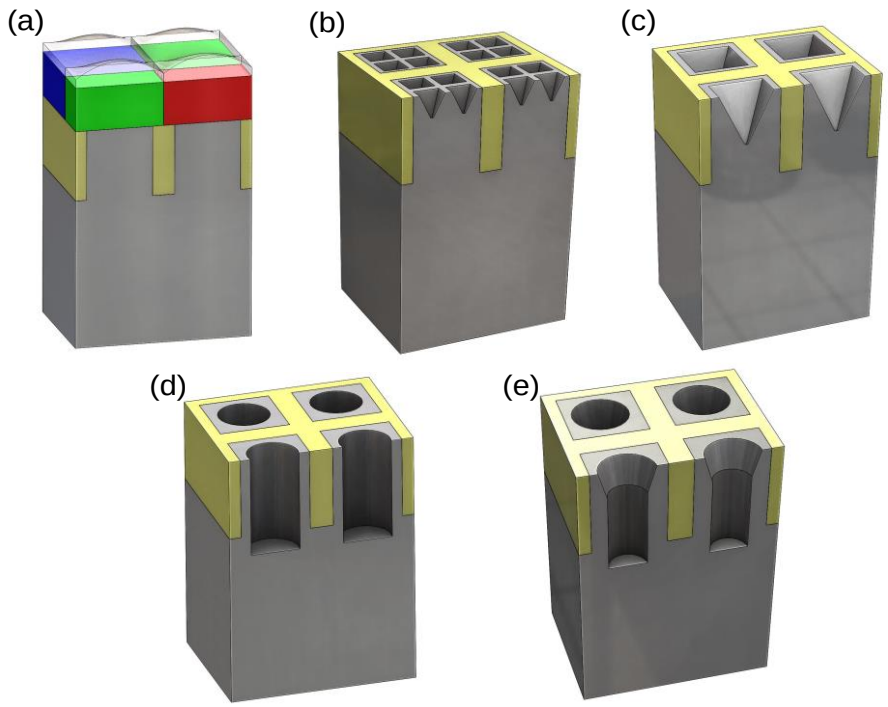


Fig. 8.7. Schematic diagram of Si CMOS image pixels: (a) view of the pixel with micro lenses, color Bayer filters, and DTI. (b) Inverted pyramids array 4X4 per pixel. (c) Single inverted pyramid per pixel. (d) Single cylindrical hole per pixel. (e) Single funnel holes per pixel. Deep trench isolation (DTI) separation between the pixels is shown (yellow coded).

8.3.2 Results and discussion

The Poynting vector (*P*) was measured around the cells. For a given current *J* in the pixel and electric field, *E*, the energy absorbed in volume *V* is calculated by applying the divergence theorem for stable state as below:

$$P_{abs} = \int_V \frac{1}{2} Re(E \cdot J^*) \cdot dv = \int_V \frac{1}{2} \nabla \cdot Re(E \times H^*) \cdot dv = -\oint_S \frac{1}{2} [Re(E \times H^*) \cdot \vec{n}] ds \quad (8.2)$$

where, S is the surface that surrounds the volume V and $\vec{n}$ is the unit vector normal to the surface S. Thus, to calculate the optical absorption in each pixel power, we integrate the Poynting vector normal to the surface over the surface of the depletion region of the pixel. The results present the difference between the real parts of the Poynting flux entering the volume at the surface between the filters and the pixel ($P_{in} = \mathrm{Re}\left(E \times H^*\right)$), and the Poynting flux leaving the pixel (P_{out}), that are simulated with FDTD method. As the optical efficiency is calculated by using the Equation (8.1). It should be noted that the calculated optical efficiencies are not normalized.

8.3.3 Enhanced Optical Sensitivity in Near-Infrared CMOS image sensor by utilizing photon-trapping designs per pixel and deep trench isolation (DTI)

The influence of integrating such photon-trapping structures was investigated on the optical efficiency, while nano/microhole structures and their dimensions were varied. The investigated photon-trapping holey structures are: (a) inverted pyramids of 400 × 400 nm array [1], (b) cylindrical, (c) single inverted pyramid of 900 × 900 nm, and (d) funnel shape. Furthermore, deep trench isolation was used between pixels to reduce the crosstalk. Silicon image sensors integrated with all the nanohole photon-trapping structures mentioned above were simulated for optical efficiency as presented in fig. 8.8 and fig. 8.9. Figure. 8.8 (a,b) compares the simulated optical efficiency of the inverted pyramids of 400 × 400 nm array IR sensitivity enhancement of CMOS Image Sensor with diffractive light trapping pixels [15], and single inverted pyramid of 900 × 900 nm. While Fig. 8.9 (a,b) compares cylindrical hole and funnel-shaped hole, respectively. The solid lines represent the pixel with trenches of 250 nm width and 2.5 µm deep, whereas the dashed lines show the pixels without trenches. While the hole arrays increase the optical efficiency up to about 40% at the near-infrared (NIR) wavelengths, a single inverted pyramid hole of 900 × 900 nm can increase the optical efficiency to more than 60% at 850 nm wavelength.

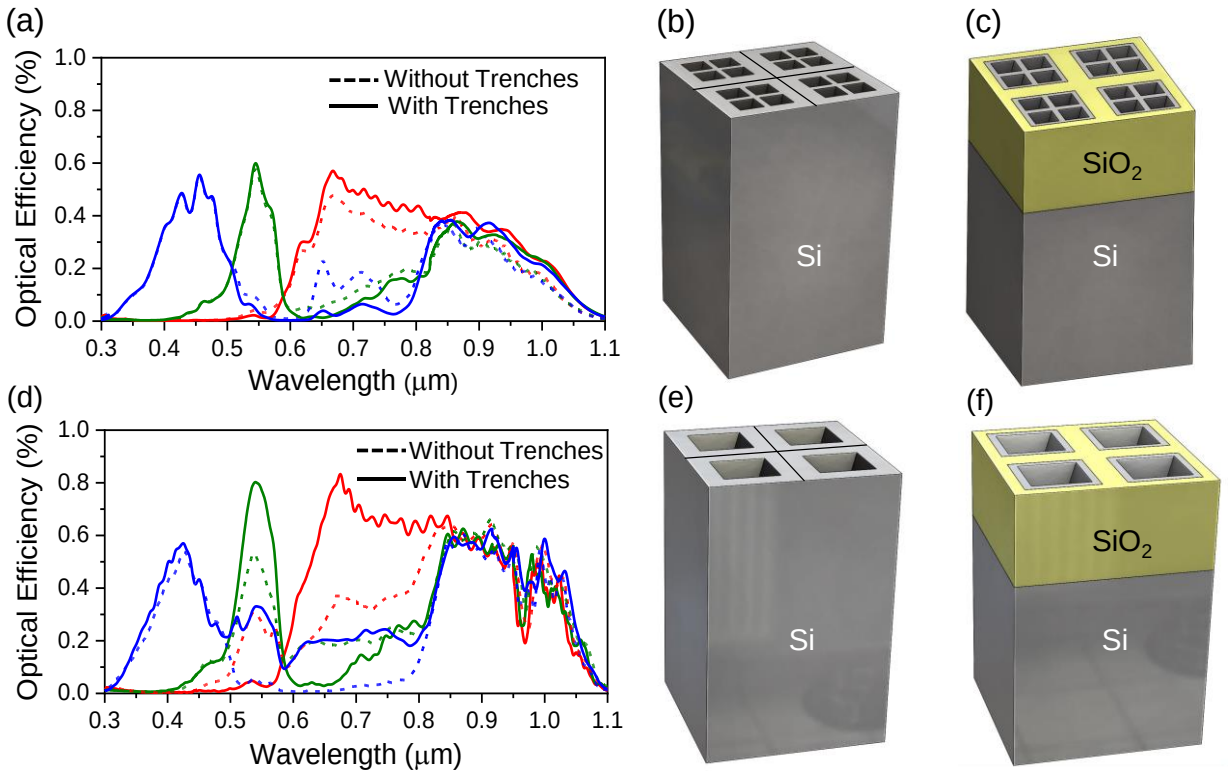


Fig. 8.8. Calculated optical efficiency with (solid) and without (dashed) DTI trenches. (a) Optical efficiency for inverted pyramids array per pixel. (b) Schematic of inverted pyramid array per pixel without trenches. (c) Schematic of inverted pyramid array per pixel with trenches. (d) Optical efficiency for inverted pyramid per pixel. (e) Schematic of inverted pyramid per pixel without trenches. (f) Schematic of inverted pyramid per pixel with trenches.

Moreover, an optimized single funnel-shaped holey photon-trapping structure can exhibit an optical efficiency up to 70% [Fig. 8.9 (b)]. The optical efficiencies of such image sensors calculated for a longer wavelength of 940 nm with encouraging results are also tabulated in table (8.2). For the wavelengths longer than 1.0 μm, the optical efficiency of the simulated image sensors sharply reduces and subsequently approaches to zero at 1.1 μm. Inverted pyramid and funnel shapes exhibit smaller reflection due to an effect that is similar to the Lambertian reflector. While a guided resonant mode can be completely absorbed, high absorption can still be achieved with leaky modes that can propagate in the device long enough to be mostly absorbed. All the microstructures increased the absorption in the pixels for blue, green, and red with higher enhancement in the green and red wavelength spectrum.

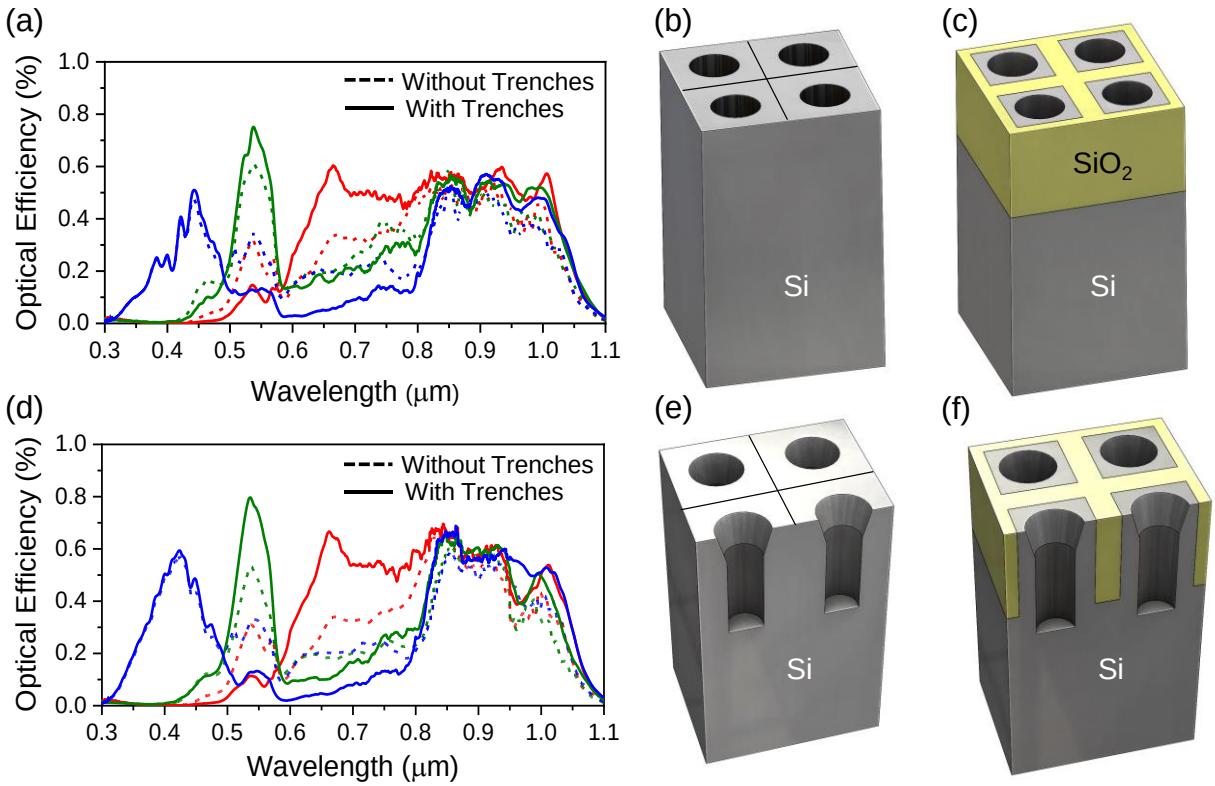


Fig. 8.9. Calculated optical efficiency with (solid) and without (dashed) DTI trenches. (a) Optical efficiency for cylindrical hole per pixel. (b) Schematic of cylindrical hole per pixel without trenches. (c) Schematic of cylindrical hole per pixel with trenches. (d) Optical efficiency for funnel hole per pixel. (e) Schematic of funnel hole per pixel without trenches. (f) Schematic of funnel hole per pixel with trenches.

Despite enhancing the optical efficiency, the integration of holes in the devices can increase the crosstalk between pixels. the crosstalk in the visible region is smaller than the near-infrared owing to the inherent material properties of the crystalline silicon. Hence, the color separation in the blue and green region is better than the red, expecting to be obtained a better color separation and low color error there [7].

8.3.4 Optimization of Deep Trenches Isolation (DTI) for cross talk reduction in single hole per pixel CMOS image sensor

The crosstalk can effectively be reduced by the implementation of trenches without any decrease in the optical efficiency. Table 8.2 shows the crosstalk index of pixel which is a ratio between the intensity of that pixel to the intensity from the side pixel. Hence, the calculated higher crosstalk index indicates a better crosstalk value or lower crosstalk. The crosstalk was calculated for a pair

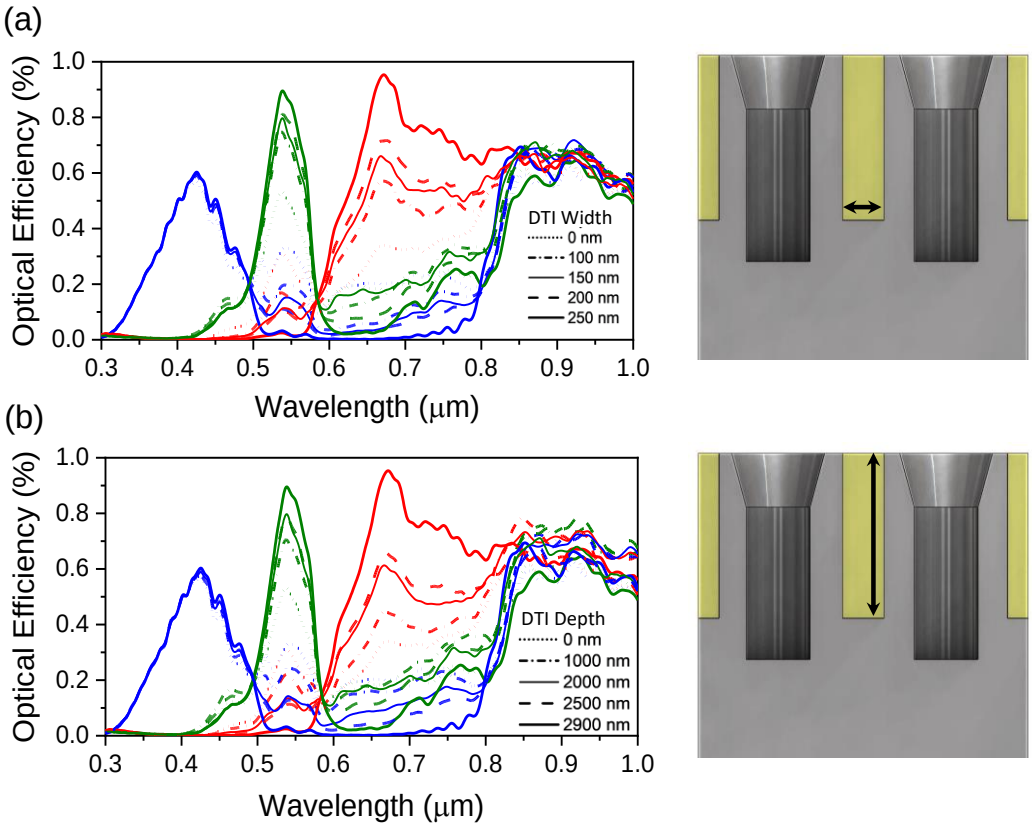
of colors as tabulated on the pixel color column, where the intensity impact of one-color pixel is calculated for the intensity from another color pixel. On other words, crosstalk index of red-green pair indicates the intensity color pixel of red color for the intensity from the green pixel. Table 8.2 represents crosstalk index with and without trenches for all the shapes studied, while the crosstalk index presented for the flat pixels is used as a reference. The flat pixels exhibit a very high crosstalk in red-green, green-blue, and blue-green, pronouncing crosstalk index of 4, 7.5, 2.97, respectively. However, the crosstalk was distinctly improved by introducing trenches between pixels as tabulated in Table 8.2. The trenches could be further optimized to provide the smallest crosstalk by varying their depths and thicknesses. In this section, the depth and width are the two degrees of freedoms in the design of deep trench isolation for the optimization.

Holes Design	Pixel color	Crosstalk index No DTI/DTI	OE(%) 850/940nm
Flat/planar conventional pixel	Red-Green Red-Blue	4 26	22/15
	Green-Red Green-Blue	20 7.5	
	Blue-Red Blue-Green	24 7.5	
Inverted Pyramids Array/pixel	Red-Green Red-Blue	6.1/26 2.6/17.9	35/20
	Green-Red Green-Blue	13.5/30 6.8/14	
	Blue-Red Blue-Green	24/24 9.97/30	
Single inverted Pyramid/pixel	Red-Green Red-Blue	1.6/14.7 4.8/63	60/50
	Green-Red Green-Blue	2.8/20 2.5/17.3	
	Blue-Red Blue-Green	50/24 6.2/130	
Single Cylindrical Hole/pixel	Red-Green Red-Blue	1.5/2.9 1.2/10.9	58/50
	Green-Red Green-Blue	2.1/5.6 1.9/5.5	
	Blue-Red Blue-Green	76/26 6/63	
Single Funnel Hole/pixel	Red-Green Red-Blue	1.34/6.9 1.3/19.9	**71/55**
	Green-Red Green-Blue	1.68/7.9 1.48/7.7	
	Blue-Red Blue-Green	21/24 5.5/30	

Table 8.2. Crosstalk index (Intensity of pixel/Intensity from side pixel) of the simulated image sensors integrated with photon-trapping holes/designs. conventional (planar) pixel is simulated as a reference. Higher crosstalk index indicates lower crosstalk.

The influence of DTI width and the depth is studied on the optical efficiency and the crosstalk mainly in the near-infrared wavelengths as demonstrated in Fig. 8.10. In this case, a single funnel-shaped or tapered hole per pixel with a size comparable to the wavelength is used to maximize the optical efficiency of such image sensors. First, the width of the trench is varied ranging from

0 nm to 250 nm. The simulated CMOS image sensor exhibits a reduced crosstalk by increasing the width of the trench as shown in Fig. 8.10 (a). In the next step, the depth of the trench is also varied from 0 nm to 2900 nm for the optical efficiency of the sensors as depicted in Fig. 8.10 (b), suggesting that the crosstalk can be decreased with the increase of the trench depth. However, such image sensor can be optimized with a reasonable crosstalk for the trench depth and width of 2500 nm and 150 nm, respectively. The crosstalk for a blue pixel from a red pixel is defined as a ratio between the response of the blue pixel near the 440 nm wavelength in the range +/− 10 nm to the response of the red pixel for the same wavelength range. In the case of near-infrared wavelengths, there will be an equal response from all three pixels and will be represented as a grayscale picture. The simulations show that while the crosstalk decreased, the optical efficiency is increased for all the colors due to the use of single holes with trenches. Single microhole per pixel image sensors studied here with enhanced absorption efficiency in the near infrared can be fabricated by standard CMOS compatible processes. We fabricated several photon trapping photodetectors integrated with microhole structures, including funnel-shaped, cylindrical, and inverted pyramid using wet or dry etching including surface treatment processes [11, 15-17].



8.10. Optimization of DTI (a) width and (b) depth in the CMOS image sensor. The influence of DTI width and depth was investigated in optical efficiency by varying them from 0 nm to 250 nm and 0 nm to 2900 nm, respectively.

So far, we have not fabricated an actual CMOS image sensor with such microhole structures per-pixel. However, Sony used anisotropic wet etching on 100 silicon to form inverted pyramid arrays [18], and Samsung utilized dry etched shallow trenches (backside scatter technology) to fabricate image sensors [19]. In this case, we can either wet etch a large single inverted pyramid or dry etch a cylindrical or funnel hole [11]. The single holes can be filled with SiO_2 and planarized for subsequent processing.

8.4 Single Micro-hole per Pixel for Thin Ge-on-Si CMOS Image Sensor with Enhanced Sensitivity up to 1700 nm

Germanium “Ge-on-Si” CMOS image sensor with backside illumination for the near-infrared (NIR) and mid-infrared (MIR) (wavelength range 300–1700 nm) detection is essential for optical sensor technology. The micro-holes help to enhance the optical efficiency and extend the range to the

1.7 μm wavelength. This section demonstrates an optimization for the width and the depth of the nano-holes for maximal absorption in the near-infrared. An imager with a thin Ge layer on Si-on-insulator (SOI) substrate with a 1.12 × 1.12 μm^2 pixel size was considered in this study. The results show a reduction in the cross talk by employing thin SiO_2 deep trench isolation (DTI) in-between the pixels. The results show a 26–50% reduction in the device capacitance with the introduction of hole. Such CMOS compatible Ge-on-Si sensors will enable a high density, ultra-fast and efficient NIR/MIR imaging.

8.4.1 Device design

This study considers Ge-on-Si backside-illuminated sensors layered over a signal processing circuit chip with a low-noise structure [4, 11, 20]. The simulations do not include the metal contacts. The contacts will add small optical losses that can reduce the results by a few percent. Novel IR transparent metals or highly doped polysilicon can also be used to avoid absorption losses. The pixel array is shown schematically in Fig. 8.11. Each pixel is 1.12 μm^2 wide and consists of a Si layer on SiO_2 and a thin layer of Ge on top of the Si layer. The thickness of Ge was varied from 150 nm to 1 μm. The Si thickness is 2-2.5 μm, and the total thickness of the Ge/Si stack is 3 μm. The buried SiO_2 layer reduces the transmittance from the thin absorbing layer by reflecting the illuminated electromagnetic waves. A lens of radius 1 μm is used at the top of each pixel, along with a filter between the lens and the Ge layer. The pixels are modeled with a Bayer array with a commonly used color filter parameters [10] as provided in table 8.1. The optical simulation methodology is similar to the discussion in section 8.1.2.

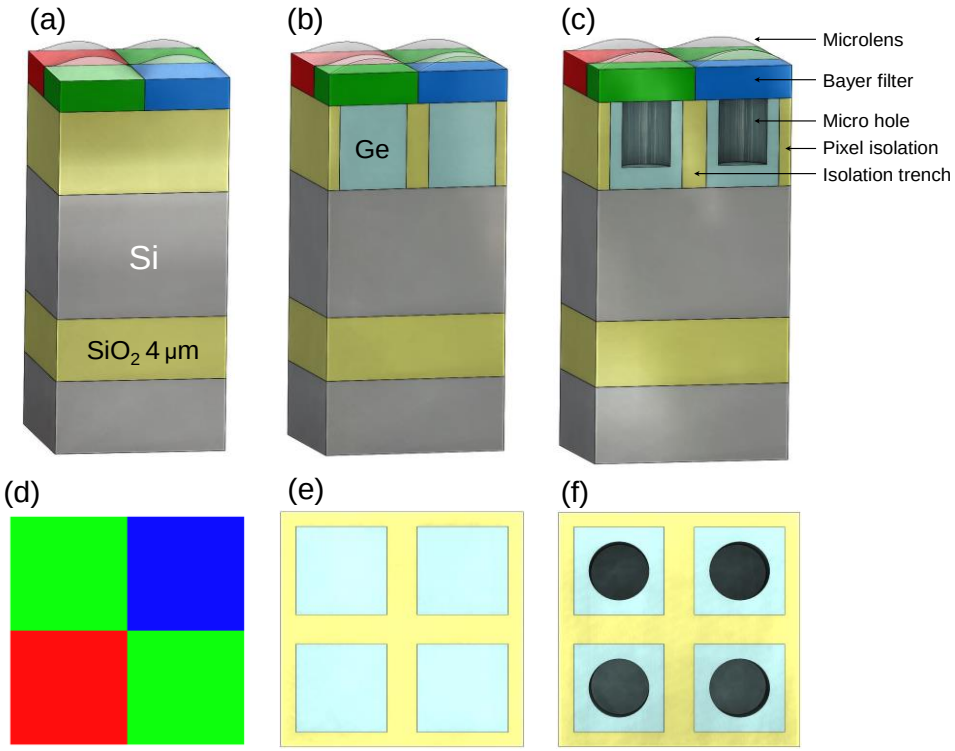


Fig. 8.11. Schematics of the Ge pixel. (a) 3D view of the image sensor with microlenses and filters. (b) Cross-sectional view of conventional (Flat) Ge pixel with oxide trenches. (c) A section of a pixel with an air-filled cylindrical hole per pixel with oxide trenches. (d) A top view of the Bayer filters. (e) Top-view of conventional Ge pixel with trenches. (f) Top-view of holes structures in Ge pixel with trenches. Ge thickness is varied from 150 to 500 nm, with a hole diameter of 800 nm, a depth of 3/4 of Ge thickness, and Si thickness of 2.5 µm. Illumination is normal to the surface from the top.

8.4.2 Results and discussion

8.4.2.1 Bayer Filter Transmittance

The optical transmittance after the filters is shown in Fig. 8.12. All filters are almost transparent at 1000 nm wavelength, and we assume they have the same characteristics in mid-infrared. In the 3D simulation setup, the transmittance associated with 900 nm thickness is used for the pigment filters [21, 22], the filters parameter is listed in table 8.1. For the wavelength higher than 1000 nm the simulations assumed the same filter parameters as for wavelength of 1000 nm. It means that the filters are almost transparent in Mid-infrared.

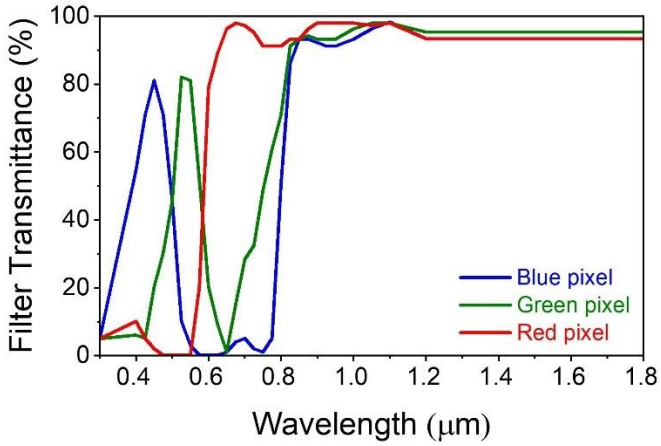


Fig. 8.12. Transmittance through the filters.

8.4.2.2 Enhanced Sensitivity in Thin Ge on Si CMOS image sensor

The calculated optical efficiency (OE) in 500 nm and 1 μm Ge layer are shown in Fig. 8.12 (a) and (b), respectively. The transmission profile of the flat pixels (no photon-trapping structure on the surface) for infrared is shown with a black line. The calculated OE, which represents the absorption of the light by the active layer of each pixel. The quantum efficiency (QE) on the other hand is the photo-current of the device normalized to the light intensity and is less than the OE due to recombination and other losses. Still, the higher OE translates to a higher QE, and optimizing the light-trapping quality would increase QE. The maximum optical efficiency for the blue, red, and green filters determined by the filter transmittance are OE_{Blue} = 75% at 440 nm, OE_{Green} = 80% at 550 nm, and OE_{Red} = 80% at 650 nm [Fig. 8.12(a-b)]. In contrast, the filters are shown to be transparent in the mid-infrared [Fig. 8.11]. The Ge optical absorption is relatively weak at 1500 nm, and the photon-trapping strategies are utilized to enhance the absorption, leading to a higher optical efficiency. To increase the OE, a cylindrical hole at the center of each pixel is incorporated [Fig. 8.11(c-f)]. The diameter of the hole per pixel is 800 nm. SiO_2 trenches introduced at the edges of each pixel with a width of 150 nm to reduce the crosstalk between the neighboring pixels. The depth of the holes and trenches is the same as the thickness of the Ge layer. Micro-hole arrays were shown to enhance the optical absorption of Si for the 800- 1000 nm wavelength range [11, 14, 15] and the Ge for 1400-1800 nm wavelength [20]. The optimal micro

hole size is comparable to the small sized pixels. The deep trench structure with the Si-SiO_2 interface is used as a barrier against electron diffusion and to prevent the crosstalk. The micro-structure redirects the normal incident light into lateral directions parallel to the surface plane and helps increase the absorption and reduce reflection [11, 20].

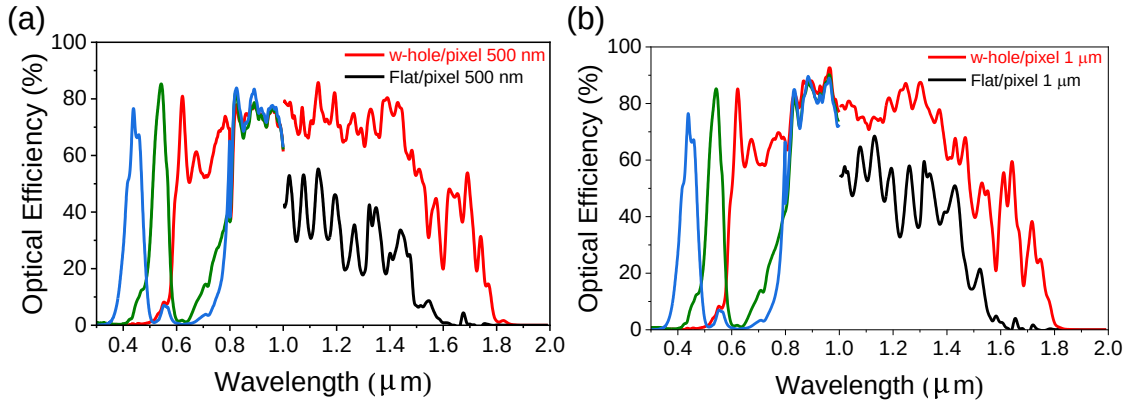


Fig. 8.13. Optical efficiency of the red, blue, and green pixels marked with the respective colors, and the optical efficiency for flat pixels marked with the black color. Optical efficiency trends with cylindrical holes sensors of (a) 500 nm, and (b) 1 μm Ge thicknesses for wavelength range between 300-1900 nm.

The influence of the Ge thickness on the optical efficiency with photon trapping holes is studied in this section. The Ge thickness has been reduced from 1000 nm to as low as 150 nm. As is expected, the optical efficiency is reduced with thinner thickness accordingly. However, the reduction is almost negligible up to 250 nm and start reducing for even thinner Ge. Although a flat/planar pixel of thickness 150 nm produces minimal optical efficiency in infrared, the single cylindrical hole per pixel increases the efficiency to about 40%, which is still useful for sensing in mid-infrared. The study [23]of an image sensor with Ge showed significant quantum efficiency at 400 nm Ge. This study shows that using a single hole per pixel is a way to significantly improve the quantum efficiency for an even thinner Ge layer for an extended range of wavelength—up to 1700 nm. The optical efficiency in the visible range is high due to the high absorption of Ge for the visible wavelengths. For ultra-thin Ge as 150 nm, the optical efficiency is reduced from 80% to 60%, which still consider highly efficient. A thin absorbing layer could be interesting from the fabrication point of view because it will not cause wafer bending or elongated threading

dislocations due to lattice mismatch with the Si substrate [24]. Also, it is interesting because a thinner absorbing layer can provide a faster performance due to the reduced transient time. The hole depth is ¾ of the Ge thickness filled with SiO_2. The OE in the visible range is shown in Fig. 8.14 for 350 nm, which is lower than 500 nm.

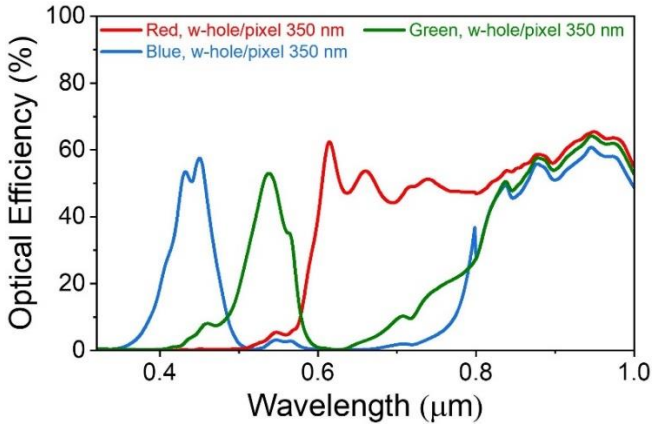


Fig. 8.14. optical efficiency of the red, blue, and green pixels in the visible spectrum (wavelengths range between 350-1000 nm) for 350 nm Ge thickness. Cylindrical hole per pixel is implemented in 350 nm Ge image sensor.

The infrared OE is demonstrated for 350 nm in Fig. 8.15 (a) and for 150 nm and in Fig. 8.15 (b) (red line) compared to flat pixels (black line) and a device with 500 nm Ge thickness (blue line). As one can see, the 350 nm with cylindrical holes pixels produces almost the same OE as that of 500 nm. However, the 150 nm pixels show a significantly reduced OE. The optical efficiency in infrared for all the Ge thicknesses is significantly higher than that for the flat pixels.

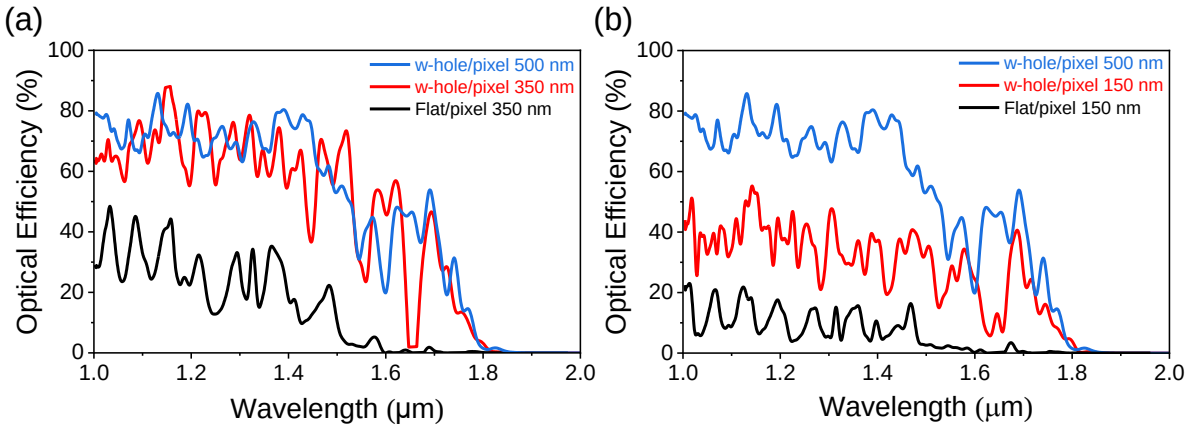


Fig. 8.15. Optical efficiency of cylindrical hole per pixel sensors for Ge thicknesses: (a) 350 nm, and 500 nm. (b) Ge thickness of 150 nm in infrared wavelength range, and are compared against a cylindrical hole Ge sensor of Ge thickness 500 nm. The hole depth is 3/4 of the Ge thickness.

8.4.2.3 Implementation of deep trench isolation (DTI) for crosstalk reduction between the designed pixels

An increase in the crosstalk between pixels could be an undesired side-effect of this increased OE. The crosstalk is desired to be reduced using deep trenches isolators (DTI) as aforementioned. The crosstalk index between each pair of colors, e.g., the red-green crosstalk, i.e., the response of the green pixel at the red wavelength, are discussed in section 8.2. This definition implies that a higher value of the index of crosstalk corresponds to higher contrast and lower crosstalk. The trenches could be optimized to reduce the crosstalk by varying depths and thicknesses. It is defined as the OE value for the maximum for the corresponding color to the OE value of the neighbor pixel at the same wavelength as can be found in table 8.3.

Pixel color	Crosstalk index Ge 500 nm	Crosstalk index Ge 350 nm	Crosstalk Index Ge 150 nm
Green-red	27	26	20
Red-green	16	15	9
Red-blue	82	82	50
Blue- red	85	82	50
Green-blue	31	29	20
Blue-green	5	4	3.5

Table 8.3. Crosstalk between pixels with different Ge thicknesses in the visible spectrum.

The crosstalk is negligible for 500 nm Ge whereas the crosstalk is slightly increasing with the decrease in the Ge thickness and the depth of the holes. However, even for 150 nm, we have a relatively small crosstalk index compared to what was previously reported in the literature [25]. In the design, the DTI technique was utilized to reduce the crosstalk, which is effective even for 150 nm Ge. The performance of the simulated Ge sensor is compared with the state-of-the-art

literature in table 8.4. This model, single hole per pixel in Ge sensor, present an increased OE in the 1.70 µm wavelength range.

Year Ref	Substrate	Active Region (µm)	Pixel pitch (µm)	QE[1]/OE[2] @ 1310 nm	QE[1]/OE[2] @ 1550 nm	QE[1]/OE[2] @ 1700 nm
2009 Ackland. B, et al.	Ge-on-Si	2-5.6	7 to 10	60[1]	10[1]	-
2011 Kaufmann. R, et al.	Ge-on-Si	1.5	120	37[1]	22[1]	-
2019 Köllner, et al.	Ge-on-Si	0.6	30	38[1]	16[1]	<1
2021 Oehme, et al.	Ge-on-Si	0.4	25	34[1]	4[1]	<1
2022 This work (Simulation)	**Ge-on-SOI**	**0.15**	**1.12**	**35[2]**	**30[2]**	**37[2]**
		0.35	**1.12**	**76[2]**	**42[2]**	**47[2]**
		0.5	**1.12**	**68[2]**	**40[2]**	**51[2]**

Table 8.4. Device bench-marking against state-of-the-art literature.

8.4.2.4 Capacitance reduction in CMOS image sensor through the incorporation of hole per pixel

To study the performance and compare the impact of incorporating the holes in the sensor, ATLAS Silvaco device simulation has been performed. The sensor structure with a 200 nm top p-Ge layer with doping 5×10^{18} cm^{-3} followed by a 300 nm p-Ge layer with 1×10^{15} cm^{-3} doping (intrinsic region) stacked over a 2.0 µm Si layer (doping 5×10^{18} cm^{-3}). The metal contacts are at the top and the bottom of the device as shown in Fig. 8.16 (a). Four different structures were simulated as follows: 1) without-hole device; 2) 200 nm hole depth; 3) 370 nm hole depth; and 4) 500 nm hole depth. The hole width is fixed at 800 nm. Shockley Read Hall, Auger, and field-dependent mobility models were used to incorporate mobility accurately. The Poisson and drift-diffusion model have been utilized for carrier transport. Due to the high doping, the Fermi probability distribution function was used instead of Boltzmann's approximation. To study the impact of the hole on the capacitance of the device, capacitance-voltage (C-V) simulation was performed on the sensors. The obtained C-V profile is shown in Fig. 8.16 (b).

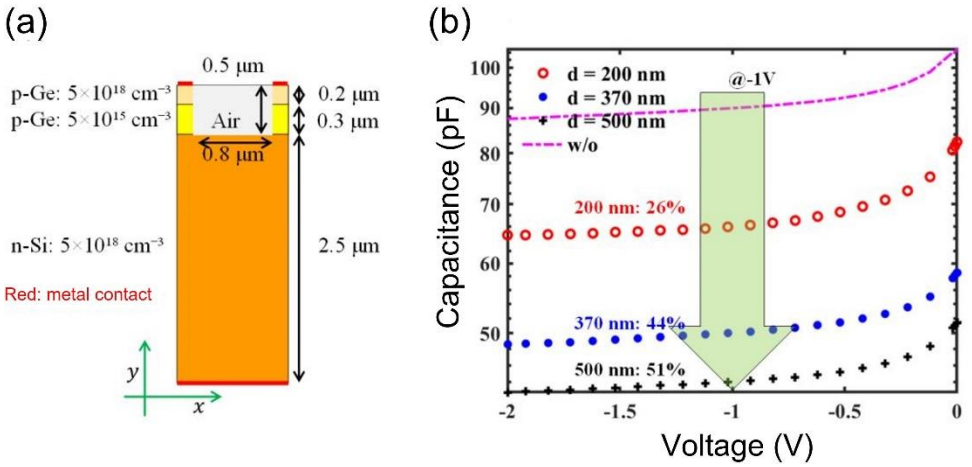


Fig. 8.16. (a) Schematic of the Ge image sensor simulated on ATLAS Silvaco; (b) Capacitance versus voltage profile extracted from simulation presenting capacitance reduction in Ge CMOS image sensor due to the implementation of PT hole per Ge pixel.

The capacitance values show a significant reduction with the introduction of the hole as opposed to the flat sensor. A gradual capacitance decrease was observed from 26% to 50% with the hole depth increasing from 200 nm to 500 nm. This reduction can be attributed to the reduced effective volume of the holey sensor. Such Ge sensors, with an enhanced power absorption at NIR wavelength, a reduced device capacitance, ultra-fast, a high carrier mobility in Ge [26], and a CMOS compatible fabrication process, have potential to revolutionize the short-wave infrared imaging.

References

[1] S. Yokogawa *et al.*, "IR sensitivity enhancement of CMOS Image Sensor with diffractive light trapping pixels," *Scientific reports,* vol. 7, no. 1, pp. 1-9, 2017.

[2] S. S. S. Group., " Imaging and Sensing Technology," ed, Nov. 22, 2020.

[3] B. J. Park *et al.*, "Deep trench isolation for crosstalk suppression in active pixel sensors with 1.7 μm pixel pitch," *Japanese journal of applied physics,* vol. 46, no. 4S, p. 2454, 2007.

[4] A. Tournier *et al.*, "Pixel-to-pixel isolation by deep trench technology: Application to CMOS image sensor," in *Proc. Int. Image Sensor Workshop*, 2011, pp. 12-15.

[5] E. P. Devine *et al.*, "Single microhole per pixel in CMOS image sensors with enhanced optical sensitivity in near-infrared," *IEEE Sensors Journal,* vol. 21, no. 9, pp. 10556-10562, 2021.

[6] L. Inc, "The Finite-Difference Time-Domain (FDTD): 3D Electromagnetic Simulator," ed.

[7] M. I. Hossain *et al.*, "Perovskite color detectors: Approaching the efficiency limit," *ACS applied materials & interfaces,* vol. 12, no. 42, pp. 47831-47839, 2020.

[8] B. E. Bayer, "Color imaging array," *United States Patent 3,971,065,* 1976.

[9] S. Yokogawa, S. P. Burgos, and H. A. Atwater, "Plasmonic color filters for CMOS image sensor applications," *Nano letters,* vol. 12, no. 8, pp. 4349-4354, 2012.

[10] C. Park and M. G. Kang, "Color restoration of RGBN multispectral filter array sensor images based on spectral decomposition," *Sensors,* vol. 16, no. 5, p. 719, 2016.
[11] Y. Gao *et al.*, "High speed surface illuminated Si photodiode using microstructured holes for absorption enhancements at 900–1000 nm wavelength," *ACS Photonics,* vol. 4, no. 8, pp. 2053-2060, 2017.
[12] S. Ghandiparsi *et al.*, "High-speed high-efficiency photon-trapping broadband silicon PIN photodiodes for short-reach optical interconnects in data centers," *Journal of Lightwave Technology,* vol. 37, no. 23, pp. 5748-5755, 2019.
[13] E. Yablonovitch and G. D. Cody, "Intensity enhancement in textured optical sheets for solar cells," *IEEE Transactions on electron devices,* vol. 29, no. 2, pp. 300-305, 1982.
[14] H. Cansizoglu *et al.*, "Dramatically enhanced efficiency in ultra-fast silicon MSM photodiodes via light trapping structures," *IEEE Photonics Technology Letters,* vol. 31, no. 20, pp. 1619-1622, 2019.
[15] C. Bartolo-Perez *et al.*, "Maximizing Absorption in Photon-Trapping Ultrafast Silicon Photodetectors," *Advanced Photonics Research,* vol. 2, no. 6, p. 2000190, 2021.
[16] A. S. Mayet *et al.*, "Surface passivation of silicon photonic devices with high surface-to-volume-ratio nanostructures," *JOSA B,* vol. 35, no. 5, pp. 1059-1065, 2018.
[17] A. S. Mayet *et al.*, "Inhibiting device degradation induced by surface damages during top-down fabrication of semiconductor devices with micro/nano-scale pillars and holes," in *Low-Dimensional Materials and Devices 2016*, 2016, vol. 9924: SPIE, pp. 36-42.
[18] I. Oshiyama *et al.*, "Near-infrared sensitivity enhancement of a back-illuminated complementary metal oxide semiconductor image sensor with a pyramid surface for diffraction structure," in *2017 IEEE International Electron Devices Meeting (IEDM)*, 2017: IEEE, pp. 16.4. 1-16.4. 4.
[19] C.-F. Han, J.-M. Chiou, and J.-F. Lin, "Deep trench isolation and inverted pyramid array structures used to enhance optical efficiency of photodiode in CMOS image sensor via simulations," *Sensors,* vol. 20, no. 11, p. 3062, 2020.
[20] S. Ghandiparsi *et al.*, "Up to 1700nm broadband high-efficiency surface-illuminated Ge/Si photodiode with microhole array," in *Integrated Photonics Research, Silicon and Nanophotonics*, 2019: Optica Publishing Group, p. IT3A. 3.
[21] A. Taflove, S. C. Hagness, and M. Piket-May, "Computational electromagnetics: the finite-difference time-domain method," *The Electrical Engineering Handbook,* vol. 3, pp. 629-670, 2005.
[22] J. Berzinš, S. Fasold, T. Pertsch, S. M. Bäumer, and F. Setzpfandt, "Submicrometer nanostructure-based RGB filters for CMOS image sensors," *ACS Photonics,* vol. 6, no. 4, pp. 1018-1025, 2019.
[23] M. Oehme *et al.*, "Backside Illuminated “Ge-on-Si” NIR Camera," *IEEE Sensors Journal,* vol. 21, no. 17, pp. 18696-18705, 2021.
[24] A. Abedin, "Germanium layer transfer and device fabrication for monolithic 3D integration," KTH Royal Institute of Technology, 2021.
[25] Y. Horie *et al.*, "Visible wavelength color filters using dielectric subwavelength gratings for backside-illuminated CMOS image sensor technologies," *Nano Letters,* vol. 17, no. 5, pp. 3159-3164, 2017.
[26] F. Schäffler, "High-mobility Si and Ge structures," *Semiconductor Science and Technology,* vol. 12, no. 12, p. 1515, 1997.

Chapter 9 Short-reach up to U/XL broadband optical communication enabled by photon trapping Ge on Si CMOS compatible high efficiency and ultra-fast photodetector

9.1 Germanium on Silicon (Ge/Si) PIN photodetectors

Datacenters are projected to scale up to meet the high demand of data connectivity. Intra- and inter-datacenter communications require optical links for short reach (up to 500m), long-reach/long-haul (~10 km), and extended reach communications (up to 40 km), which need optical transceivers operating at wavelengths of 1310 nm. While, passive optical networks (PONs), which provide low-cost solutions for the demand in high data rate access to users, require optical transceivers operating at a wavelength of 1550 nm [1]. The data rate can be enhanced in such systems by employing dense wavelength division multiplexing (DWDM). However, the demand for data traffic is growing beyond the current capacity of single-mode fiber operating at the C band (1530–1560 nm) and the L band (1560–1620 nm) for DWDM in long-haul communication links. One of the promising solutions to overcome the capacity crunch is to extend existing single-mode fiber bandwidth beyond the L band to the U/XL band (1620-1700 nm). Recent developments in fiber amplifers [2, 3] that can operate in the new band of 1620–1700 nm pave the way to realize data transmission to the U/XL band. In addition, holllow-core photonic-bandgap fibers [4, 5] has the ability to extend fiber bandwidth up to 2000 nm through utilizing these new optical amplifiers. In addition, emerging applications such as quantum communications [6], eye-safe lidar systems [7], and photonic biosensors [8], require detectors operated at the near-infrared, particularly at 1310 or 1550 nm, taking advantage of the low-loss windows of optical fibers and low scattering of light at those wavelengths in the atmosphere and tissue, respectively. Commercially existing optical receivers often contain photodiodes (PDs) based on III–V materials such as InGaAs/InP [9, 10]. Nevertheless, these materials are not compatible with CMOS technology and would incur additional costs for wafer bonding, packaging, yield, thermal management, etc. [11, 12]. Alternatively, monolithic integration of PDs with all electronics on a single chip, fully hermetic and

without ceramic multichip carriers for the receiver end, can reduce the manufacturing and assembling cost dramatically. Ge/Si devices provide a possible solution for these kinds of high-speed applications, as BiCMOS SiGe technology has already been proved in CMOS foundries [13]. Additionally, low field transport is much faster in Ge than in Si, and high field transport is similar between both materials. Hence, using Ge for the i-layer in a pin PD is highly advantageous in improving speed [14]. Although bulk Ge has a very broad absorption spectrum, the direct bandgap of Ge is only 0.8 eV, which results in weak absorption at and beyond 1500 nm. A conventional surface-illuminated pin PD is limited by the EQE and bandwidth product as there is often a trade-off: smaller absorption thickness leads to a fast but low efficiency device, while larger absorption thickness results in an efficient but slow device. The optical efficiency of Ge can be greatly enhanced beyond 1500 nm by integrating photon trapping nanoholes without sacrificing the speed performance. This chapter discusses the demonstration of surface-illuminated Ge-on-Si pin PD with high EQE (>80% at 850 nm, >87% at 1310 nm and 77% at 1550 nm) for 10 Gb/s operation for short reach and long-haul optical data communication links. The EQEs of photon trapping (PT) holes PDs are enhanced to >120% at short reach communication 850 nm compared to the control PDs (without holes). In addition, the EQEs of PT PDs enhanced >400% up to 1700 nm compared to the control PDs, which is promising to realize optical receivers for data transmission beyond the L band such as U/XL optical band window.

9.2 Device design

The designed Ge on Si pin photodiodes were epitaxially grown on a Si substrate as can be seen in Fig 9.1. A high phosphorus-doped (10^{19} cm^{-3}) Si n-type contact layer was initially grown to form the bottom n-mesa. Subsequently, 2 µm thin intrinsic Ge layer is grown. Finally, a high boron-doped (10^{20} cm^{-3}) Ge p-type layer was grown to form the top contact layer (both contact layers are designed to be 0.2 µm thick). The contact layers are highly doped to reduce the minority carriers' lifetime outside the space charge region and minimize carriers' diffusion. The intrinsic Ge

layer is kept relatively thin to be able to minimize the transit time of photogenerated electrons and holes, thus making the PD operate at a high speed. As can be seen in Fig 9.1 (a), control PD without holes was fabricated as a reference PD. Photon trapping PD's complete design can be seen in Fig 9.1 (b).

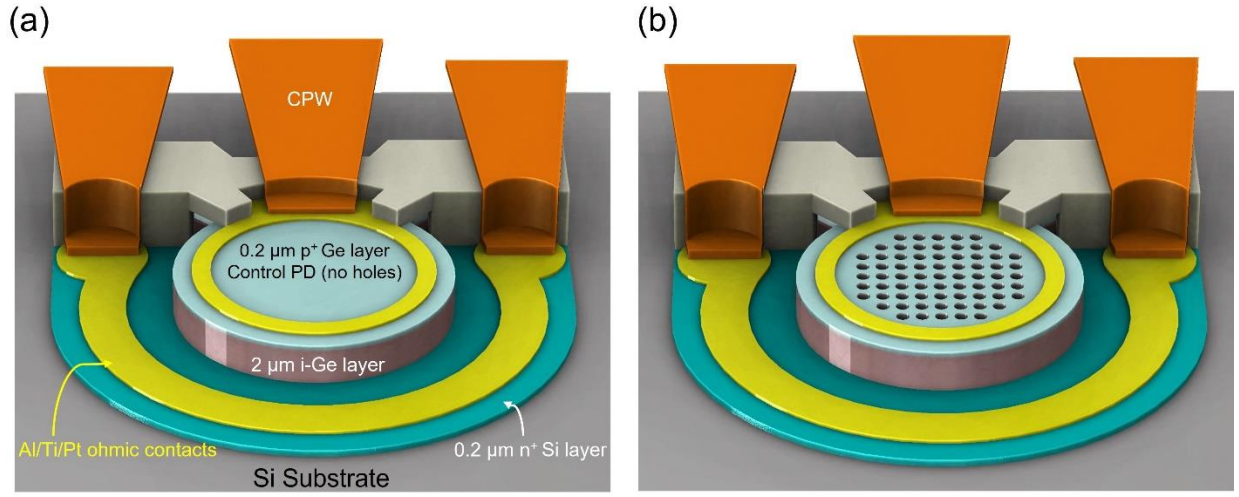


Fig. 9.1. Schematics of Ge on Si PD active layers with the completed structure of the fabricated devices. (a) Control PD. (b) Photon trapping PD.

9.3 Optical simulations

Light propagation in a structure with periodic hole arrays can be different from that in a slab (control) without holes. Constructive and destructive interference of light in the incident direction is expected as light travels through a thin slab. However, a structure with periodic hole arrays interacts with light in a way that a lateral component of light propagation occurs in addition to the vertical component of propagation in the incidence direction. Figure 9.2 (a) present the simulated electric field in the cross section of the control Ge-on-Si (without hole) and (b) with a tapered hole array where it can be seen that light travels not only vertically but also propagate in the lateral direction in the Ge layer. Such light guiding in the thin Ge layer enhances the optical path and ultimately improves absorption without increasing thickness. Figure 9.2 (a) shows the field propagation in Ge without holes (steady state; time is enough for the wave front to reach the bottom and a part reflect from the interface of Ge and Si) while unabsorbed light leaks out

(transmit). The light in the slab without holes propagates only in the vertical direction, and the field intensity is also smaller compared to that in the one with hole arrays due to higher reflection from the surface of the slab.

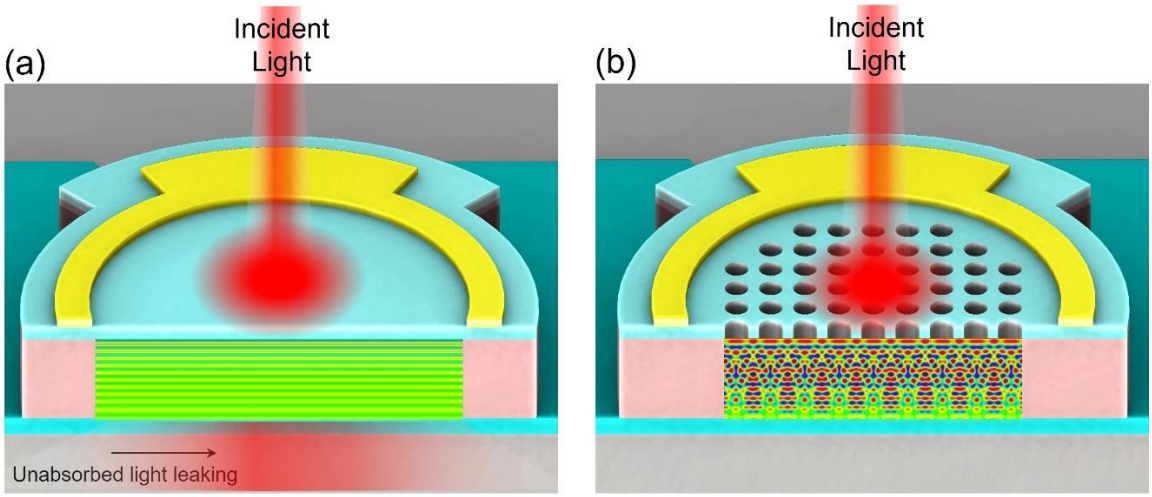


Fig. 9.2. Schematic diagram and cross sections of the electric field intensity at 1550 nm. (a) Light propagating in the direction of incidence throughout the control PD with less intensity. (b) Light guiding near-perpendicular to the incoming light in photon-trapping PD with high intensity.

Ge-on-Si PDs with hexagonally packed tapered holes modeled numerically by using the FDTD method for a wavelength range of 1200–1800 nm. In addition, different thicknesses of Ge i-layer were simulated to study the optical absorption in control PD and PT PD. The optimized PT structures such as holes diameter, periods, depth, and sidewall's profile can be designed according to the targeted wavelength. Figure 9.3 present enhanced optical absorption in PT PD for a broadband spectrum.

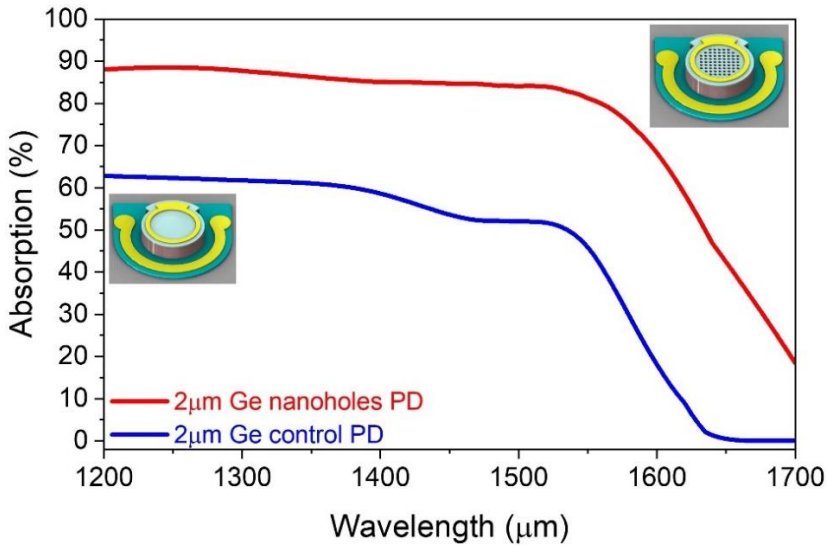


Fig. 9.3. Calculated absorption of Ge on Si PD, optical absorption comparison in Ge control PD vs. Ge PT PD for 2 μm i-layer.

9.4 Device Fabrication

The photon-trapping holes can guide light nearly perpendicular to the surface and allow light to propagate laterally and eventually get absorbed through the device layer as can be seen in Fig. 9.4 (a). Since the lateral dimension of the device is much larger than the thickness of the absorbing layer, PDs with micro/nanoholes are efficient and fast at the same time. The Ge-on-Si wafer doping profile after growth is shown in Fig. 9.4 (b).

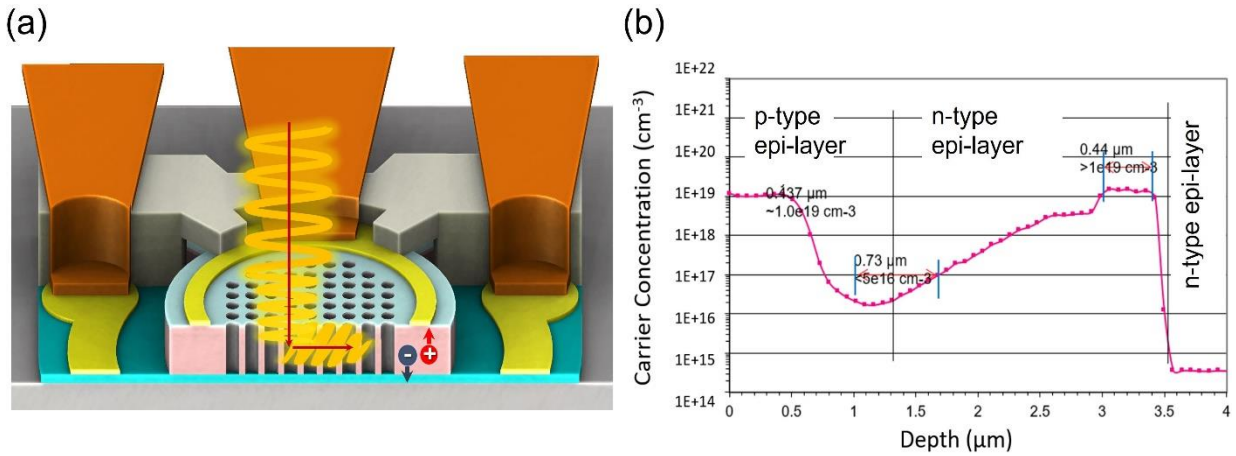


Fig. 9.4. (a) Schematic of a surface-illuminated PD with integrated holes with vertical carrier collection and lateral light absorption. The dark circle with the "-" sign and the red circle with the "+" sign represent photon-generated electron and hole, respectively. (b) Carriers' concentration profile of the fabricated Ge on Si PIN PD.

The fabrication processes for the Ge PDs are CMOS compatible and were conducted in a class 100 cleanroom. The as-grown Ge-on-Si wafer was first cleaned in PRS3000 solution to remove any organic contaminant.

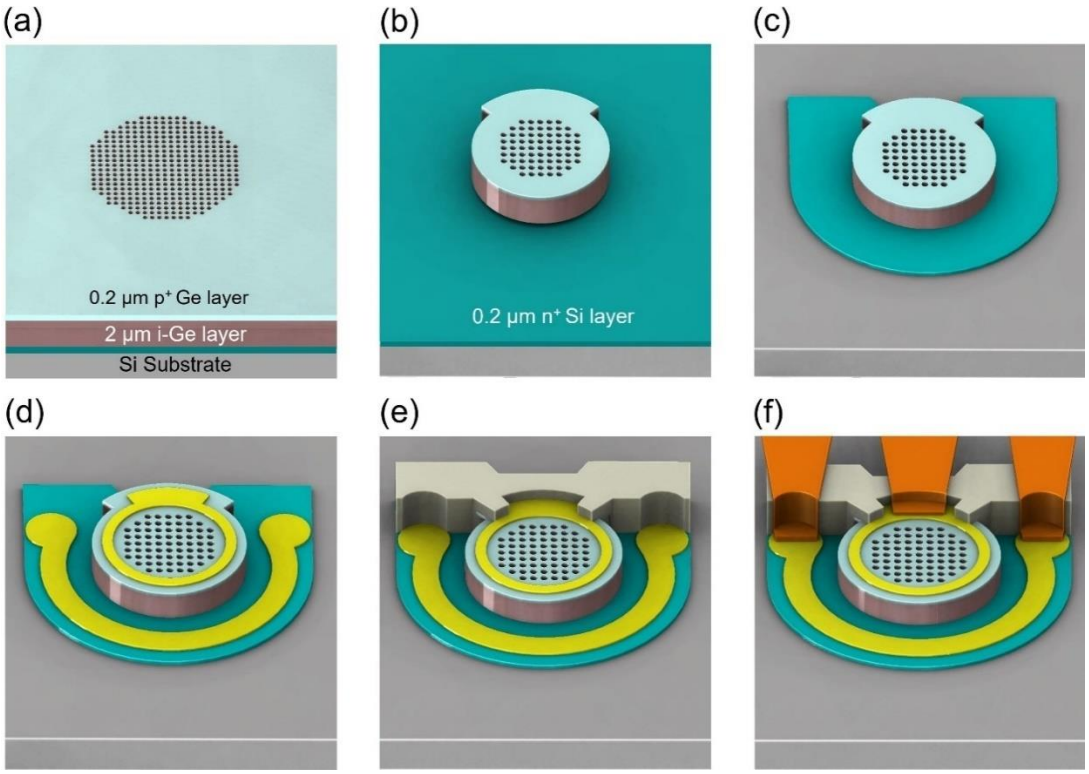


Fig. 9.5. Schematic diagram of fabricating Ge photon trapping PDs. (a) Starting wafer (grey: Si wafer substrate; turquoise: n^+-type layer, composed of 0.2 µm Si layer; maroon: 2 µm i-Ge layer; blue: 0.2 µm p^+-Ge layer), DUV photolithography and holes etch to create tapered or cylindrical holes with diameters ranging from 630 to 1500 nm in a hexagonal lattice. (b) p-mesa etch to n-Si layer, (c) n-mesa etch to the substrate layer, followed by 10 nm (ALD) SiO2 surface passivation. (d) Ohmic metal deposition (100 nm Al, 10 nm Ti, 30 nm Pt). (e) 3 µm of polyimide layer used for planarization. (f) Coplanar waveguides (CPWs) metal deposition (brown color).

9.4.1 Nanoholes formation

After wafer cleaning, 0.9 µm i-line resist was uniformly spin-coated onto the Ge-on-Si wafer. GCA 8500 i-line stepper was used as the exposure tool to pattern the i-line resist. Similar to the reactive ion etch (RIE) technique performed on silicon described in chapter 4, cylindrical and funnel-shaped micro-/nanoholes were created on the Ge surface, as can be seen in Fig. 9.6.

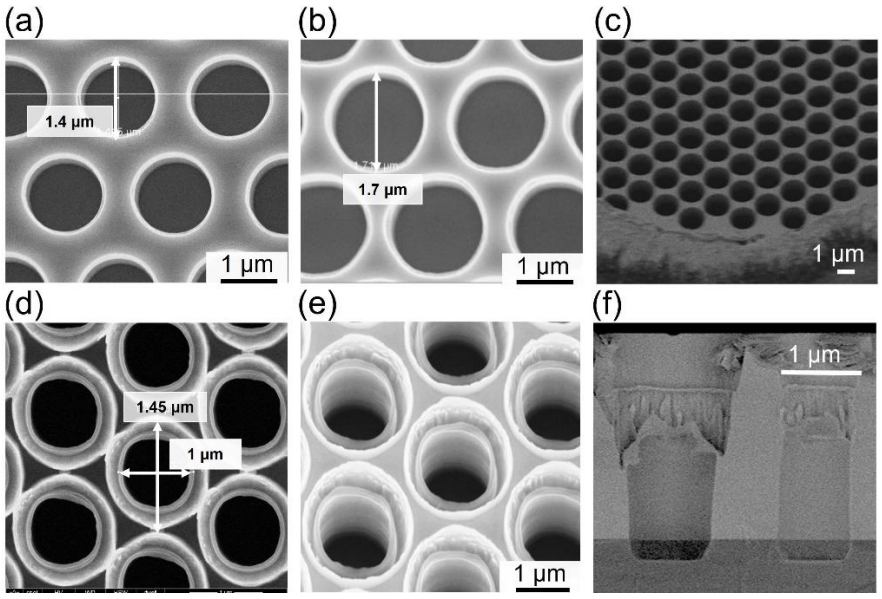


Fig. 9.6. Scanning electron microscope (SEM) images. (a) Cylindrical holes with 1.4 µm diameter. (b,c) Cylindrical holes with 1.7 µm diameter. (d,e) Funnel-profile holes. (f) Cross-sectional view of funnel-profile hole.

To form funnel-profile, the resist between the dense holes can form positive angles due to the lateral etch of the resist in RIE. After a critical thickness of the resist (~200 nm) is reached, the nanoholes in Ge start to widen and form a tapered angle. The resist thickness must be calibrated by taking into consideration of the etch ratio of the Ge and resist, so that the desired depth of the holes can be reached. The funnel-shaped nanoholes with some degree of tapering angle can reduce the reflection, and thus improve the quantum efficiency of the PDs as previously discussed in chapter 4.

9.4.2 Device mesa formation

After the holes etch, the PD mesa structures were etched to the respective layers via RIE: p-mesa was etched through the p^+-Ge and i-Ge layers and stopped at the n^+-Si layer, and n-mesa was etched through the n^+-Si layer and stopped at the Si substrate.

9.4.3 Device surface passivation

To minimize the dark current of the device, a 10 nm of SiO_2 was deposited using plasma enhanced atomic layer deposition (ALD) at 270°C as a device passivation layer [15].

9.4.4 Ohmic contacts deposition

Metal layer stacks composed of 100 nm Al, 10 nm Ti, and 30 nm Pt were deposited in sequence on p-mesa and n-mesa using sputtering, followed by a lift-off process. Ohmic contacts between the metal and semiconductors were formed by rapid thermal processing (RTP) at 465°C for 30 s in a forming gas (H_2/N_2) environment.

9.4.5 Planarization process

A layer of polyimide (3 μm) was used for planarization as well as reducing the parasitic capacitance of coplanar waveguides (CPWs) as can be seen in Fig. 9.4 (e).

9.4.6 CPW metal deposition

CPWs composed of 10 nm Ti and 300 nm Al were sputtered followed by a lift-off process.

9.5 Experimental results and discussion

9.5.1 External Quantum Efficiency (EQE)(NIR-MIR) at 850, 1310, 1550, and 1700 nm

External quantum efficiency of the fabricated Ge PDs integrated with funnel-shaped PT holes (diameter ~1200 nm and period~1800 nm) with hexagonal unit cell was characterized for a broad range of spectrum (800 nm-1800 nm). Control Ge PD (no holes) was also characterized for the comparison purposes. High EQEs of the Ge PDs is highly desired in both data communication wavelengths (1310 and 1550 nm). Therefore, the design parameters were slightly different than Si since the targeted wavelength in this study was 1310 nm, 1550 nm and 1700 nm. Hence, considering the shorter range of MIR spectrum, PT holes diameter and periods were optimized to yield the best light coupling in these photonic crystal's structures. As can be seen in Fig. 9.7. the EQE of Ge PT PD reaches around 81% at 850 nm (NIR) short-reach communication window, whereas Ge control PD EQE presents only 63%. For the MIR region which these devices were optimized, around 85% EQE is achieved for Ge PT PD at 1310 nm wavelength, whereas control Ge PD provides around 62% EQE. Similar trend is observed at a wavelength of 1550 nm, where

the EQE is improved from 46% for control Ge PD to 74% for PT Ge PD. The acquired results potentially offering data transmission possible beyond the L band in the new band of 1620–1700 U/XL window as well. The EQE of the PT Ge PD showed an enhanced values around 5% with only 2 μm i-layer, whereas control Ge PD has no response at such longer wavelengths where intrinsic Ge bandgap limits its ability to absorb longer wavelength's photons. The FDTD simulation results found that the absorption simulated by assuming a 2 μm thick effective i-layer fits closely with the experimental results for the control Ge PD. Whereas, PT Ge PD FDTD results shows a slightly high value specially at 1570-1720 nm). Such discrepancy can be attributed to fabrication-related deviation and recombination loss of photo-generated carriers. Additionally, light with longer wavelengths can penetrate deep into the material and can be absorbed beyond the i-layer, where the electric field is weak for efficient carrier collection.

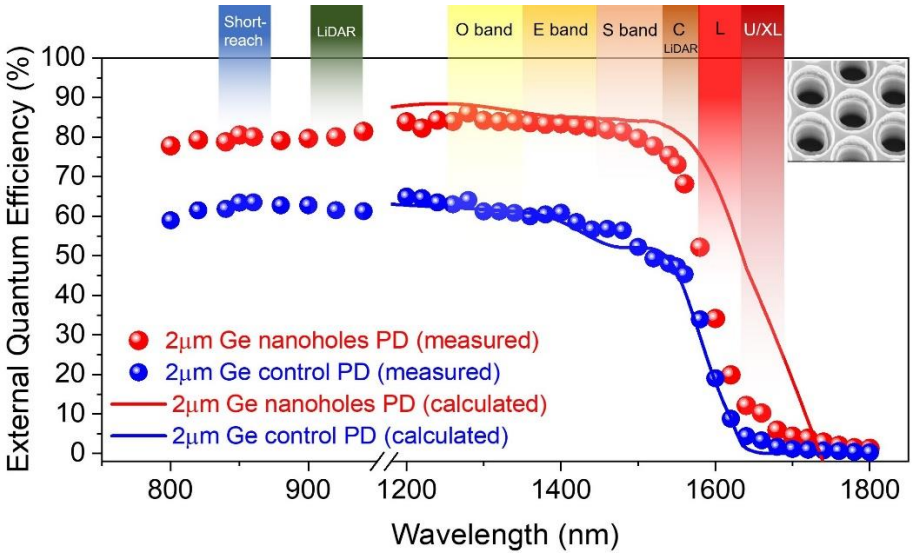


Fig. 9.7. Measured EQE vs. calculated absorption of Ge-on-Si PDs with photon-trapping holes (diameter/period: 1150/1750 nm) and control (planar) Ge PD, for s wavelength range of 800–1800 nm. Simulation results are in decent agreement for control Ge PD, whereas PDs with holes are expected to show higher EQE at the longer wavelengths beyond 1580 nm. Such discrepancy can be attributed to the deviation in fabricated structures from design and recombination loss of photo-generated carriers. Optical communication bands (windows) are shown in the top of the figure.

Responsivity of photon-trapping Ge PDs and control Ge PD is shown in Fig. 9.8. The measured responsivity presents 0.91 A/W responsivity achieved at 1550 nm in photon-trapping Ge PD while 0.59 A/W responsivity is shown in control Ge PD.

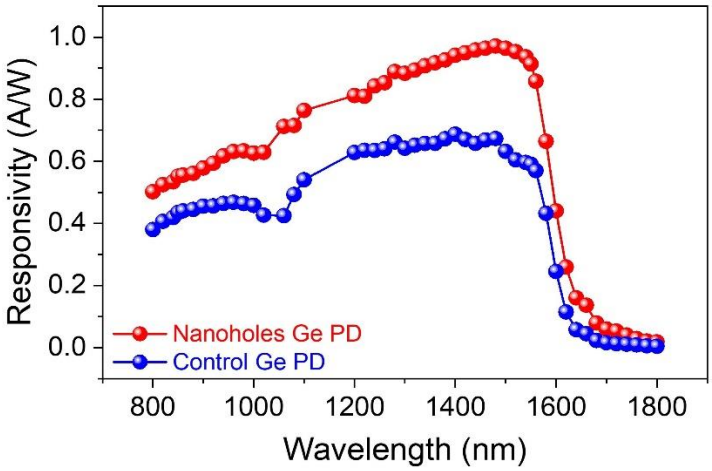


Fig. 9.8. Responsivity of Ge-on-Si PDs for PT Ge PD vs. control Ge PD for the wavelength range of 800–1800 nm. More than 0.91 A/W responsivity is achieved at 1550 nm with photon-trapping designs.

9.5.2 EQE enhancement in photon-trapping Ge PD

The enhancement in EQE is present over the entire broadband of wavelengths (800 nm-1800 nm) in Fig. 9.9. The enhancement becomes more considerable at wavelengths above 1600 nm, where the EQE of photon-trapping Ge PD has 34% efficiency, whereas the control Ge PD has only 19% EQE. A >400% enhancement in EQE was observed in photon-trapping Ge PD compared to the control Ge PD up to 1700 nm wavelength, potentially offering data transmission possible beyond the L band up to U/XL band.

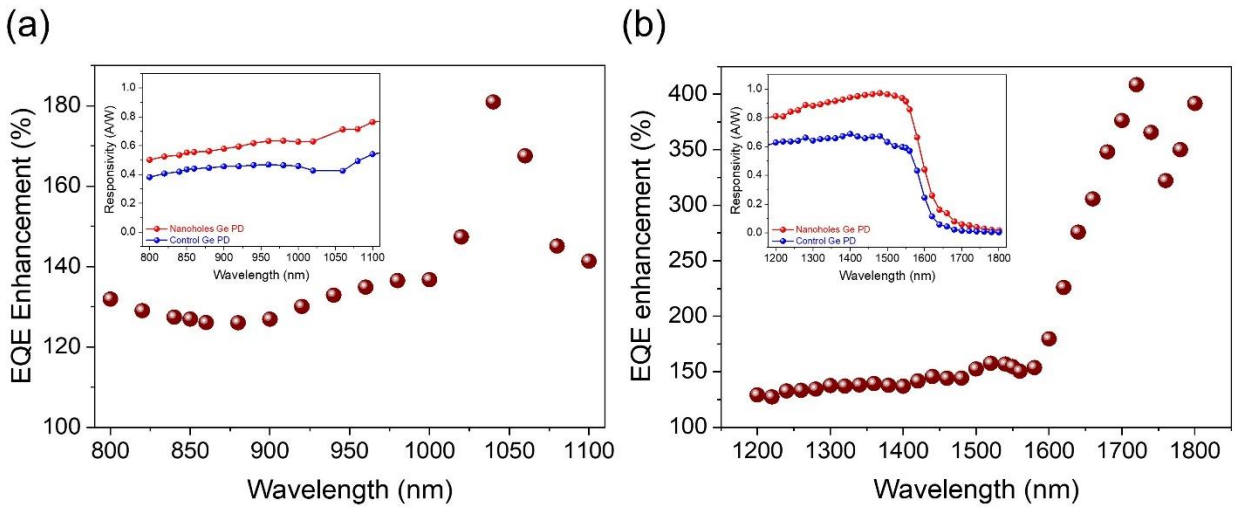


Fig. 9.9. EQE enhancement. (a) EQE enhancement for wavelengths 800-1100 nm. (b) EQE enhancement for wavelengths 1200-1800 nm. Photon-trapping Ge PD shows >350% increase in EQE with holes for wavelengths beyond 1700 nm.

9.5.3 Optimizing the optical absorption in photon trapping Si PD for a long-haul optical communication wavelength (λ=1550 nm)

For a more in-depth analysis of how the design of photon trapping structures affects the EQE on Ge PDs, an input light of 1550 nm wavelength (long-haul optical communication window) is injected, in photodiodes with all the design variations. A cylindrical and funnel profile photon-trapping structures were fabricated on Ge PD with a variety of different hole diameters and periods. As depicted in Fig 9.10, in all the designs, keeping the hole diameter (d) fixed, and varying the period (p), the EQE changes accordingly. It should be noted that the PDs with larger holes seem to have better EQEs at the wavelength of 1550 nm, which is different from our previous work on Si PDs at 800–980 nm wavelengths, where smaller holes outperform [16]. As for Ge PDs, the target wavelength is longer, and the diameter can period of the holes should also be large enough to couple lateral modes into the device structure. The broad EQE characterization was carried out on funnel holes with a diameter/ period of 1150/1750 nm in a hexagonal lattice and showed an enhanced 73% EQE at 1550 nm. Figure 9.10 shows cylindrical and funnel hole profiles EQEs. The highest EQE ~80% was acquired through the cylindrical hexagonal hole with a diameter and period of 1000/1500 nm. Subsequent high EQE for the funnel profile hole is around 77% for 800/1050 design structure. However, according to our analysis and

characterizations, the highest EQEs are acquired through funnel profile holes. By closer looking at the results, we can find out that the average EQEs for cylindrical holes profile is around 60%. Whereas the average EQEs for funnel holes profile is around 70%. FDTD simulations confirm that the modes in the top view of holes are much stronger for the funnel-profile holes, and the absorption versus wavelength dependence is more uniform than for cylindrical holes. Funnel-profile holes also experience smaller reflections as discussed in chapter 4 for Si PD. When one of the dimensions of the nanostructure diameter of the holes d and/or spacing between adjacent holes (p–d)—is less than the wavelength λ (p is the period), the effective refractive index gradually changes from the surface through the Ge, in contrast to the cylindrical holes, where there is an abrupt change. Thus, the funnel-shaped holes create an effect similar to a graded-refractive-index antireflection (AR) coating, with smaller refraction [17].

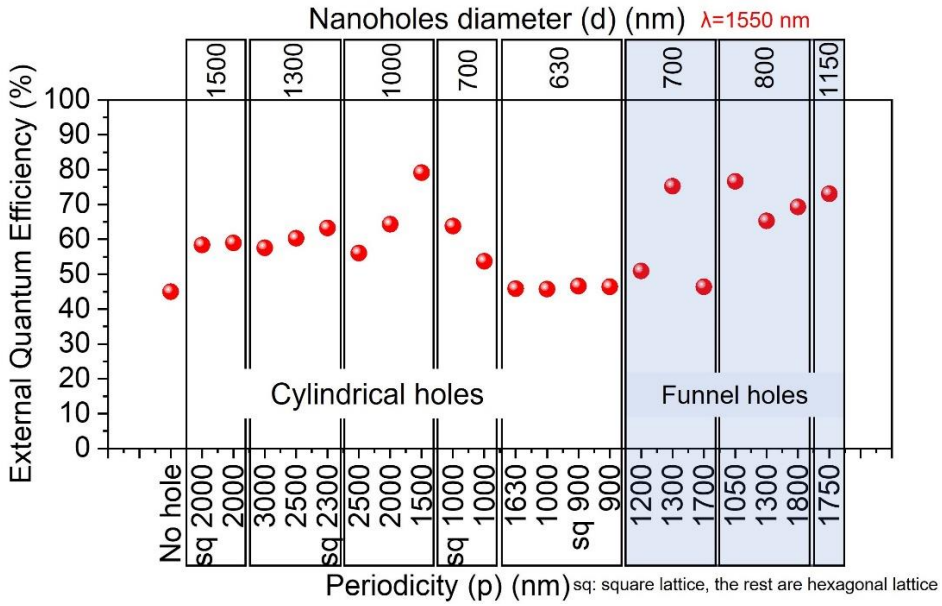


Fig. 9.10. EQE of Ge-on-Si PDs with different photon-trapping holes designs. The highest EQE ~ 80% was achieved with cylindrical holes (d=1000/p=1500). While highest averaged EQEs was achieved through funnel holes designs Ge PDs. PDs with slightly larger holes show a better EQEs at the wavelength of 1550 nm, which is different from our Si PDs at visible wavelengths, where smaller holes perform better as for EQE.

Figure 9.11 presents the EQEs of different funnel profile hole designs Ge PD compared to control Ge PD at optical communication windows of 1310 nm and 1550 nm. Different photon-trapping

funnel designs are showing different optical responses, regardless of achieving higher EQE than control Ge PD.

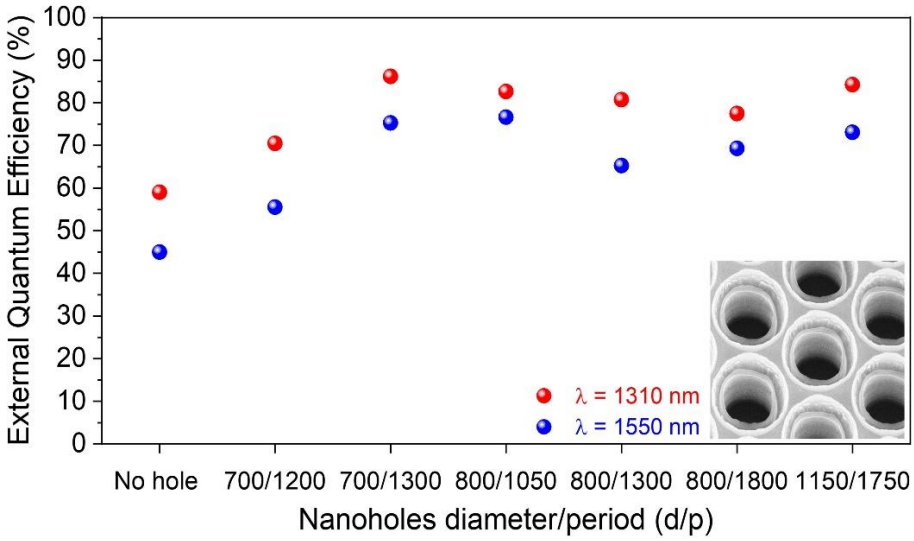


Fig. 9.11. EQE for funnel-hole designs in Ge PDs at wavelengths 1310 nm and 1550 nm. Photon-trapping designs on Ge PDs show different responses for different geometries which can be optimized and enhanced for specific application accordingly.

9.5.4 Dark current characteristics

The fabrication of Ge PT PDs is created by dry etching (RIE) with the physical bombardment of high-energetic plasma ions. Therefore, beside Ge is intrinsically a leaky material, crystalline defects, and dangling bonds can be formed at the Ge surface and create surface states that can contribute to the increased dark current level. Consequently, surface passivation with 10 nm SiO_2 was uniformly deposited on the wafer via ALD after the hole and mesa etches, reducing the leakage current in the PT devices. More passivation methods need to be investigated to effectively reduce the leakage current further. The dark current and photocurrent characteristics can be seen in Fig. 9.12.

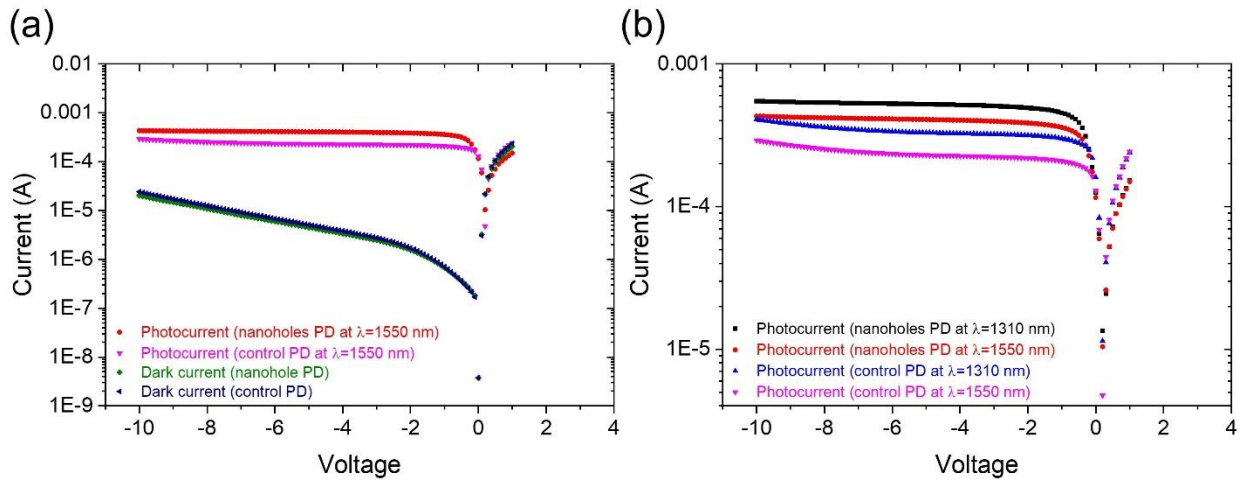


Fig. 9.12. DC characterization for Ge PDs. (a) Dark current and photocurrent for control Ge PD vs. photon-trapping Ge PD at 1550 nm wavelength. (b) Photocurrent responses for control Ge PD vs. photon-trapping Ge PD at 1310 nm, and 1550 nm incident wavelength.

9.5.5 RF and high-speed characterization

High -speed measurement is conducted by surface illumination of a 1310 nm pulsed laser (pulse width: ~15ps) via a single-mode fiber -probe and results were recorded using 20GHz sampling scope. To maximize the depletion in the intrinsic region the device is biased at high voltages - up to 17V. Figure 9.13. shows the impulse response full-width at half-maximum (FWHM) of the photon-trapping Ge PD and control Ge PD were measured to be 69 ps (blue) and 76 ps (black), respectively. The FWHM and tail characteristics of the impulse responses of the photon-trapping Ge PD correspond to a 10Gb/s transmission rate as can be seen in Fig 9.13 (b) insets. This is the fastest reported surface-illuminated Ge/Si PIN PD with broadband efficiency up to 1700 nm [18, 19].

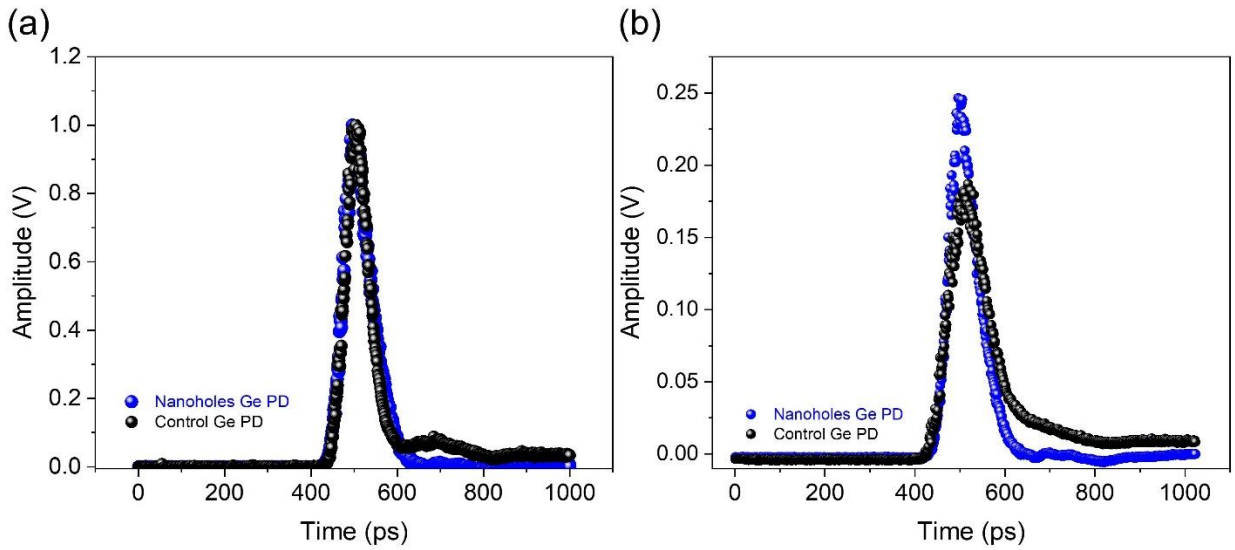


Fig. 9.13. (a) Measured impulse response (FWHM: 69 ps (photon-trapping Ge PD), FWHM: 77 ps (control Ge PD)) at 1310 nm. (b) Measured impulse response shows FWHM is smaller for photon-trapping PD, control PD shows a longer tail.

Figure 9.14. show the simulated eye diagrams at the filter output for a 10 Gb/s data transmission rate, indicating possible operation at such a rate. Compared to the eye diagrams generated with the measured impulse response of Ge PDs without hole arrays, there is an apparent improvement in transmission speed by Ge PDs with hole arrays, securing an operation of 10 Gb/s.

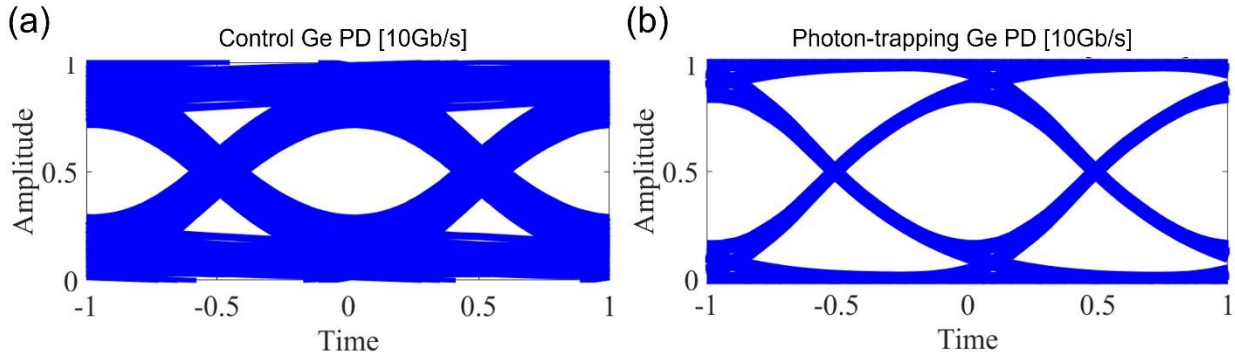


Fig. 9.14. Simulated eye diagrams at the filter output for a 10 Gb/s data transmission rate. (a) control Ge PD. (b) Photon-trapping Ge PD.

The bit error rate measurement is conducted using an Anritsu pattern generator that can generate up to 12.5Gb/s rectangular random pulse pattern. The pattern generator is used to derive a Finisar commercial transceiver (VCSEL laser) to generate an optical pulse pattern that illuminated the fabricated Ge-on-Si devices. The output signal is collected by a GSG probe and using a high

bandwidth waveguide is delivered to a Tektronix Digital Serial Analyzer with 25Gb/s bandwidth. A pattern generator measurement has been done and as the eye diagrams show, this photon trapping Ge-on-Si overcomes the bulky devices and can operate at such a high rate as can be seen in Fig. 9.15. and Fig. 9.16. The input wavelength was set to 1310 nm. The measured eye diagrams at 10 Gb/s bit rate at 10V for the control Ge PD and photon-trapping Ge PD as can be depicted in Fig. 9.15.

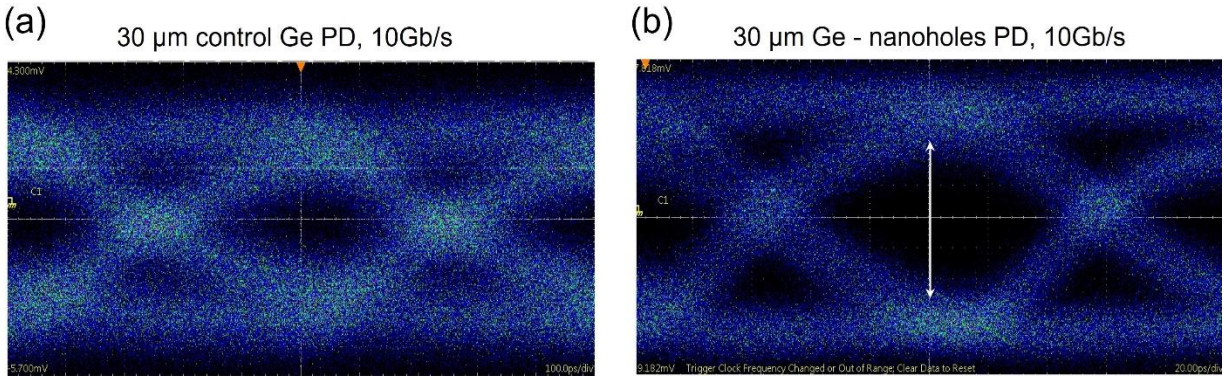


Fig. 9.15. Measured eye-diagram of a 30 µm Ge PDs at 10Gb/s, (a) control Ge PD (10V), (b) photon-trapping Ge PD (10V).

At higher bit rates the performance of control Ge PD drops rapidly while photon-trapping Ge PD are still operational as can be seen in Fig. 9.15. The control Ge PD performance at 10Gb/s shows the eye diagram opening is just 0.13 compared to a device integrated with photon-trapping that shows more than 0.5 eye diagram opening at 17V.

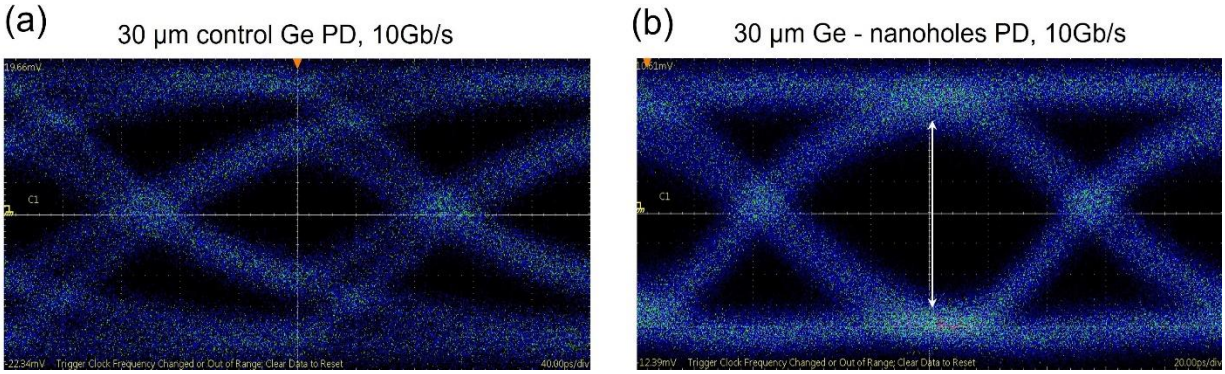


Fig. 9.16. Measured eye-diagram of a 30 µm Ge PDs at 10Gb/s, (a) control Ge PD (17V), (b) photon-trapping Ge PD (17V).

9.5.6 Optical performance prediction for thin photon-trapping Ge PD

Optical simulations are performed by an FDTD method, and the absorption efficiency of 500 nm thin Ge integrated with and without photon-trapping structures are further studied, as depicted in Fig. 9.17. Similar to the Ge with 2 μm thickness, photon-trapping thin 500 nm Ge exhibits dramatically higher absorption efficiency than the planar Ge counterpart. The photon-trapping design was optimized to incorporated PT structures with cylindrical holes diameter of 1200 nm and pattern periodicity of 1500 nm. This also proves that such enhancement in absorption is a direct consequence of enhanced light-matter interaction. More than 65% and 25% absorption efficiencies are observed at 1550 nm, and 1700 nm illumination wavelengths in Ge PT PD with 500 nm absorption thickness, respectively. By contrast, the absorption efficiency is less than 28% and 3% at 1550 nm, and 1700 nm illumination wavelengths in Ge control PD with 500 nm absorption thickness, respectively.

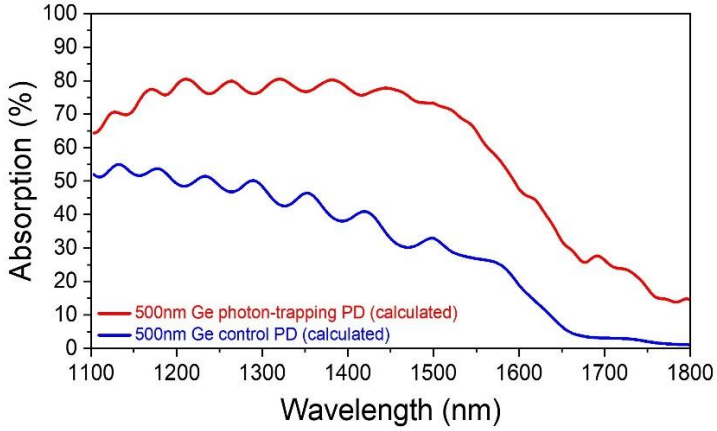


Fig. 9.17. Optical absorption calculated in 500 nm Ge photon-trapping PD vs. Ge control PD.

9.5.7 Estimated Enhanced 3dB bandwidth of operation for Ge PT PDs

Figure. 9.18 presents the estimated 3dB bandwidth of Ge PD for a variation of thin intrinsic layers thicknesses in a conventional (control) PD and enhanced performance with incorporation photon-trapping PDs (assuming a 50% of capacitance reduction) for different diameter device (fig. 9.18 (a-d)). As can be seen in fig. 9.18 (d), a PD with 8 μm of diameter is expected to have its highest 3dB frequency of operation over 100 GHz with only 0.2-0.4 μm of thickness. Enhancing the 3dB

frequency value >30% is feasible if 50% of its capacitance is reduced by utilizing photon-trapping designs. Sensors that require PDs with a significant area, such as single-pixel imagers, would be limited in speed of operation due to their large junction capacitance related with the area of the device. Nevertheless, photon-trapping structures implemented in such devices can decrease their capacitance, and enhance their speed of operation, enabling imaging systems with higher resolution as discussed in chapter 8 (8.3.2.4).

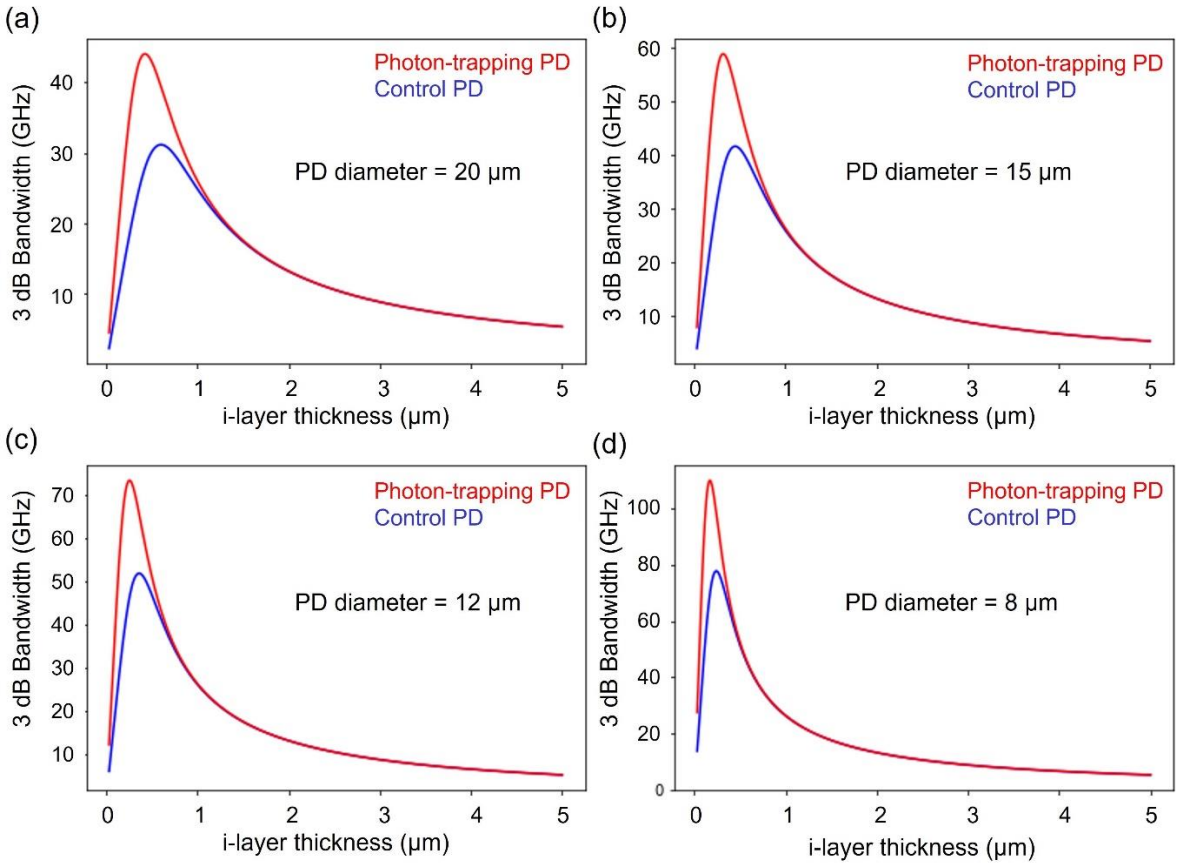


Fig. 9.18. Estimated 3dB bandwidth of operation for Ge PDs with different absorption layer thicknesses for: (a) 20 µm diameter PD. (b) 15 µm diameter PD. (c) 12 µm diameter PD. (d) 8 µm diameter PD. Photon-trapping Ge PDs shows enhanced bandwidth of operation for thinner devices such as 0.2-0.7 µm.

A CMOS -compatible high-speed and broadband efficient surface -illuminated Ge/Si PD integrated with photon-trapping holes is demonstrated. A significant enhancement in EQE in the range of 800 -1700nm (87% EQE at 1310 nm and 77% EQE at 1550 nm) and 10Gb/s high-speed performance is experimentally demonstrated. The PDs can be monolithically integrated with

CMOS electronics used for long-reach (LR)/ long haul (~10km) datacom optical links, PON transceivers, LIDAR systems, and extended single -mode new optical communication window (1620 -1700nm) beyond the L band up to U/XL (1625-1675nm) band.

References

[1] V. Houtsma, D. van Veen, and E. Harstead, "Recent progress on standardization of next-generation 25, 50, and 100G EPON," *Journal of Lightwave Technology,* vol. 35, no. 6, pp. 1228-1234, 2016.

[2] S. V. Firstov *et al.*, "A 23-dB bismuth-doped optical fiber amplifier for a 1700-nm band," *Scientific reports,* vol. 6, no. 1, pp. 1-6, 2016.

[3] Z. Li *et al.*, "Extreme short wavelength operation (1.65–1.7 μm) of silica-based thulium-doped fiber amplifier," in *Optical Fiber Communication Conference*, 2015: Optica Publishing Group, p. Tu2C. 1.

[4] T. Morioka, Y. Awaji, R. Ryf, P. Winzer, D. Richardson, and F. Poletti, "Enhancing optical communications with brand new fibers," *IEEE Communications Magazine,* vol. 50, no. 2, pp. s31-s42, 2012.

[5] H. Zhang *et al.*, "81 Gb/s WDM transmission at 2μm over 1.15 km of low-loss hollow core photonic bandgap fiber," in *2014 The European Conference on Optical Communication (ECOC)*, 2014: IEEE, pp. 1-3.

[6] P. Jouguet, S. Kunz-Jacques, A. Leverrier, P. Grangier, and E. Diamanti, "Experimental demonstration of long-distance continuous-variable quantum key distribution," *Nature photonics,* vol. 7, no. 5, pp. 378-381, 2013.

[7] R. Sabatini, M. A. Richardson, H. Jia, and D. Zammit-Mangion, "Airborne laser systems for atmospheric sounding in the near infrared," in *Laser Sources and Applications*, 2012, vol. 8433: SPIE, pp. 288-327.

[8] L. A. Sordillo, Y. Pu, S. Pratavieira, Y. Budansky, and R. R. Alfano, "Deep optical imaging of tissue using the second and third near-infrared spectral windows," *Journal of biomedical optics,* vol. 19, no. 5, p. 056004, 2014.

[9] S. Gunapala, B. Levine, D. Ritter, R. Hamm, and M. Panish, "InGaAs/InP long wavelength quantum well infrared photodetectors," *Applied physics letters,* vol. 58, no. 18, pp. 2024-2026, 1991.

[10] H. Ito, T. Furuta, S. Kodama, and T. Ishibashi, "InP/InGaAs uni-travelling-carrier photodiode with 310 GHz bandwidth," *Electronics Letters,* vol. 36, no. 21, p. 1, 2000.

[11] H. Cansizoglu *et al.*, "A new paradigm in high-speed and high-efficiency silicon photodiodes for communication—Part I: Enhancing photon–material interactions via low-dimensional structures," *IEEE Transactions on Electron Devices,* vol. 65, no. 2, pp. 372-381, 2017.

[12] H. Cansizoglu *et al.*, "A new paradigm in high-speed and high-efficiency silicon photodiodes for communication—Part II: device and VLSI integration challenges for low-dimensional structures," *IEEE Transactions on Electron Devices,* vol. 65, no. 2, pp. 382-391, 2017.

[13] J. S. Dunn *et al.*, "Foundation of RF CMOS and SiGe BiCMOS technologies," *IBM Journal of Research and Development,* vol. 47, no. 2.3, pp. 101-138, 2003.

[14] S. M. Sze, Y. Li, and K. K. Ng, *Physics of semiconductor devices*. John wiley & sons, 2021.

[15] Y. Lin *et al.*, "High-efficiency normal-incidence vertical pin photodetectors on a germanium-on-insulator platform," *Photonics Research,* vol. 5, no. 6, pp. 702-709, 2017.

[16] Y. Gao *et al.*, "High speed surface illuminated Si photodiode using microstructured holes for absorption enhancements at 900–1000 nm wavelength," *ACS Photonics,* vol. 4, no. 8, pp. 2053-2060, 2017.
[17] Y. Gao *et al.*, "Photon-trapping microstructures enable high-speed high-efficiency silicon photodiodes," *Nature Photonics,* vol. 11, no. 5, pp. 301-308, 2017.
[18] H. Cansizoglu *et al.*, "Surface-illuminated photon-trapping high-speed Ge-on-Si photodiodes with improved efficiency up to 1700 nm," *Photonics Research,* vol. 6, no. 7, pp. 734-742, 2018.
[19] S. Ghandiparsi *et al.*, "Up to 1700nm broadband high-efficiency surface-illuminated Ge/Si photodiode with microhole array," in *Integrated Photonics Research, Silicon and Nanophotonics*, 2019: Optica Publishing Group, p. IT3A. 3.

Chapter 10 Photon-trapping structures in III-V photodetectors for optical communication (850-1550 nm)

10.1 Modeling photon trapping structures to achieve high optical efficiency and ultra-high-speed GaAs PD for GaAs short-reach communication. (850 nm)

Data communication and telecommunication applications, beyond 400 Gbps link rate (200 Gbps single channel), demand simple and efficient short-reach optical communication technologies. Although GaAs-based photodetectors have been the dominant technology for decades, the application of sub-micron absorbers for ultra-high bandwidth, beyond 100 Gbps, is challenged due to low responsivity. This chapter utilizes frequency domain time domain (FDTD) simulations to demonstrate an ultra-fast- and high-efficient GaAs PIN photodiode integrated with photon-trapping nanohole structures. The proposed device with increased light-matter interaction within the thin-film (500 nm) GaAs layer exhibits more than 55% external quantum efficiency (EQE) at 850 nm. The data transfer rate can be as high as 100 Gbps Non-Return-Zero (NRZ) with no equalization.

10.1.1 Device Design

Figures 10.1 (a-b) show the various configurations of the simulated photon-trapping GaAs structures with different shapes of nanoholes. The holes are etched into the dielectric material such as the SiO_2 layer deposited on top of the 0.5 μm GaAs substrate. Figure 10.1 (c) shows the hexagonal closed-packed lattice arrangement of GaAs. In the structures illustrated Fig. 10.1 (d,e), the cylindrical and funnel-shaped nanoholes are integrated directly into the GaAs substrate. Frequency-domain time-domain (FDTD) simulations are used to calculate the electric field distribution within PD. A plane wave with wavelengths ranging between 775-875nm is normally incident to the surface of the PD. Periodic boundary conditions (PBC) are assumed laterally between unit cells, and perfect matching layer (PML) boundary conditions are set at the top and bottom of the GaAs PD. The photon absorption is calculated in the first step, where

electromagnetic field distributions are used as input parameters. The absorption (A) is obtained by subtracting the transmission (T) and the reflection (R) as A = 1–T–R. Next, the EQE/absorption, which is defined as the ratio of the total incident power on the PD to the number of photons absorbed in the intrinsic layer, is calculated, assuming that all the photogenerated carriers are collected by the electrodes. All simulations have been carried out using the commercial Lumerical FDTD simulation package.

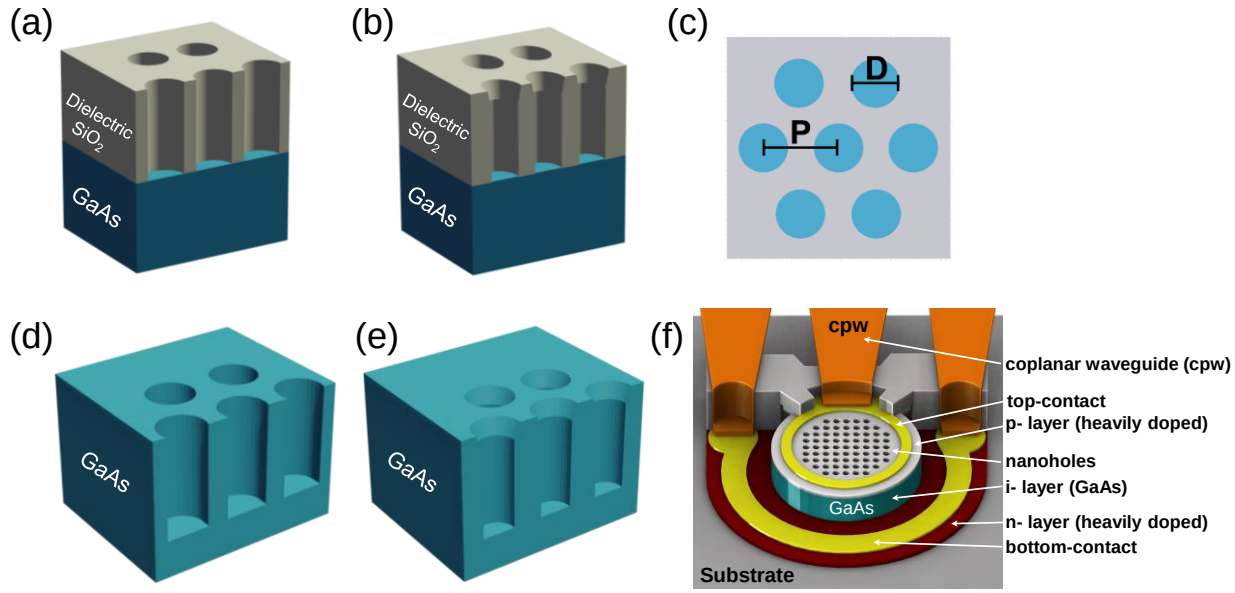


Fig. 10.1. Schematic of thin GaAs with photon trapping structures. (a) Cylindrical nanoholes embedded in SiO_2. (b) Funnel-shaped nanoholes embedded in SiO_2. (c) Hexagonal lattice where D is the diameter of holes and P is the periodicity of the holes. (d) Cylindrical nanoholes embedded in GaAs. (e) Funnel-shaped nanoholes embedded in GaAs. (f) Schematic of the complete pin GaAs device with photon-trapping design including coplanar waveguide (cpw) for ultra-fast operation.

10.1.2 Results and discussion

The integrated nanohole array patterned on top of the oxide or directly onto GaAs, bends the incoming vertical light into horizontal guided modes. This results in increased absorption efficiency by trapping the light in the thin layer of the absorbing material, where the amount of absorption depends on the shape, diameter (D), and depth in this chapter denoted as (d), while periodicity is denoted as (P) of the nanoholes. Different configurations of light-trapping nanostructures are integrated with GaAs PIN devices to evaluate their optical performance and select the most efficient structure. Absorption enhancement at 850nm window is studied which is ideal for the

short-reach (<300m) multi-mode data communications as well as the short wavelength division multiplexing (SWDM) band[1]. Incorporating the PT nanoholes increases the absorption, due to the improved coupling of vertically incident light into laterally propagating modes[2].

10.1.2.1 Photon trapping structures embedded in dielectric coated GaAs PD

Figure 10.2 (a) shows optical absorption enhancement by cylindrical nanoholes, in a hexagonal lattice, etched into SiO_2 on top of a 0.5 µm thin GaAs, which varies with the depth (d) of the nanoholes. The control device does not contain any photon-trapping (PT) nanoholes and is made by growing 0.5 µm thick SiO_2 on top of 0.5µm GaAs. The diameter (D) and the pitch (P) of the nanoholes are 700 nm and 1000 nm, respectively. The simulated structure is shown in the inset of each figure. Optical absorption drops sharply above 840nm as the bandgap of GaAs (1.42eV) is approached. At 850nm, the control device absorbs ~27% of the incident light while the rest is transmitted without any interaction with the absorber layer. The almost perpendicular bending of light results in the light propagating along the surface, producing enhanced light-matter interactions and an increase in the effective optical path of light. As the planar area of the device is reduced with increasing hole depth, reflection from the top surface is reduced and the absorption improves, such that the maximum nanohole depth (d = 0.5 µm) yields the highest absorption of ~37%, at λ = 850 nm. Figures 9.2(b) and (c) depict the absorption vs wavelength plots for varying diameter (D) and period (P) of the PT nanoholes, where the depth of the holes is fixed at 0.5 µm. A smaller hole diameter of ~ 100 nm induces strong scattering for shorter wavelengths (λ < 850 nm). The shorter wavelength absorption weakens while the longer wavelength (λ > 850 nm) absorption increases when the D/P ratio becomes larger[3]. The optimum D/P ratio is ~ 0.7, which provides the maximum absorption at λ = 850 nm when the depth of the holes reached 0.5 µm in SiO_2.

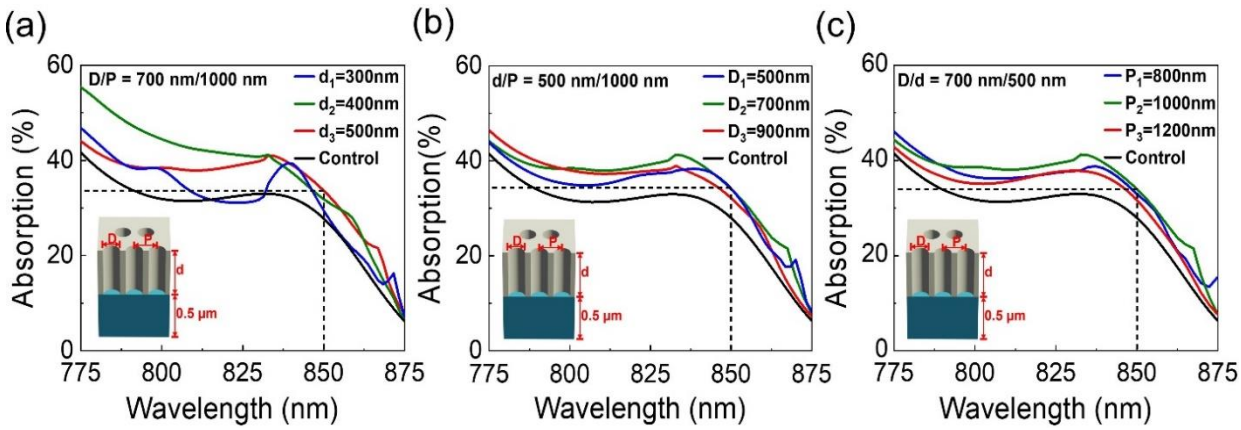


Fig. 10.2. Absorption as a function of wavelength for photon-trapping nanostructures, having cylindrical nanoholes etched into SiO_2 on top of GaAs substrate for varying (a) depth (d) (b) diameter (D) and (c) periodicity (P) of nanoholes. The control device in each case consists of 0.5 µm thick SiO_2 on top of 0.5 µm GaAs.

Light trapping using a cylindrical nanohole array can be tailored via different dielectric materials. Hafnium oxide (HfO_2) as a high-k material (>25 dielectric constant) and large bandgap (5.7eV) is one of the promising dielectric materials for advanced GaAs photonics applications [4]. With a dielectric constant that is 4-6 times higher than that of SiO_2, HfO_2 reduces interface states, which otherwise, would lead to Fermi-level pinning and mobility degradation. Figure 9.3 (a) shows the average absorption by cylindrical nanoholes etched into SiO_2, and HfO_2 placed on top of the GaAs substrate. It can be noticed that HfO_2 as a dielectric material noticeably enhanced the optical absorption in a wide spectrum of the incident wavelengths (775-875 nm). Additionally, the average absorption between λ = 775nm and 875nm, is maximum when hafnium oxide (HfO_2) is used as the dielectric material, as illustrated in Fig. 9.3 (b).

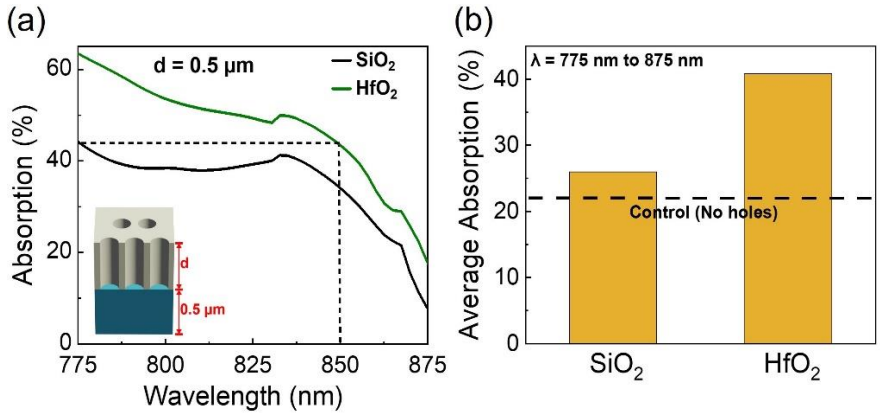


Fig. 10.3. Absorption as a function of wavelength for photon-trapping nanostructures, having cylindrical nanoholes etched into SiO_2 and HfO_2 dielectrics on top of GaAs substrate. For each dielectric, the depth of the nanoholes is 0.5 µm. (b) Average absorption between λ = 775nm and 875nm for different dielectrics. The control device in each case consists of 0.5 µm thick SiO_2 on top of 0.5 µm GaAs, without any nanoholes.

Light trapping by funnel-shaped nanoholes is also investigated. The bottom diameter is fixed at 700 nm as shown in Fig. 10.4 (a)-(c). Funnel holes produce a similar antireflection effect caused by the gradually changing refractive index and create an effect much like a graded refractive index antireflection coating[2, 5]. Due to the reduced reflection, a higher absorption efficiency is obtained when the D/P ratio is high. At a fixed diameter, a smaller period yields a higher filling ratio of PT nanoholes, reducing surface reflection[6].

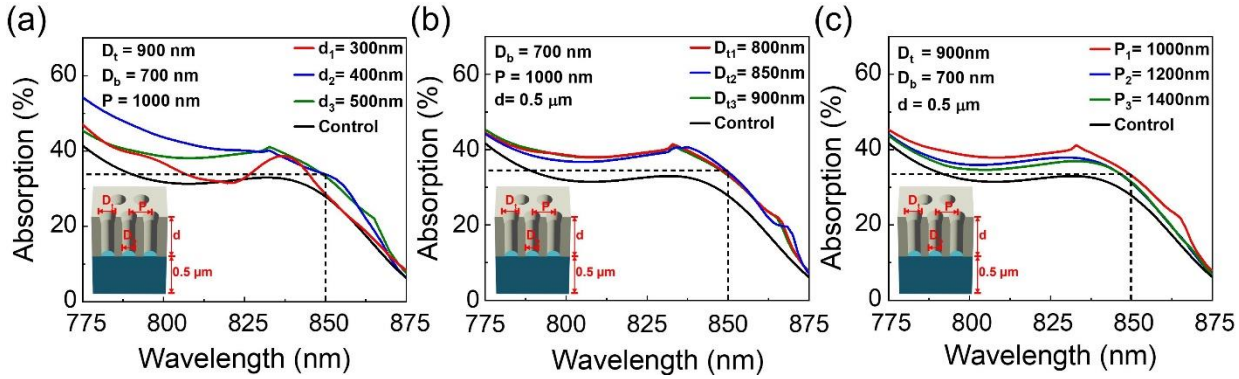


Fig. 10.4. Absorption as a function of wavelength for photon-trapping nanostructures, having funnel-profile nanoholes etched into SiO_2 on top of GaAs substrate for varying (a) depth (d) (b) top diameter (D) and (c) periodicity (P) of nanoholes. The bottom diameter is fixed at 700 nm and the control device in each case consists of 0.5 µm thick SiO_2 on top of 0.5 µm GaAs.

10.1.2.2 Photon trapping structures embedded in GaAs PD

Figure 10.5 (a) shows the absorption profile for the structure where the cylindrical PT nanoholes are directly patterned onto the GaAs substrate, while the structure in Fig. 9.4 (b) contains nanoholes that are etched through the top SiO_2 and the underlying GaAs layers. In both cases, maximum absorption of ~54% is achieved when the depth (t) of holes in the GaAs layer is 0.2 µm. Hence 0.2 depth is an optimum point where we can have a maximum absorption value. While deeper or shallower holes show smaller optical absorption.

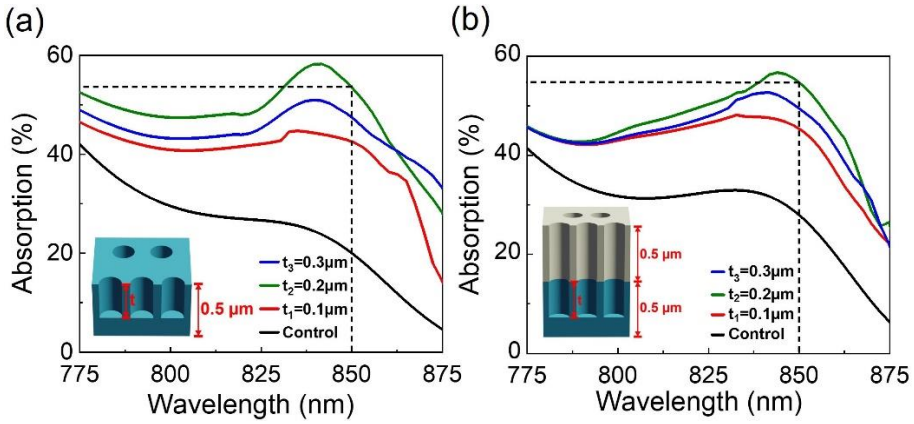


Fig. 10.5. Absorption as a function of wavelength for photon-trapping nanostructures, having cylindrical nanoholes etched into (a) GaAs and (b) top SiO_2 and bottom GaAs substrates for varying nanohole depth (t) in the GaAs layer. The control device in each case consists of 0.5 μm thick SiO_2 on top of 0.5 μm GaAs.

The absorption profile for structures with funnel holes in GaAs and SiO_2/GaAs is displayed in fig 10.6 (a) and (b), where t is the depth of the nanoholes in the GaAs substrate. The abbreviations: D_b refers to the bottom holes' diameter, t_2 refers to the bottom holes' depth, and t_1 refers to the top angled holes' depth.

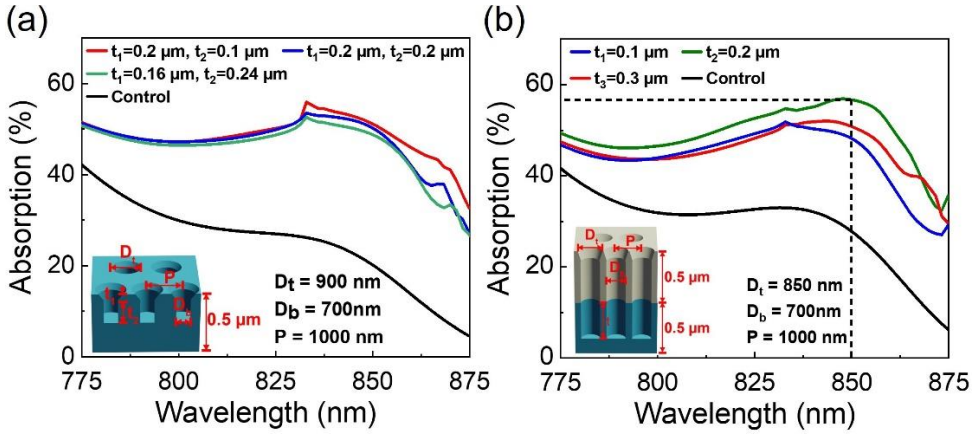


Fig. 10.6. Absorption as a function of wavelength for photon-trapping nanostructures, having funnel-profile nanoholes etched into (a) GaAs and (b) top SiO_2 and bottom GaAs substrates for varying nanohole depth (t) in the GaAs layer. The control device in each case consists of 0.5 μm thick SiO_2 on top of 0.5 μm GaAs.

10.1.2.3 Optical generation of carriers in photon-trapping GaAs

Figures 10.7 (b)-(g) show the optical generation of carriers for, conventional, cylindrical, and funnel-shaped PT structures embedded in SiO_2, extended to GaAs, and embedded in bare GaAs

with respect to the planar SiO_2 deposited on planar GaAs [Fig. 10.7 (a)], with no nanoholes, where the incident wavelength is 850 nm. Structures consist of PT nanoholes, etched into the SiO_2 layer [Fig. 10.7 (b) and (e)], which is placed on top of the GaAs substrate. The D/P ratio is 700 nm/1000 nm for the cylindrical and funnel-shaped nanoholes, where the top and bottom diameters are 900 nm and 700 nm, respectively. Figure. 10.7 (a) shows planar oxide on top of GaAs does not experience a high optical carrier generation when comparing to nanoholes cylindrical or funnel design etching only in the oxide layer [Fig. 10.7 (b) and (e). These results confer the impact of integrating nanoholes in the dielectric material without etching the semiconductor substrate to enhance the optical absorption. Figures 10.7 (c)-(f) show higher lateral optical modes are obtained from nanoholes extended from SiO_2 to GaAs, thus resulting in higher optical absorption. In each case, the depth of nanoholes in SiO_2 is 0.4 μm. Lateral modes are directed through the holes and into the adjacent absorbing layer. All devices have larger diameters (5-50 μm) in the lateral direction relative to the thickness in the vertical direction. Funnel-shaped holes provide a gradual change in the refractive index. This reduces reflection and so the modes are much stronger in these two configurations compared to the cylindrical structure where reflection is high due to the abrupt change in the index at the interface. The top diameter of the funnel-shaped PT structures, being closer to the wavelength of 850 nm, results in the strongest modes among all structures. Direct nanoholes embedding in GaAs is shown in Fig. 10.7 (d) and (g) for the cylindrical and funnel design nanoholes, respectively. The results show a higher photon accumulation in the x-z plane around the nanohole after coupling into laterally propagating modes and hence ultimately being absorbed. These results suggest that, embedding nanoholes directly into bare GaAs is the most efficient process to enhance optical absorption. However, embedding nanoholes into dielectric layer has the ability to enhance optical efficiency performance comparing to the conventional planar processes.

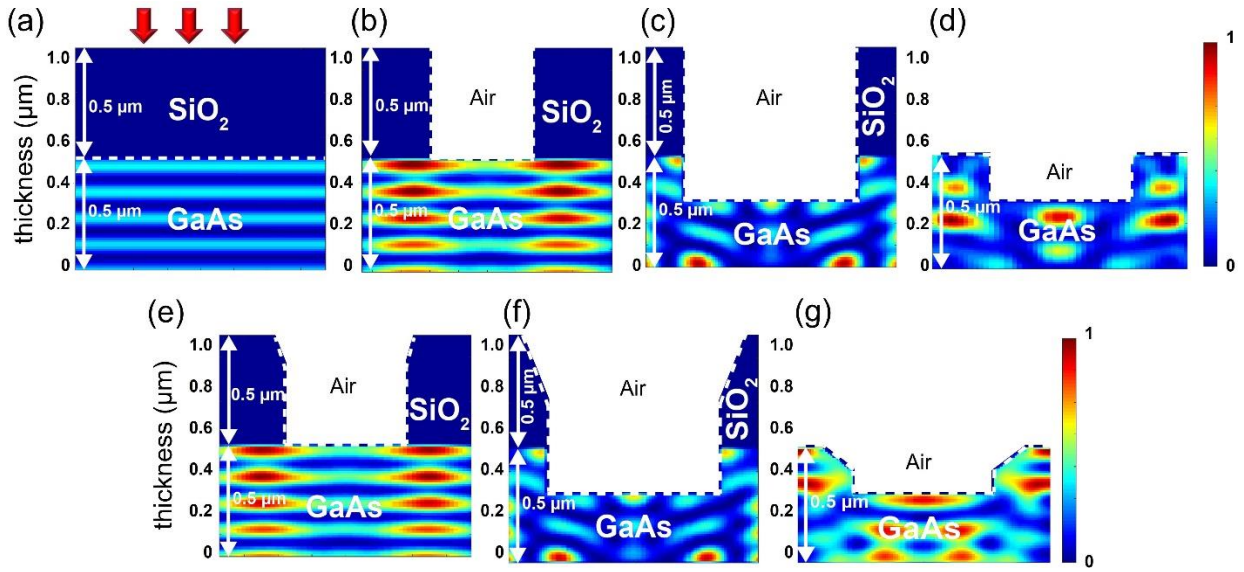


Fig. 10.7. Optical generation of carriers at λ = 850 nm with (a) SiO_2 on top of GaAs with no PT nanoholes in SiO_2 and with (b) cylindrical hole in SiO_2, (c) cylindrical hole in SiO_2 extended to GaAs, (d) cylindrical hole in GaAs, (e) funnel nanoholes in SiO_2, (f) funnel nanoholes in SiO_2 extended to GaAs, and (g) funnel nanoholes in GaAs.

The average absorption as a function of the D/P ratio for cylindrical and funnel-shaped of nanohole structures is shown in fig. 10.8 (a), where the nanoholes are etched into the SiO_2 layer placed on top of the GaAs substrate. The high (D/P) ratio shows high optical absorption values which increase as (D/P) varies from 0.4 to 1.0 due to the variation of holes arrays symmetries in the 2D plane. The maximum absorption presented by the control PD is about 23%, while the highest averaged absorption presented are for the cylindrical nanoholes and funnel nanoholes in GaAs for different patterns parameters. Figure 10.8 (b) compares the average absorption, between the incident wavelengths (λ = 775 nm - 875 nm), for PD structures with light trapping holes etched into SiO_2 on top of GaAs, into both SiO_2 and GaAs, and etched directly into GaAs (without the dielectric). The absorption by bare GaAs substrate is shown as a reference. It is observed that the average absorption is maximum when nanoholes are integrated directly into GaAs. While aligning holes in SiO_2 and in GaAs shows an enhanced optical absorption as well. Although direct etching in GaAs shows the maximum optical absorption, etching holes only on SiO_2 could avoid surface pinning challenges induced by nanoholes meanwhile enhancing optical

absorption. While Fig 10.8 presents average optical absorption results, the structures' designs can be optimized according to the desired wavelength, and optical performance can be further enhanced. It should be noted that surface pinning/defects in GaAs induced by nanoholes can be treated by an epitaxial GaAs regrowth process and/or an effective surface passivation process which leads to higher optical performance compared to the other designs.

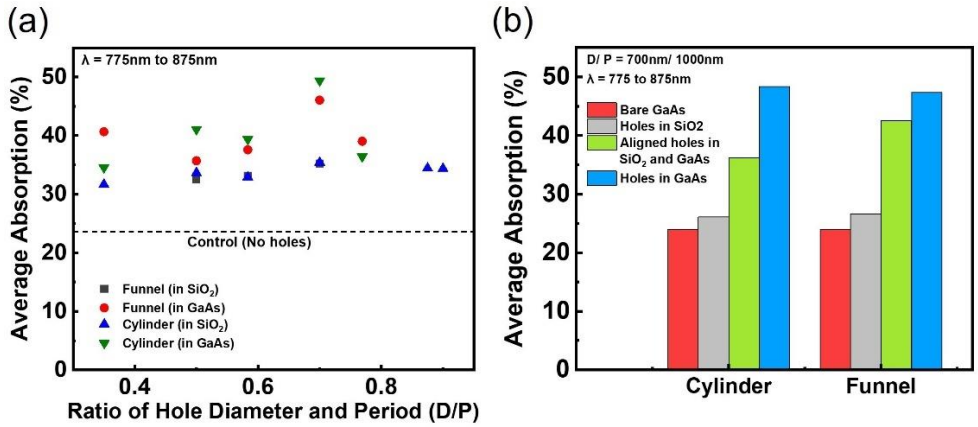


Fig. 10.8. (a) Average absorption, between λ = 775 nm and 875 nm, as a function of nanohole diameter/period (D/P) ratio for cylindrical, and funnel-shaped nanoholes, etched into SiO_2 on top of GaAs substrate (b) Average absorption by PT structures with different etch profiles, with respect to bare GaAs.

10.1.2.4 Photon trapping structures in dielectric extended to GaAs PD (misaligned nanoholes)

Reflection from the surface due to a significant mismatch between an in-plane component of wave vector (specifically normal incident) and the propagating mode poses a significant challenge in achieving highly efficient photodiodes. Numerous studies on suppressing the reflection, such as anti-reflection coatings and diffraction grating on the interface have been conducted[7, 8]. Gradual refractive index conversion from ambient (n_a) to absorbing material (n_s), results in an effective refractive index (n_{eff}) of the grating which satisfies $n_a < n_{eff} < n_s$ and leads to higher coupling of incident mode to propagating mode in the absorber[9]. Therefore, a hybrid structure could facilitate such a scheme to efficiently couple the incident mode to the lateral propagating mode in thin absorbers and enhance the absorption efficiency. The hybrid structure in Fig. 10.9 (a)-(b) shows the cylindrical holes in both SiO_2 and GaAs layers. Here, the diameters of holes in SiO_2 and GaAs are different. Larger holes (diameter = D_1) are integrated into the SiO_2 layer, and the

smaller holes (diameter = D_2) are integrated into the GaAs layer. While keeping the period P = 1000 nm, D_1 = 950 nm, and D_2 = 700 nm, the nanohole depth (t) in GaAs is varied from 0.1 µm to 0.3 µm as shown in Fig. 10.9 (c)-(d) where D_1 = 900 nm and 800 nm, respectively, while P = 1000 nm and a fixed D_2 = 700 nm. In each case, maximum absorption occurs when the optimum depth in GaAs reaches to t = 0.2 µm as observed in fig. 10.5. Figure 10.9 (e) summarizes the average absorption within the wavelength range of 775nm to 875nm, with respect to 0.5 µm flat GaAs. The average optical absorption results suggest that misaligned holes (SiO_2/GaAs) present around 63% average optical absorption for the incident wavelengths between (775-875 nm), whereas aligned holes (SiO_2/GaAs) present around 43% average optical absorption for the incident wavelengths between (775-875 nm) [Fig. 10.5 (b)]. Hence, hybrid nanohole structures can add an additional photon-trapping parameter to couple the light in the device layer and obtain a high-efficiency photodetector.

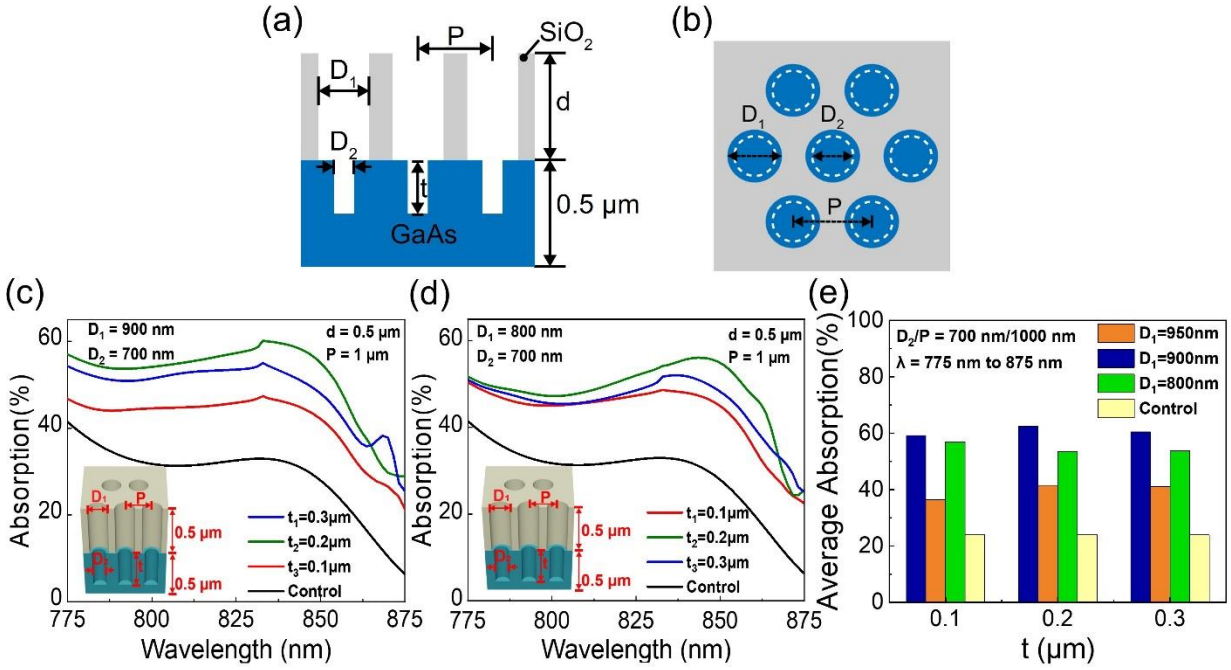


Fig. 10.9. (a) Cross-sectional view of PD with misaligned nanoholes in SiO_2 and GaAs (b) Top-view. Absorption at varying nanohole depth for (c) P = 1000 nm, D_1 = 900 nm and D_2 = 700 nm (d) P = 1000 nm, D_1 = 800 nm and D_2 = 700 nm, (e) Average absorption between λ = 775 nm and 875 nm for various etching depths.

10.1.2.5 3 dB bandwidth HFSS simulation of 25 μm, 8 μm, and 5 μm diameters photodiodes with different nanoholes filling-ratios

The frequency response of the photodetector with 25 μm, 8 μm, and 5μm diameter is shown in Figs. 10.10 (a)-(c), respectively. The 3 dB bandwidth of the photodetector depends on the RC time constant and the transit time. Smaller photodetectors have smaller junction capacitance, leading to a smaller RC time constant, and as a result, more 3 dB bandwidth. The photodetector is a parallel-plate capacitor with the capacitance of $C = \varepsilon_0 \varepsilon_r A/d$, where ε_0 is the permittivity of the vacuum, ε_r is the permittivity of the GaAs in this case, where A is the junction area, and d is the thickness of the i-layer. Therefore, as the diameter of the PD decreases, the junction area decreases, and the PD capacitance also decreases. Moreover, the integrated nanoholes in the PD reduce the cross-sectional junction area, which also decreases the junction capacitance even further. Thus, the existence of nanoholes leads to a higher 3 dB bandwidth of the PD. This can be verified by the frequency response of the photodetector shown in Fig. 10.10 (a)-(c). As the percentage of the nanoholes in the PD increases which represents by the filling fraction (ff) ($Area_{nanoholes}/Area_{PD}$), the 3 dB bandwidth of the PD also increases. To extract the junction capacitance and resistance, the PD has been modeled and simulated using ANSYS high-frequency structure simulator (HFSS) tool. The S-parameter of the device with different diameters and nanoholes filling ratio is simulated using HFSS and the junction capacitance and resistance were calculated in Virtuoso Cadence based on the S-parameter results.

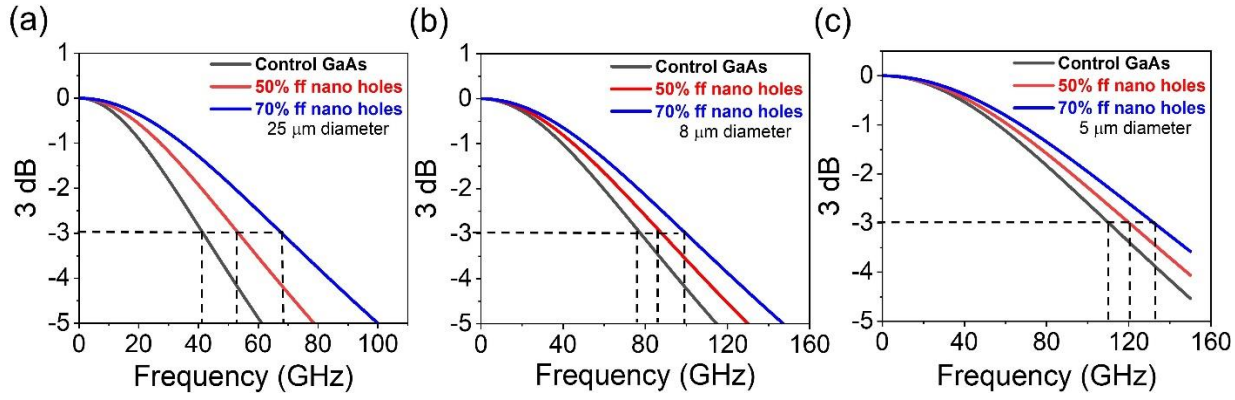


Fig. 10.10. Frequency response of the photodetector with (a) 25µm diameter for planar GaAs, 50% ff nanoholes, 70% ff nanoholes. (b) 8µm diameter for planar GaAs, 50% ff nanoholes, 70% ff nanoholes. (c) 5µm diameter for planar GaAs, 50% ff nanoholes, 70% ff nanoholes.

The equivalent small-signal circuit of the PD can be shown in Fig. 10.11. The C_j is the PD junction capacitor, while the R_{PD} represents the series resistance of the PD. The current source I_{PD} models the photocurrent. It is worth mentioning that the L_S and R_S represent the inductance and parasitic resistance of the coplanar waveguide (CPW) which is used in fabrication for measurement purposes.

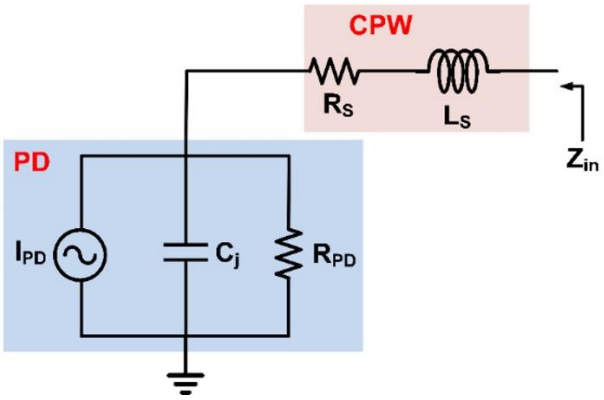


Fig. 10.11. Equivalent small-signal circuit of PD including CPW.

The CPW is assumed to be similar for all devices with LS =130 pH inductance and RS =1.33 Ω parasitic resistance at low frequencies. These values are based on the ANSYS HFSS simulation of typical CPWs utilized in the photodetector fabrications. Table 10.1 summarizes the PD parameters for different diameters and nanohole filling fractions (ff).

Device	C_j (fF)	R_{PD}(Ω)
5µm (Control)	15.5	65
5µm (50 % ff Holes)	10.5	70
5µm (70 % ff Holes)	7	74
8µm (Control)	34.6	28
8µm (50 % ff Holes)	23.7	35
8µm (70 % ff Holes)	18.3	40
25µm (Control)	107	7
25µm (50 % ff Holes)	66.7	14
25µm (70 % ff Holes)	44.9	18

Table 10.1. The parameters for the equivalent small-signal circuit of the PD. PDs diameters are 5 µm, 8 µm and 25 µm.

The S11 parameters of the equivalent small-signal circuit, which is shown, in Fig. 10.12 is simulated in Virtuoso Cadence. The simulated S11 of the PD with 25 µm, 8 µm, and 5 µm nanohole diameter for -150 GHz frequency range is presented in Fig. 10.12(a)-(c), respectively.

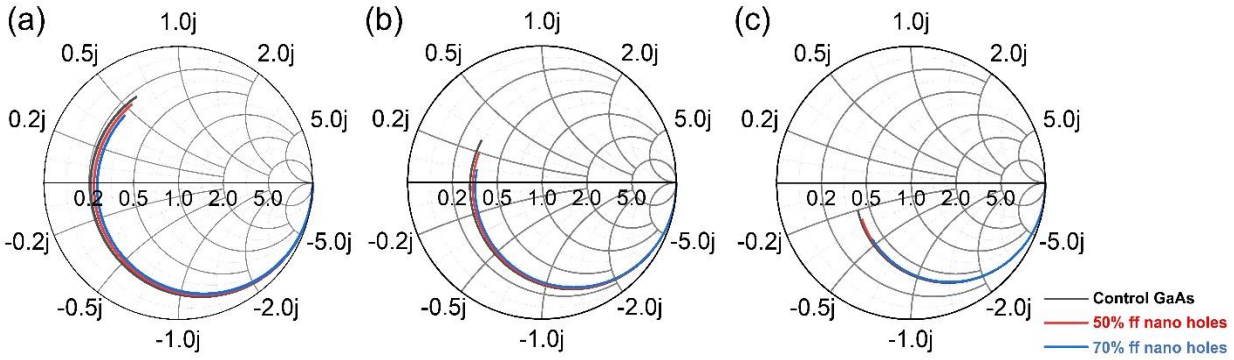


Fig. 10.12. (a) S11 parameters of the PD with 25µm diameter from 1-150GHz (b) S11 of the PD with 8µm diameter from 1-150GHz (c) S11 of the PD with 5µm diameter from 1-150GHz

As can be seen from the S11 simulation results shown in Fig. 10.12, the devices are not matched to 50 Ω termination. Therefore, there needs to be careful design consideration for the CPW as well as a matching network to match the input impedance of the devices to 50 Ω for the maximum power transfer. In addition, a transimpedance amplifier (TIA) can be designed and connected to the PD to improve the output power of the PD's signal in future designs. The large bandwidth of the proposed devices requires high bandwidth TIAs and matching networks which is possible to design and implement on-chip in modern technologies.

10.2 Modeling photon trapping structures to achieve high optical efficiency and ultra-high-speed In0.53Ga0.47As PIN PD long-reach communication. (1550 nm)

$In_{0.53}Ga_{0.47}As$-based photodetectors (PDs) with ultra-fast and high efficiency can be obtained through the implementation of photon-trapping holes (PT) to enable high photon absorption capability and enhance PD's operational speed. It has been demonstrated that a perpendicular light beam could be bent to allow guiding parallel to the surface of the photodetectors, greatly enhancing the interaction of light with the absorption material. PDs with photon trapping structures

can inhibit broadband reflection and improve broadband absorption by photon manipulation and slow light. This section discusses the simulation, device epi-structure growth, and fabrication of $In_{0.53}Ga_{0.47}As$ PT PD. The results show that the EQE is enhanced by ~ 3x with PT holes with only 700 nm $In_{0.53}Ga_{0.47}As$ active layer compared to the conventional InGaAs photodetectors. Additionally, bandwidth can be enhanced to meet future THz optical detection and communication demand in the C and L bands as well as other emerging applications. Based on PT approach, $In_{0.53}Ga_{0.47}As$ PT PDs have the potential to be operational with >250 Gbps data transmission rate and around 70% detection efficiency.

10.2.1 Device Design

Figures 10.13 (a-b) show the PIN structure of the modeled $In_{0.53}Ga_{0.47}As$ PT PD. Figure 10.13 (a) shows the complete structure of the PD, while Fig. 10.13 (b) shows the cross-section of the structure. The FDTD simulated structures are designed to be hexagonal lattice since it provides higher optical confinement and absorption.

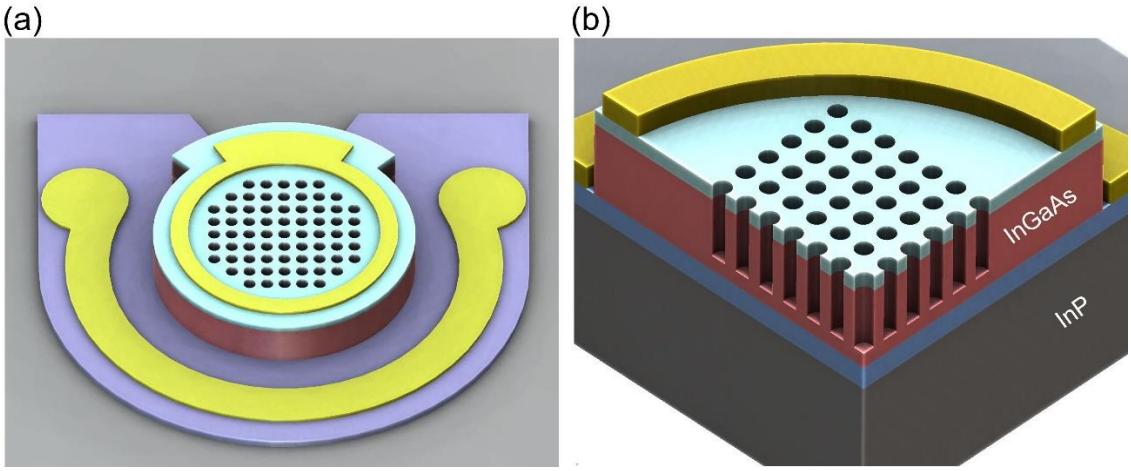


Fig. 10.13. Schematic of $In_{0.53}Ga_{0.47}As$ PT PD. (a) complete $In_{0.53}Ga_{0.47}As$ pin PT PD. (b) Cross-section of the $In_{0.53}Ga_{0.47}As$ PT PD.

10.2.2 Results and Discussion

Chapter 1 The integrated nanohole array modeled and integrated into $In_{0.53}Ga_{0.47}As$ bends the incoming vertical light into horizontal guided modes. This results in increased absorption efficiency by trapping the light in the thin layer of the absorbing material, where the amount of absorption

depends on the shape, diameter (D), and depth in this chapter denoted as (d), while periodicity is denoted as (P) of the nanoholes. A control PD with a planar surface is also designed as a reference to compare the absorption enhancement with photon-trapping nanoholes. The surface-illuminated $In_{0.53}Ga_{0.47}As$ PT PD can provide a high EQE for the potential application to long-haul data communication links. The EQEs of PDs with PT holes integrated into $In_{0.53}Ga_{0.47}As$ is enhanced by around 3x as compared to fabricated control PDs, which is promising for the realization of optical receivers for data transmission with both high efficiency and ultra-fast operation.

10.2.2.1 Optical simulation for In0.53Ga0.47As photon-trapping PD

Optical simulations were carried out to study the absorption of light in the control and photon-trapping devices. Figures 10.14 show the results of finite difference time domain (FDTD) simulations calculated for broadband wavelength vs. the absorption of light illuminating at a 0^o incidence angle. The photon-trapping structure with cylindrical nanohole 1500/1900/250 nm is designed for $In_{0.53}Ga_{0.47}As$. Furthermore, a control device with a planar surface is designed as a reference to compare the absorption enhancement with photon-trapping structures. In control devices, photons do not experience perpendicular bending and continue to propagate in a vertical orientation. The simulation predicted that $In_{0.53}Ga_{0.47}As$ PDs with photon-trapping structures could absorb light about ~2.3x more than control PD.

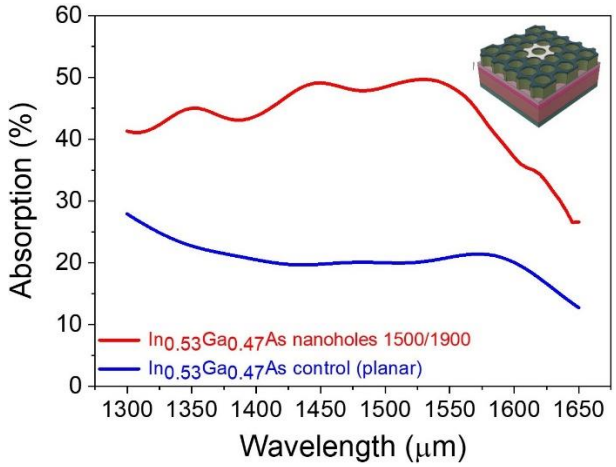


Fig. 10.14. FDTD Simulation for 0.5μm thin $In_{0.53}Ga_{0.47}As$ control vs. PT nanoholes.

10.2.2.2 Unique optical absorption response with different photon-trapping nanoholes In0.53Ga0.47As PD

As can be seen in Fig. 10.15 (a), the optical absorption of $In_{0.53}Ga_{0.47}As$ layers with varying thicknesses (0.25, 0.5, and 1 μm) and shallow holes (100 nm with fixed p/d) shows different absorption profiles. A 0.5 μm thick device layer can achieve an absorption of 1 μm at λ=1500 nm, which shows an opportunity to optimize the design of the PT nanoholes to enhance the performance of such devices by minimizing these devices' thicknesses. Figure 10.15 (b) shows the absorption results for different $In_{0.53}Ga_{0.47}As$ PT with a fixed device thickness, and varied PT hole diameters. The results present a unique optical pattern response assigned to different PT designs (diameter in this case). $In_{0.53}Ga_{0.47}As$ does not absorb photons as efficiently around its bandgap cut-off as other materials. However, FDTD results show that PT nanoholes can be utilized to push $In_{0.53}Ga_{0.47}As$ absorption limits slightly beyond λ=1700 nm and modify its effective absorption coefficient. Figure. 10.15 (c) presents a set of unique optical absorption responses through varying the periodicity of PT nanoholes. All these parameters, including PT etching profiles, depth, and dielectric coating parameters could lead to the design an efficient $In_{0.53}Ga_{0.47}As$ PD for the desired operating optical window.

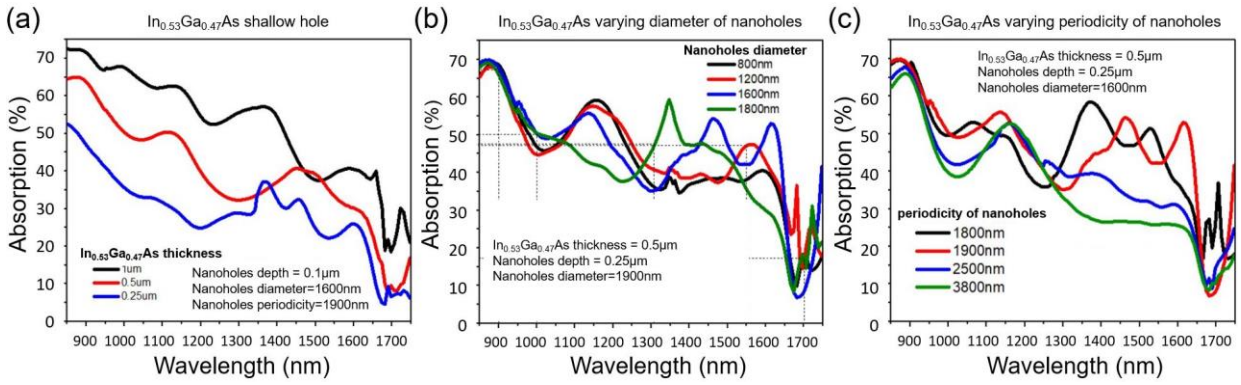


Fig. 10.15. FDTD simulation for $In_{0.53}Ga_{0.47}As$ absorption vs. incident wavelengths. (a) $In_{0.53}Ga_{0.47}As$ varying thickness and shallow hole etched. (b) $In_{0.53}Ga_{0.47}As$ varying diameters of holes and fixed thickness, and fixed holes depth. (c) $In_{0.53}Ga_{0.47}As$ varying periodicity of holes and fixed thickness, and fixed holes depth.

10.2.2.3 In0.53Ga0.47As PD molecular beam epitaxy (MBE) epitaxial growth on GaAs substrate

The structure was grown in a Gen II MBE system on a semi-insulating (SI) GaAs substrate [10]. All layers were doped by Si at a nominal Si doping centration of $5\times10^{14}cm^{-3}$ (the value is derived from beam flux-cell temperature curve but not calibrated). Firstly, a 500 nm thick GaAs layer was grown on an oxide-removed substrate at 580°C to provide a better growth surface for $In_xGa_{1-x}As$. Then the grown layer was step-graded in indium concentration to x = 0.53 at 530°C. The step grading rate was set low enough (increasing x value by 0.025 in every ~100 nm) to provide smooth lattice constant transition and avoid defects brought by lattice mismatch as much as possible. After the grading layer, a 700 nm thin $In_{0.53}Ga_{0.47}As$ layer was grown to serve as the active layer for the photodetector (PD). Finally, the last layers were another grading layer from $In_{0.53}Ga_{0.47}As$ to GaAs, the growth structures can be seen in fig. 10.16. The grading layer could provide a high Schottky barrier at the detector contacts and provide a barrier to prevent the photo-generated carriers from being trapped at the surface states.

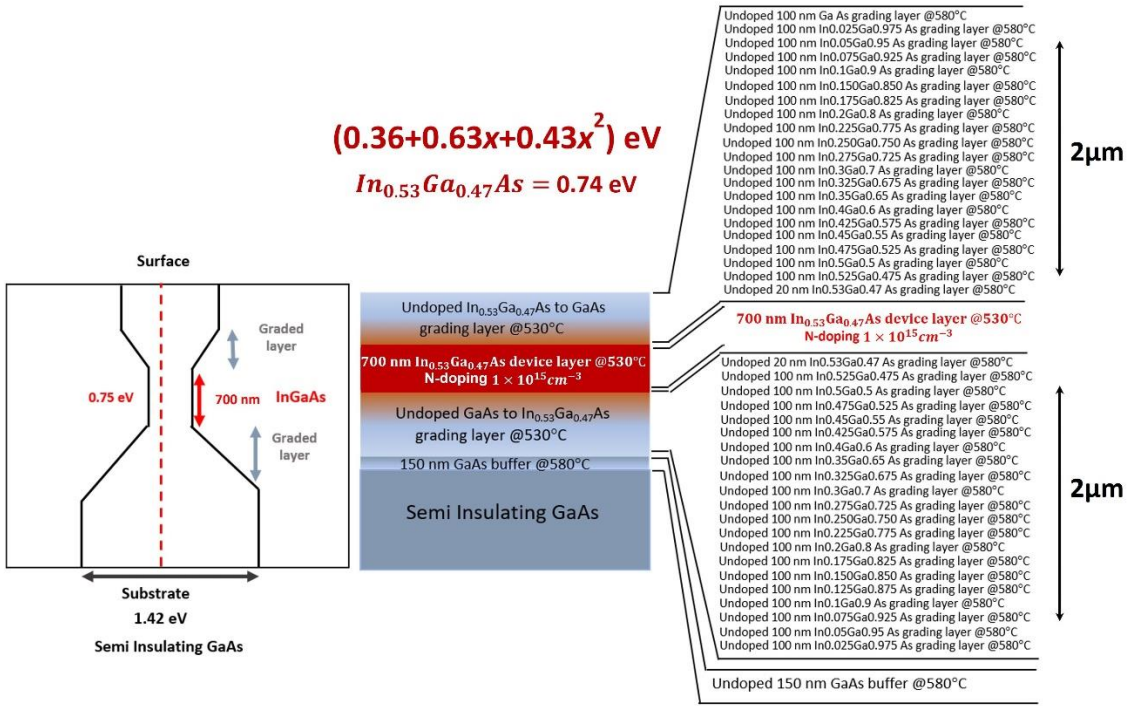


Fig. 10.16. $In_{0.53}Ga_{0.47}As$ PD epitaxial growth structure.

10.2.2.4 SEM/EDS Analysis

The scanning electron microscope (SEM) image of the grown structure and energy dispersive spectroscopy (EDS) profile were measured by an FEI Scios Dual Beam FIB/SEM system equipped with an Oxford EDS detector. As can be seen in Fig. 10.17 (a), the cross-sectional EDS line scanned along with the growth layers. Quantitative EDS analysis indicated the increase of (In) component gradually up to the active layer to form the desired $In_{0.53}Ga_{0.47}As$ device layer. Figure 10.17 (b) shows an SEM image of the cross-sectional growth, the field color contrast shows the epitaxially graded layers.

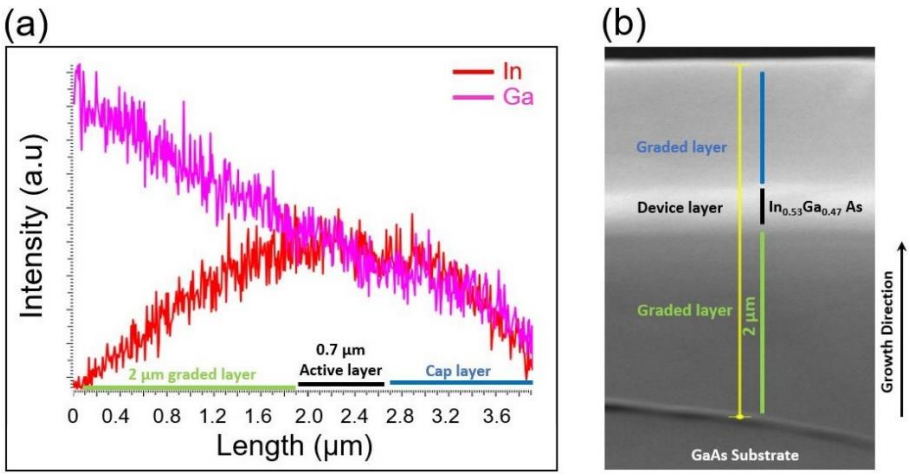


Fig. 10.17. (a) Cross-sectional EDS measurement across the grown structure, showing (In) component is increasing up to the device layer. (b) Cross-sectional SEM image of the grown structure.

10.2.2.5 Device Fabrication

10.2.2.5.1 Photolithography

The starting GaAs with grown $In_{0.53}Ga_{0.47}As$ layer wafer was pre-cleaned in piranha solution to remove any organic contaminants. Then, the wafer was spin-coated with hexamethyldisilane HMDS to promote adhesion of the photoresist. After that, S1813 photoresist is coated with a 2.1 µm thickness. Subsequently, the pattern of the holes was generated by photolithography using EVG 620 mask aligner.

10.2.2.5.2 Photon-trapping holes formation

After the holes were patterned, the wafer was put inside an oven at 120°C to hard bake the photoresist. Reactive Ion Etch (RIE) PlasmaTherm Apex SLR RIE/ICP is used to form cylindrical holes with a depth of 2.5 μm.

10.2.2.5.3 Mesa Isolation

After etching the designed nanoholes, the device was isolated by mesa etching to the GaAs SI substrate. The SEM images in fig. 10.18 show fabricated $In_{0.53}Ga_{0.47}As$ with hole sizes of 1.5 μm and 2μm. The SEM images show the hexagonal and square photon-trapping unit cells with funnel-shaped profiles. Figure 10.18 (a,b) are designed to study and analyze the lateral optical propagation and absorption test structures.

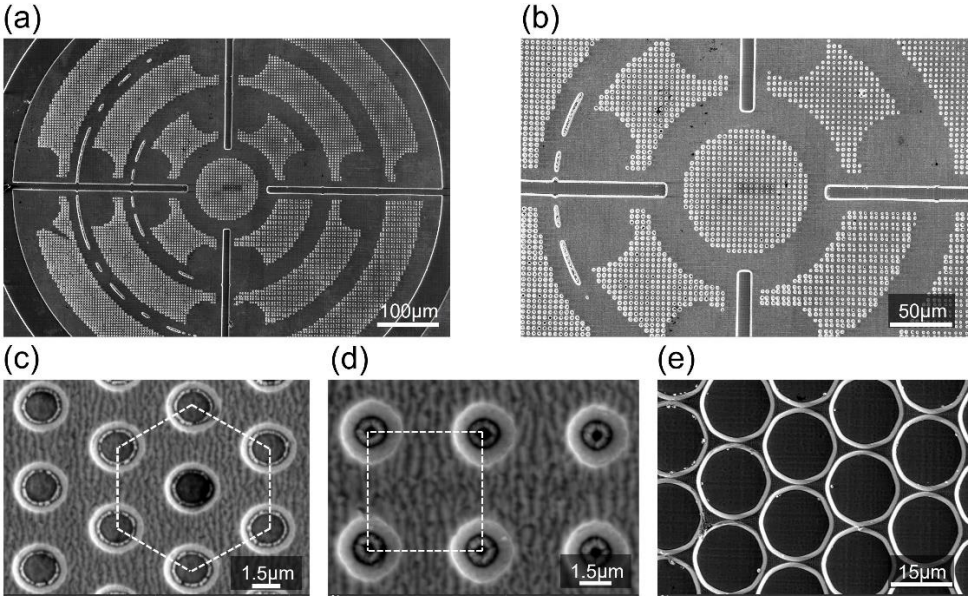


Fig. 10.18. SEM images for the fabricated $In_{0.53}Ga_{0.47}As$ PT PD. (a,b) Lateral optical propagation test structures. (c) Hexagonal lattice PT holes. (d) Square lattice PT holes, holes are funnel-shaped. (e) Large diameter compact holes.

10.2.2.6 Optical characterization

The reflection measurement of the fabricated devices is depicted in Fig. 10.19. The measured light reflectance from the sample's surface confirmed that PT holes arrays not only contribute to efficient photon-trapping but also act as an effective anti-reflection coating for broadband wavelengths. Finding efficient but simple methods to suppress reflectance has always been a

challenging issue for the photodetection community. Therefore, employing PT holes is a promising way to reduce reflection without adding extra steps to fabrication processes. Experimental observations were carried out to measure the reflection from the surface of the control PD as well as the surface of the PT holes PD from 300 nm up to 1050 nm. The available characterization setup allows us to measure up to a 1050 nm wavelength. Nevertheless, the measurements clearly show the efficacy of PT holes in reducing light reflection in broadband wavelengths. Control PDs show very high reflection, as shown in Fig. 10.19. For the incident wavelength of 850 nm, the PT PDs exhibit a reflection of about 25%, compared to approximately 77% for control PD with planar surfaces. The high reflection is attributed to the graded layer that was grown epitaxially on the device layer which acts as a semi-reflecting cap layer.

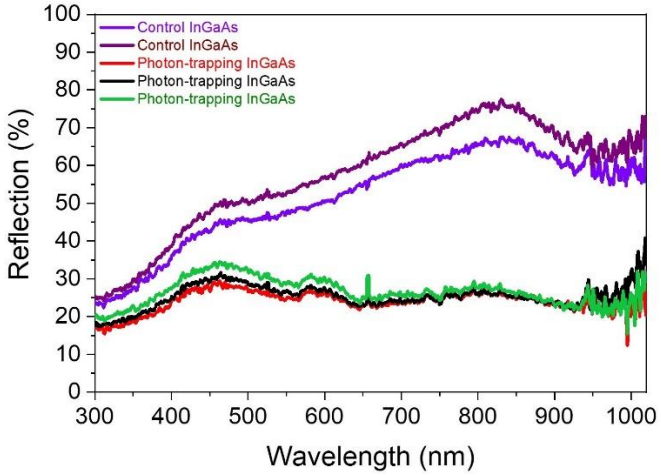


Fig. 10.19. Experimentally measure of the fabricated $In_{0.53}Ga_{0.47}As$ control PD and $In_{0.53}Ga_{0.47}As$ PT PD reflection vs. wavelengths from 300 nm-1050 nm

10.2.2.7 EQE characterization and optical enhancement

Figure 10.20 shows the EQE characterization results of the fabricated $In_{0.53}Ga_{0.47}As$ PDs. The impinging light was divided into two fiber patch cords with a splitter; one was connected to a fiber probe that delivered the incident light to the device under test. In contrast, the other patch cord was connected to a power meter to monitor the optical power of incident light in real time. A supercontinuum laser was used to tune the wavelength of the incident light. Figure 10.20 (a) shows $In_{0.53}Ga_{0.47}As$ control PD EQE for a variety of wavelengths (700 nm to 1500 nm). For the

control devices as shown in Figure 25 (a), the EQEs are as low as ~8% for an incident wavelength of 1550nm with −4.5V bias. The active layer of $In_{0.53}Ga_{0.47}As$ is around 0.7 μm, which is considerably thinner than the 2 μm that has been used in such detectors. The low quantum efficiency is anticipated to have a high reflection on the top surface of the device due to the graded layers that act as a semi-reflecting layer. PT holes array allows lateral propagating waves leading to enhanced photon-matter interactions and result in a measured maximum EQE of 62% at 1550 nm when biased with −4.5V. This proves the efficacy of the photon-trapping holes in enhancing light interaction with thin III-V semiconductors. Another advantage of the photon-trapping holes is high broadband efficiency. This combination of broadband high efficiency and high speed makes III-V PDs with photon-trapping holes favorable for many important applications. It should be noted that the fabricated devices were showing a relatively high leakage current. Hence, an effective passivation process is needed to address it. Wet etching and/or material epitaxial regrowth can be utilized as well to avoid/terminate the induced surface states. The enhancement factor of the thin 0.7 μm thin photon-trapping $In_{0.53}Ga_{0.47}As$ PD is higher than that of the bulk $In_{0.53}Ga_{0.47}As$ PD over a broad near-infrared (NIR) wavelength spectrum as can be seen in Fig. 10.20 (c).

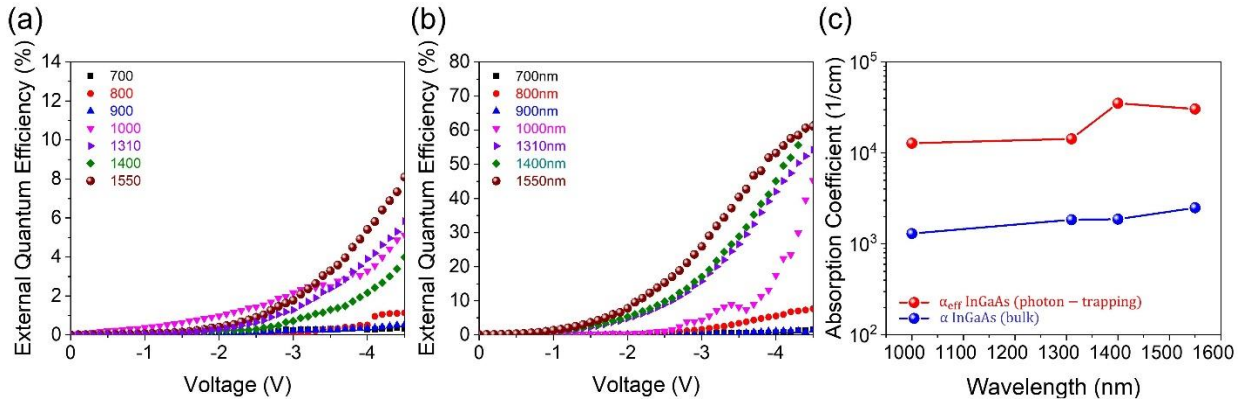


Fig. 10.20. Optical enhancement in PT $In_{0.53}Ga_{0.47}As$ PD. (a) Experimentally measured EQE for $In_{0.53}Ga_{0.47}As$ control PD. (b) Experimentally measured EQE for $In_{0.53}Ga_{0.47}As$ PT PD. (c) Enhanced absorption coefficient (α_{eff}) of the photon-trapping PD and the intrinsic absorption coefficient of bulk $In_{0.53}Ga_{0.47}As$.

10.2.2.8 Ultimate Bandwidth-Efficiency

In III-V PIN photodetectors, the 3dB bandwidth can be modeled based on two parameters: the carrier transit time (t_r) and the RC constant time as given in Equation. 10.1:

$$f_{3db} = \frac{1}{\sqrt{(2\pi \mathrm{RC})\ 2 + (t_r/0.44)}} \tag{10.1}$$

By considering the PIN PD as a parallel plate, the capacitance can be written as $C=\varepsilon_o\varepsilon_r A/w$, where εo and ε_r are the permittivity of vacuum (8.84 x 10-12 F/m) and $In_{0.53}Ga_{0.47}As$ (12.96), respectively; w is the depletion layer width, typically the intrinsic-layer, and A is the junction area. The use of a thin intrinsic layer reduces the transit time but increases the junction capacitance in control (planar) devices. However, the introduction of an array of photon-trapping structures (holes) leads to the reduction of the effective cross-section area and materials of the PD. Consequently, the overall junction capacitance of the PD is assumed to be reduced. Figure 10.21 shows the calculated PIN 3dB bandwidth enhancement for GaAs and $In_{0.53}Ga_{0.47}As$ PT PDs. These enhancements are attributed to the reduction of 50% of junction capacitance due to the PT holes junction reduction. The blue curves show control photodetector 3dB values, whereas orange curves show PT photodetectors 3dB enhancements for 12μm diameter devices. Figure 10.21 (a,b) show the efficacy of PT design to enhance the 12μm diameter devices with a thickness of 0.5 μm to operate at 140 GHz for GaAs, and 175 GHz for $In_{0.53}Ga_{0.47}As$. 3dB values can be even enhanced since optical communication PDs diameter for long-haul communication is designed around 8 μm, which is equal to a single fiber core's diameter. CMOS foundries have the capability to further reduce the capacitance by integrating the photon-trapping holes more compactly (reduce capacitance > 60% with 8m PD's diameter) which will offer a higher 3db bandwidth and ultra-fast operation capabilities.

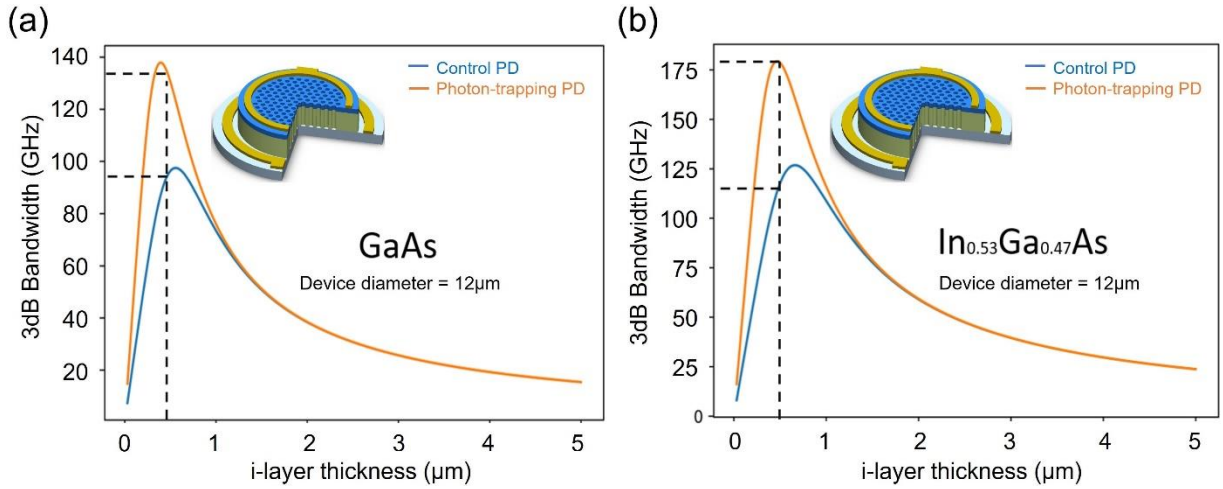


Fig. 10.21. Ultimate bandwidth for GaAs and $In_{0.53}Ga_{0.47}As$. (a) 3db bandwidth of operation for GaAs PDs with different layer thicknesses (control vs. PT). (b) 3db bandwidth of operation for $In_{0.53}Ga_{0.47}As$ PDs with different layer thicknesses (control vs. PT).

The reduction of capacitance can also promote sensors that involve PDs with a large area, such as single-pixel image sensors. These sensors are normally limited in speed of operation due to their large junction capacitance related to the area of the device. Therefore, photon-trapping arrays implemented in such devices can decrease their capacitance, and enhance their speed of operation, enabling imaging systems with higher resolution[11].

References

[1] J. A. Tatum *et al.*, "VCSEL-based interconnects for current and future data centers," *Journal of Lightwave Technology,* vol. 33, no. 4, pp. 727-732, 2015.

[2] Y. Gao *et al.*, "Photon-trapping microstructures enable high-speed high-efficiency silicon photodiodes," *Nature Photonics,* vol. 11, no. 5, pp. 301-308, 2017.

[3] L. Hong *et al.*, "Light trapping in hybrid nanopyramid and nanohole structure silicon solar cell beyond the Lambertian limit," *Journal of Applied Physics,* vol. 116, no. 7, p. 074310, 2014.

[4] B. Lu, H. Lv, Y. Zhang, Y. Zhang, and C. Liu, "Comparison of HfAlO, HfO2/Al2O3, and HfO2 on n-type GaAs using atomic layer deposition," *Superlattices and Microstructures,* vol. 99, pp. 54-57, 2016.

[5] J.-Q. Xi *et al.*, "Optical thin-film materials with low refractive index for broadband elimination of Fresnel reflection," *Nature photonics,* vol. 1, no. 3, pp. 176-179, 2007.

[6] J. Gou *et al.*, "Rigorous coupled-wave analysis of absorption enhancement in vertically illuminated silicon photodiodes with photon-trapping hole arrays," *Nanophotonics,* vol. 8, no. 10, pp. 1747-1756, 2019.

[7] K. Askar *et al.*, "Self-assembled self-cleaning broadband anti-reflection coatings," *Colloids and Surfaces A: Physicochemical and Engineering Aspects,* vol. 439, pp. 84-100, 2013.

[8] A. S. Sarkın, N. Ekren, and Ş. Sağlam, "A review of anti-reflection and self-cleaning coatings on photovoltaic panels," *Solar Energy,* vol. 199, pp. 63-73, 2020.

[9] S. Mokkapati and K. Catchpole, "Nanophotonic light trapping in solar cells," *Journal of applied physics,* vol. 112, no. 10, p. 101101, 2012.
[10] W. P. McCray, "MBE deserves a place in the history books," *Nature nanotechnology,* vol. 2, no. 5, pp. 259-261, 2007.
[11] E. Ponizovskaya-Devine *et al.*, "Single Micro-hole per Pixel for Thin Ge-on-Si Image Sensor with Enhanced Sensitivity upto 1700 nm," *arXiv preprint arXiv:2209.14242,* 2022.

Chapter 11 Photon-trapping in GaSb/InGaAs Multi Quantum Well (MQW) Photodetectors

11.1 High performance GaAsSb/InGaAs Multi Quantum Well (MQW) Photodetectors

Near-infrared (IR) and Mid-infrared (MIR) detectors have exceeded the boundaries by marking their applications in numerous fields such as free space communications [1], satellite IR imaging [2], molecular absorption spectroscopy [3, 4], IR cameras, medical diagnostics, chemical identification, etc. Many studies focus on enhancing the semiconductors' optical absorption without compromising the device's speed. The direct band gap semiconductors from group III-V are extensively explored for numerous photonics applications [5, 6]. The development of controlled deposition processes such as molecular beam epitaxy [7], a quantum scale epitaxial mono-layer growth has been made possible, which has enabled us to exploit the quantum mechanical (QM) devices. Multi-quantum wells (MQWs) are one such device-level realization of the complex QM physics. In contrast to their bulk counterparts, the MQW-based photodetectors [8, 9] facilitate a band gap engineering mechanism and enable an efficient interband transition [10]. Such controlled electronics transitions and engineered bandgap equip us to design a photodetector for the desired wavelength range which could not be possible with its bulk counterparts. This chapter studied an optimized MQW type-II $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ by changing the dimensions and period for MIR wavelength (~1-3 μm) range sensitivity. InGaAs is used as a barrier layer and GaSb as a quantum well layer. It should be noted that, GaSb and GaAsSb were assumed to have the same (n, k) values, while the GaAsSb layer is referred as GaSb. The lattice constant of $In_{0.53}Ga_{0.47}As$ is 5.86 ˚A, and the lattice constant of $GaAs_{0.5}Sb_{0.5}$ is ~5.88 ˚A, which makes these two tertiary III-V compound semiconductors compatible for layer-by-layer epitaxial growth. Figure 11.1 presents a schematic of the electronic band diagram by cascading the bulk band structures of the $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5}$ stack, and elevated energy states (red and purple lines) due to the quantum confinement. The possible interband transitions

(green arrows) are enabled due to the cascading of the nanoscale layers of InGaAs and GaAsSb as can be seen in Fig. 11.1 (b) while the effective absorption coefficient profile for the InGaAs/GaAsSb MQW stack is shown in Fig. 11.1 (c).

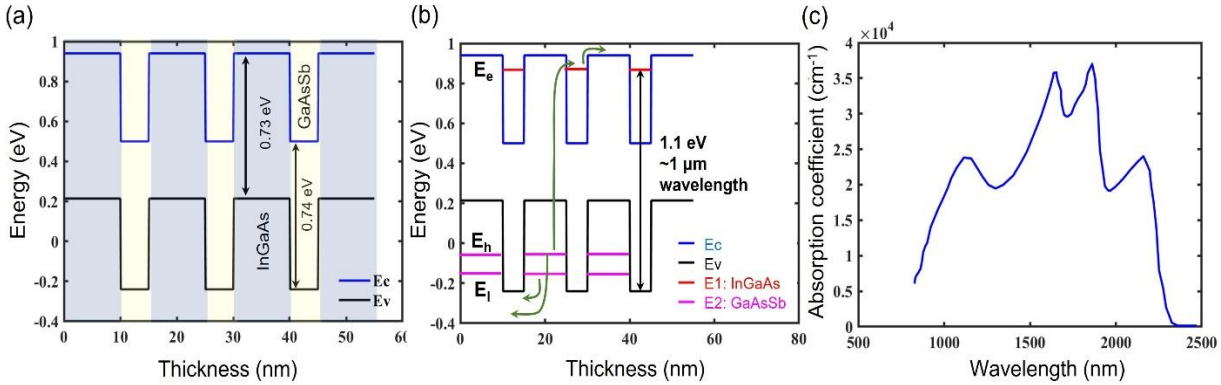


Fig. 11.1. Energy band diagram for InGaAs/GaAsSb MQW stack. (a) Conduction and valance band schematic for the MQW stack presenting the bulk band-gap for InGaAs and GaAsSb. (b) MQW imposed energy levels and possible interband electronic transitions enabled by the presence of MQWs. (c) Estimated theoretical absorption coefficient profile for InGaAs/GaSb MQW.

In this chapter, we aimed to design, simulate, fabricate and characterize a muti-quantum-well (MQW) infrared (IR) photodetector integrated with photon-trapping (PT) holes, sensitive to a range of 1.0 μm to 3.0 μm wavelength to enhance the device's external quantum efficiency (EQE). This study revealed that the embedding PT hole arrays not only enhance the optical absorption in IR ultra-thin structures but also can provide a method to reduce the material filling ratio to > 50%, which leads to a lower bulk dark current, ensuring lower-temperature operation of the IR detectors.

11.2 MQW PD optical simulation

Finite-difference time-domain (FDTD) optical simulation was used for MQW PD optimization. Specifically, GaSb/InGaAs, which is a type II MQW PD. Table 11.1 shows a couple of semiconductors' bandgaps and detection cutoff frequencies/wavelengths.

Semiconductor	BG (eV)	Wavelength (µm)
GaN	3.4000	0.3647
GaP	2.2600	0.5487
GaAs	1.4300	0.8671
InAs	0.4300	2.8837
InP	1.4200	0.8732
InGaAs	0.7500	1.6530
GaSb	0.8100	1.5309

Table 11.1. III-V Semiconducting materials and their energy bandgaps.

The desired PD detection is expected to have an optical sensitivity that ranges from 1 – 3 µm. Therefore, type II MQW stack constructed using GaSb/InGaAs which has multiple energy levels made available for an enhanced wavelength sensitivity range. A schematic of the band structure for GaSb/InGaAs type-II MQW is shown in Fig. 11.2.

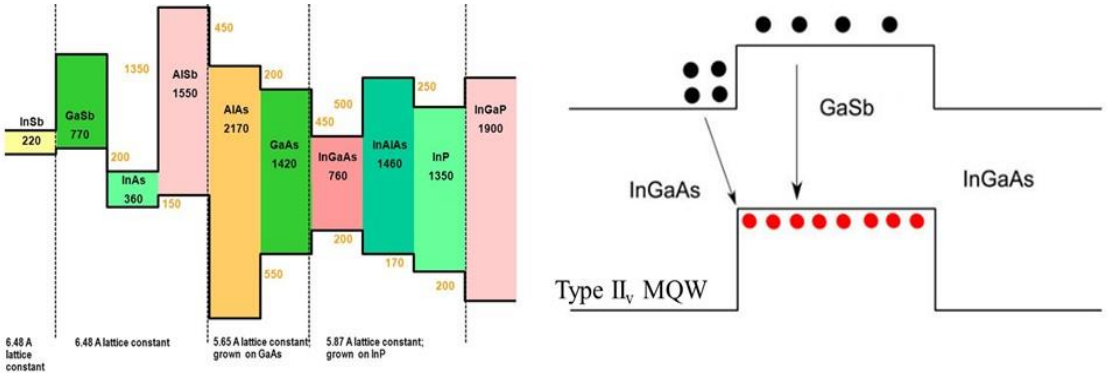


Fig. 11.2. Band diagram of GaSb/InGaAs based type II MQW.

A perfectly matched layer (PML) boundary condition was used in the z-direction and a periodic boundary condition in the x and y directions, and a plane wave source was used for the illumination with 1 W/m^2 power. The MQW stack layers were placed on a SiO_2 layer. The SiO_2 layer facilitates a semi-reflecting interface and reflects the illuminated light into the MQW stack and increases the optical power absorption due to the resonance. Next, 100 and 200 MQW stacked layers periods for a fixed well (GaSb-5nm) and barrier (InGaAs-5nm) width was simulated to examine the modulation in the optical absorption. Further, an introduction of a cylindrical

photon-trapping (PT) hole with a diameter of 1.4 µm, a period of 2 µm, and a depth of 1 µm was simulated to examine the optical enhancement in MQW PT PD. Following, a variation of the MQW and the barrier widths for a fixed period (100 MQW stacked layers) was simulated to examine the optical responsivity for different layer thickness combinations.

11.2.1 Impact of MQW period on optical absorption

The optical power absorption profile of the bulk-InGaAs and GaSb layers was simulated and is shown in Fig. 11.2 (a) as a reference. Figure 11.2 (b) presents the variation in optical response for a fixed well and the barrier widths of 5 nm and the period chosen to be 100 and 200 stack layers. By fixing the MQW dimensions we fixed the wavelength sensitivity range. However, we see an increase in the P with the increase in the period which is expected as we are increasing the thickness of the structure. The presence of the MQW and multiple reflections from the SiO_2 interface results in an enhancement in absorption.

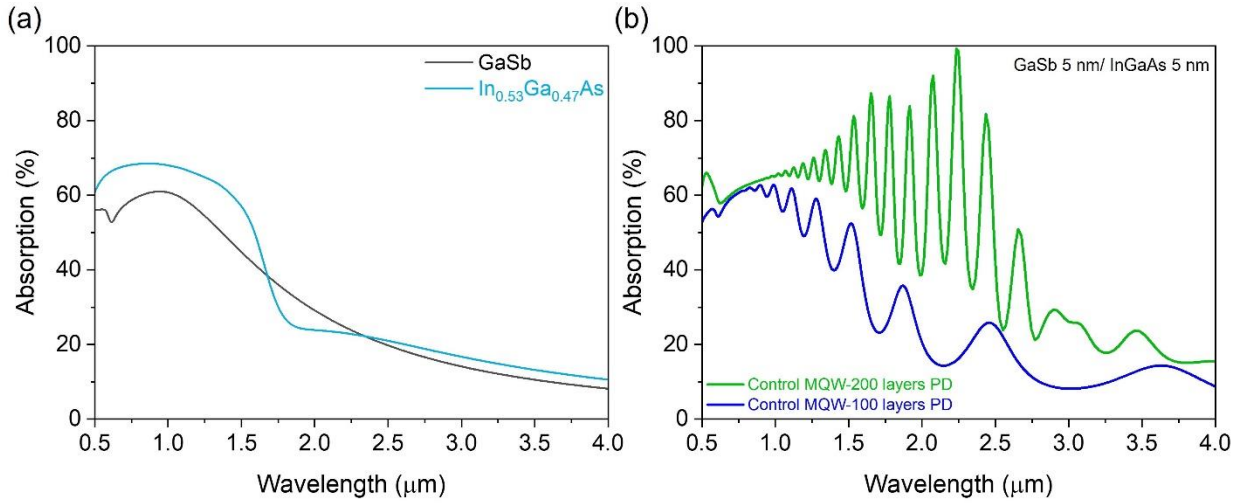


Fig. 11.2. Power absorption profile as a function of illumination wavelength. (a) Bulk-InGaAs and GaSb. (b) Fixed well dimension and varying MQW period.

11.2.2 Impact of MQW stacked layer thickness on optical performance

In this section, we fixed the period (stacked layers) of the MQW to be 200 and vary the well and the barrier dimensions (thicknesses) from 5 nm to 10 nm as can be seen in Fig. 11.3. The optical absorption is increased in the wavelength sensitivity range with increased well and barrier

thickness with longer wavelengths > 2.5 µm. Whereas MQW with thinner layers presents higher optical resonance and response as can be depicted in Fig. 11.3.

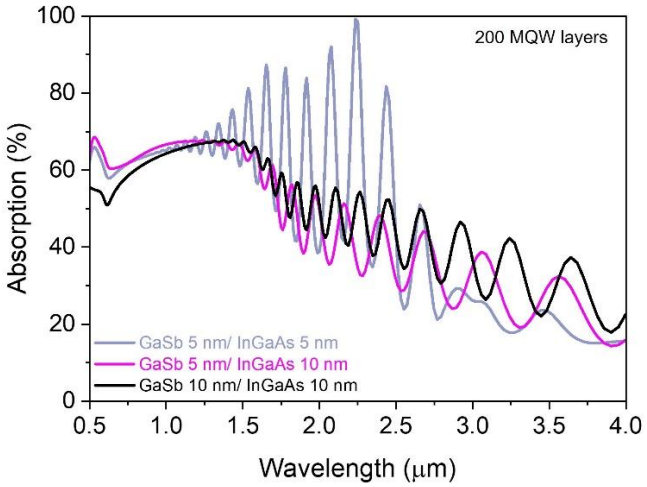


Fig. 11.3. Power absorption profile as a function of illumination wavelength for 200 MQW layers and a variation of MQW layers thicknesses.

11.2.3 Impact of photon-trapping holes on MQW PD

In this section, photon-trapping holes were integrated in the MQW PD design. The addition of the PT holes allows the optical illumination to bend in the lateral direction and results in an increased absorption for 100 MQW periods at a fixed MQW layer thickness of 5 nm (both well and the barrier) as can be seen in Fig. 11.4 (a). We observe a significant increase in absorption with the introduction of PT holes. However, we observe an increase in the optical absorption for 200 MQW periods at fixed MQW layer thicknesses of 5 nm, in the longer wavelength range as can be seen in Fig. 11.4. (b). Since 200 MQW is a thicker structure and shows high absorption profile, the PT holes impact is not predominant in the shorter wavelength.

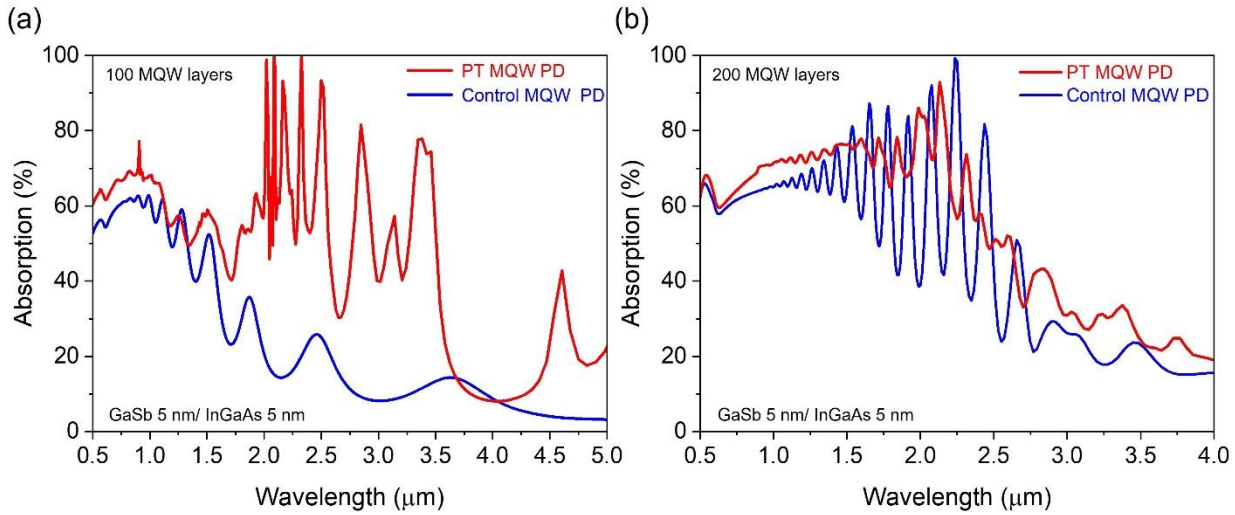


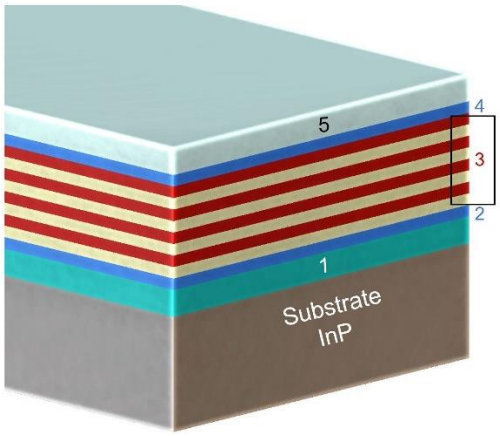
Fig. 11.4. Power absorption profile as a function of illumination wavelength comparing the impact of integrating photon-trapping hole structures for MQW (a) 100 MQW layers. (b) 200 MQW layers.

11.3 MQW PD Fabrication Process

11.3.1 MQW PD growth and structural design

The project aims to design and fabricate a muti-quantum-well (MQW) infrared (IR) photodiode, sensitive to a range of 1.0 μm to 3.0 μm wavelength. Therefore, the MQW PD structure was grown in a molecular beam epitaxy (MBE) system on InP substrate. The structural design is similar to the conventional top-illuminated pin photodetector. Firstly, a 500 nm thick InGaAs buffer layer was grown on an oxide-removed lattice matched InP substrate to provide a better growth surface for $In_{0.53}Ga_{0.47}As$ and a highly doped n-type layer to form the bottom contact laye with a doping concentration of $> 5\ x\ 10^{18} cm^{-3}$. Then, around 100 nm undoped layer of $In_{0.53}Ga_{0.47}As$ was grown. The MQW absorption layers consists of $In_{0.53}Ga_{0.47}As/GaAs_{0.5}Sb_{0.5\ 6}$ 6 nm/3 nm and repeated 160 times were epitaxially grown to form around 1.44 μm thin i-layer. This MQW structure is expected to provide a fast response operation for longer wavelength applications (1.0 μm to 3.0 μm). Next, around 100 nm undoped intermediate layer of $In_{0.53}Ga_{0.47}As$ was grown. Finally, the top contact layer (400 nm) of $In_{0.53}Ga_{0.47}As$ was epitaxially grown and heavily doped p-type to act as a top-contact layer $> 5\ x\ 10^{19} cm^{-3}$. The device structure and the specification can be seen in Fig. 11.5.

(a)



(b)

Layer	Description	Material	Thickness (nm)	Doping (cm^{-3})	type
5	Cap layer/top contact	InGaAs	400	>5e19	p
4		InGaAs	100	UID	
3	MQW 160 layers Layer= 9 nm	InGaAs/GaAsSb	1440	UID	i
	$In_{0.53}Ga_{0.47}As$ = 6 nm $GaAs_{0.5}Sb_{0.5}$ = 3 nm				
2		InGaAs	200	UID	
1	Buffer/ bottom contact	InGaAs	500	>5e18	n
Substrate		4" InP wafer	~ 600	2.5-3e19	n

Etched 2.27 µm

Fig. 11.5. Device's structural design. (a) Device schematic (top-illuminated). (b) Device's layers specification.

11.3.2 MQW PD fabrication

In this section, MQW wafer's cleaning process is discussed. Next, a devised process was developed to smoothly pattern and etch the photon-trapping holes. Subsequently, the top mesa was patterned and etched on the MQW stack and exposed the bottom n-type highly doped layer to enable robust metal contact. The bottom mesa was then defined and etched to isolate the devices. Next, top and bottom contacts pattern and deposition were developed using respective suitable metals. After the metallization, a conventional hot plate annealing was performed to form an ohmic contact. Then, polyimide planarization process was developed and followed by coplanar waveguides (CPWs) metal deposition. Finally, a passivation process was developed to reduce the dark current.

11.3.2.1 Wafer cleaning

The fabrication process started with conventional wafer cleaning. To clean the MQW wafers, three solvent-cyclic cleaning methods were used. At first, the wafer was sonicated in Acetone for 30 sec, followed by sonicating the sample in Methanol and Isopropyl alcohol for 30 sec each. Finally, the wafer was rinsed with de-ionized (DI) water and dried in N_2 flow.

11.3.2.2 Defining photon-trapping holes, top, and bottom mesas

Photolithography with S1813 positive photoresist (PPR) was utilized to perform photolithography. However, since the InP-to-PPR selectivity and the adhesion are poor. Therefore, SiO_2 layer was developed and deposited as a hard mask to define the photon-trapping holes, top, and bottom mesas.

11.3.2.3 SiO_2 deposition as a hard mask

To pattern the photon-trapping holes and subsequently the top mesa, SiO_2 was utilized as a hard mask. To enable SiO_2 based hard mask lithography, at first, a 1000 nm thick SiO_2 layer was deposited in high-density plasma chemical vapor deposition (HDPCVD) system. The SiO_2 layer was deposited in O_2, SiH_4, and Ar plasma struck at using 100 W RF_1 power and 600 W RF_2 power. The deposition is done at 180°C temperature for 7 min 52 seconds. The deposition process takes place in four steps. At first, a chamber cleaning process was performed in O_2 plasma for 10 min. A 6-inch dummy sapphire wafer was used during the chamber cleaning. Following the chamber cleaning, a chamber conditioning process was performed using the same dummy wafer for 2 min. During the chamber conditioning, the same gases were injected to be used for deposition (O_2, Ar, SiH_4 as per the flow rate listed in table 11.2) Finally, the main sample was loaded on a 6-inch carrier wafer into the chamber. Table 11.2 shows the flow rate of the gases and other process details used to deposit a 1000 nm thick SiO_2 layer. The obtained deposition rate is 127 nm/min, and as expected the measured thickness across the wafer is ~1000 nm as it was confirmed using the nanometric “Nanospec” reflectometer. The process was terminated by cleaning the chamber after the deposition. The final chamber cleaning is done using O_2 plasma in presence of sapphire wafer.

Process steps	O_2 (sccm)	Ar (sccm)	SiH_4 (sccm)	RF_1 (W)	RF_2 (W)	Temperature (°C)	Duration (min:sec)
O_2 clean	50	-	-	100	500	180	10
Conditioning	56	20	28	100	600	180	2
Deposition	56	20	28	100	600	180	7:52
O_2 clean	50	-	-	100	500	180	10

Table 11.2. Process parameter details used for SiO_2 deposition in HDPCVD system.

11.3.2.4 Top-mesa patterning

To pattern the top mesa and possibly photon-trapping holes, EVG mask aligner with S1813 positive photoresist (PPR), and a chromium-coated 7-inch mask plate were utilized. At first, the wafer was coated with S1813 PPR at 1500 RPM for 30 sec, followed by a 3 min prebaking to evaporate the solvent. This spin rate would result in a resist thickness of ~3.5 *μm.* After spin casting the sample was loaded in the EVG system for ultra-violate light exposure, followed by pattern development in for 40 sec in MF 319 solution. A post-baking of the wafer was performed to make the resist hard and robust to sustain the high-voltage RIE plasma. After the post-baking, the SiO_2 hard mask was etched using the PPR as the mask. The etching was done in an inductively coupled plasma reactive ion etching (ICPRIE) system. The SiO_2 etching process involves four process steps. It starts with chamber cleaning in O_2 plasma. Followed by the chamber conditioning process. After the chamber conditioning, the sample was loaded on a 6-inch carrier wafer, and the system injected CHF_3 and CF_4 gases with a respective flow rate of 10 sccm and 30 sccm, while the plasma set at 50 W RF and 500 W ICP power. The process details are listed in table 11.3. The estimated SiO_2 etch rate is 152.43 nm/min and the selectivity of SiO_2 against the PPR is 5.6:1. Using the patterned SiO_2 as a hard mask, PT holes and top mesa were etched using the ICPRIE etching. The MQW etch process parameters are listed in table 11.4.

Process steps	O_2 (sccm)	CHF_3 (sccm)	CF_4 (sccm)	RF (W)	ICP (W)	Duration (min:sec)
O_2 clean	50	-	-	100	500	15
Conditioning	-	10	30	50	500	2
Etching	-	10	30	50	500	6:34
O_2 clean	50	-	-	100	500	15

Table 11.3. SiO_2 dry etch process parameters.

A profilometer measurement was utilized to estimate the selectivity of the MQW etch rate against SiO_2. In order to do so, the measured SiO_2 thickness was around 980 nm. The thickness of the SiO_2 is measured using a profilometer after the SiO_2 etch. In addition, the depth of SiO_2 with MQW stack was measured using a profilometer after the etching. Finally, the MQW etched depth was measured after removing the SiO_2 layer. The estimated MQW etch rate is 732.25 nm/min. The selectivity of MQW against the SiO_2 hard mask is 4.5:1.

Process steps	O_2 (sccm)	CHF_3 (sccm)	CF_4 (sccm)	RF (W)	ICP (W)	Duration (min:sec)
O_2 clean	50	-	-	100	500	15
Conditioning	-	10	30	50	500	2
Etching	-	10	30	50	500	6:34
O_2 clean	50	-	-	100	500	15

Table 11.4. MQW dry etch process parameters.

The MQW etch process was repeated with a reduced etch duration (4 min) to reach the desired depth to the bottom contact n-type layer as demonstrated in Fig. 11.5 (b). The measured top mesa depth is measured using a profilometer measurement and found to be 2.27 μm as can be seen in Fig. 11.6. The same process was used to pattern and etch the bottom mesa for devices isolation purposes.

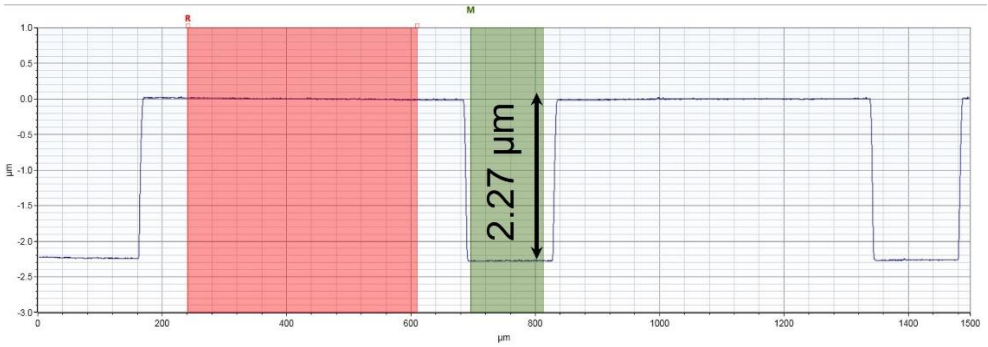


Fig. 11.6. The MQW top mesa etch and profilometer mesa depth measurement.

11.3.2.5 Metallization

11.3.2.5.1 Top contact metallization

To pattern the top contact (p-type contact), Pt/Ti/Ni/MQW stack was used. The top contact is patterned using S1813 PPR and UV lithography in alignment with the top mesa. After the patterning, the sample was loaded into an E-beam evaporator chamber. After the desired vacuum is achieved, 10 nm Ni, 10 nm Ti, and 100 nm Pt were deposited in the respective order. During the Pt deposition, the PPR gets hard and becomes hard to remove. To dissolve the hardened PPR, PRS 3000 solution was used. The PRS 3000 was heated at 80°C and the Pt-coated samples were kept in the solution for 10 min. Followed by sonication for 30 sec, rinsing and drying processes. The samples before and after the PRS 3000 cleaning are shown in Fig. 11.7.

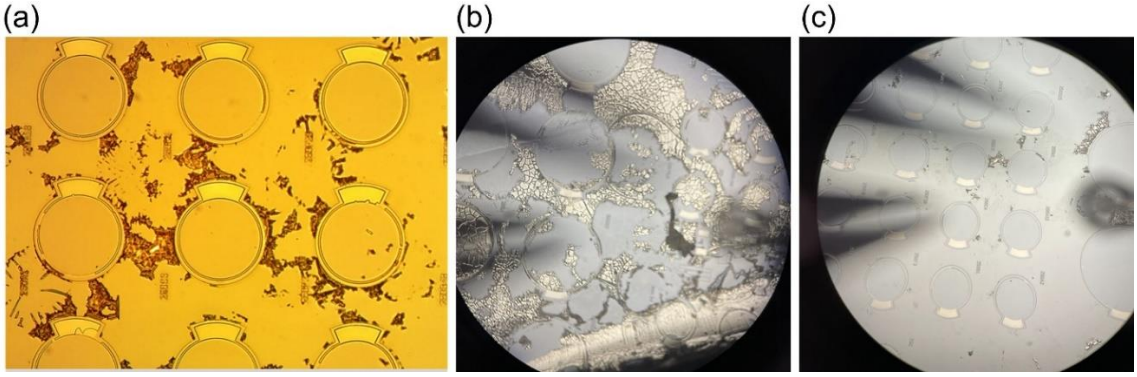


Fig. 11.7. Microscopic images of the sample (a-b) before and (c) after the PRS 3000 solution cleaning

11.3.2.5.2 Bottom contact metallization

To pattern the bottom contact (n-type contact), Au/Ge/n-InP stack was used. After the PRS 3000 cleaning, the bottom contact was patterned using PPR and UV lithography. After the pattern

development, the sample was loaded into an E-beam evaporator system. A deposition of 10 nm Ge followed by 100 nm Au was performed. After the deposition, a standard lift-off process in Acetone for 10 min was done. After the metallization, a hot plate annealing process was completed at 450°C for 30 min under N_2 laminar flow. Top and bottom metal contacts on the fabricated devices is shown in Fig. 11.8.

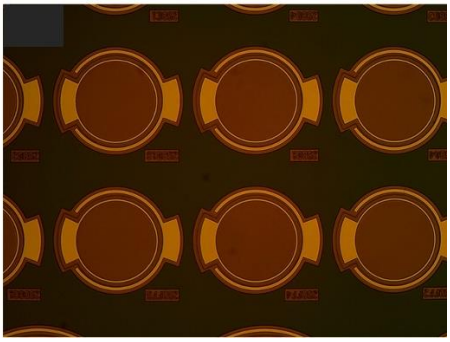


Fig. 11.8. Top and bottom metal contact after the Al evaporation and lift-off.

The complete fabrication process is depicted in Fig. 11.9. It should be noted that, planar complete devices are fabricated at first hand. Subsequently, photon-trapping devices will be fabricated and characterized.

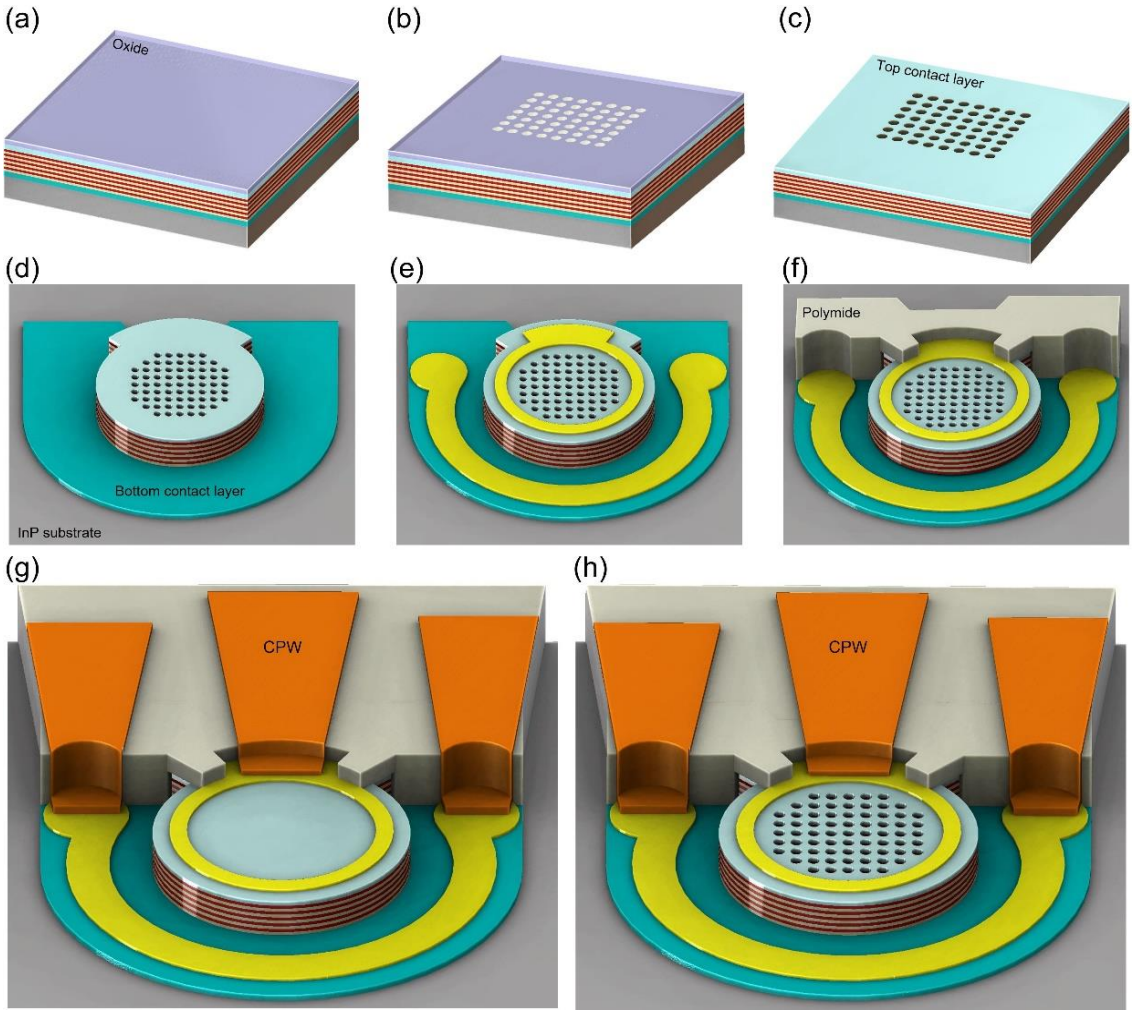


Fig. 11.9. Schematic diagram of fabricating the photon trapping PDs. (a) Starting wafer coated with SiO_2. (b) DUV photolithography and holes etch to create PT holes in SiO_2. (c) ICP/RIE holes etch in MQW. (d) Top mesa and bottom mesa defining and etching. (e) Ohmic metal deposition, top contact (10 nm Ni, 10 nm Ti, and 100 nm Pt), and bottom contact (10 nm Ge and 100 nm Au) followed by surface passivation. (f) PECVD deposition to isolate the n and p mesas and polyimide planarization. (g) Coplanar waveguides (CPWs) metal deposition (brown color) for control MQW PD and (h) for PT MQW PD.

11.4 Electrical Characteristics

A DC IV measurement was performed on the fabricated control MQW devices using a b1500 analyzer interfaced with EasyExpert and illuminated the devices using an NKT photonics—supercontinuum laser. The available laser system allowed to characterize the fabricated devices up to 1800 nm wavelength. The devices were biased with 1 to -4 V DC voltage and captured the dark and illuminated IV profile for wavelength range varying from 1200-1800 nm. The captured IV

profile is shown in Fig. 11.9 (a). The external quantum efficiency (EQE) was calculated using Equation 11.1:

$$EQE = \frac{1240}{\lambda} \times \frac{I - I_{dark}}{Power} \times 100 \quad (11.1)$$

The measured EQE is plotted in Fig. 11.10 (b).

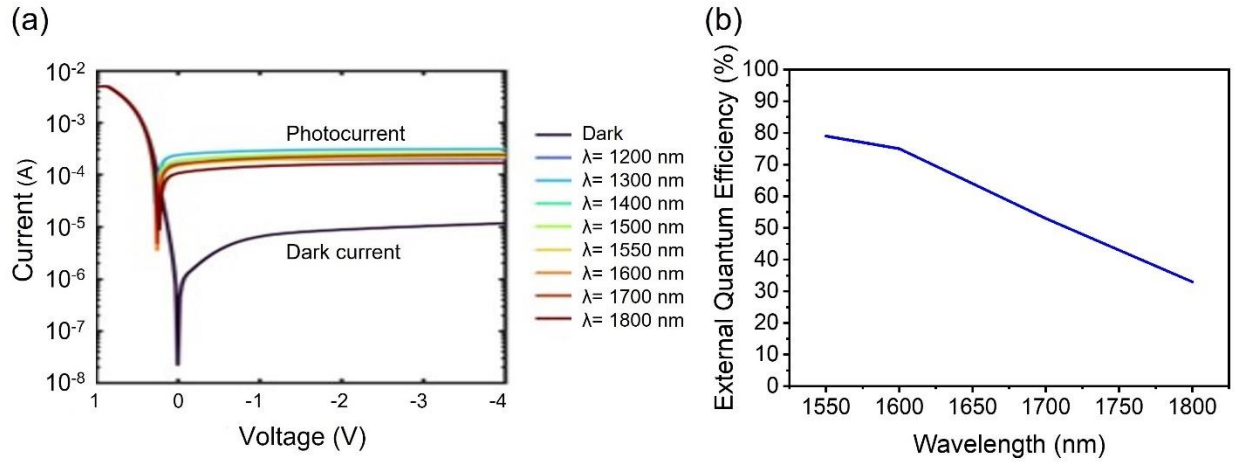


Fig. 11.10. Current-voltage characteristics of the fabricated control MQWs PDs. (a) Dark current vs. photocurrent for NIR illuminations. (b) MQWs PD's EQE responses for NIR illuminations.

The fabricated control MQW PDs shows a good response according to the thickness of the MQWs structures for NIR optical spectrum such as 1600 nm to 1800 nm. Next step would be designing optimizing, and fabricating photon-trapping MQWs PD, and comparing their performances with the fabricated control MQWs PDs. Then, surface passivation process will be developed and cpw (RF) ultra-fast characterization will be carried out to examine and study the control and PT MQWs PDs performances.

11.5 Photon-trapping MQWs PDs optical mask designs

Optical absorption enhancement was confirmed in PT MQWs PD by running many FDTD optical simulations. Additionally, photon-trapping patterns, dimensions, structures profile and periodicity are optimized, and subsequently optical mask is designed accordingly. Figure 11.11. shows optical mask design with photon trapping designs such as spiral design (a), aperiodic photon-trapping (b,c), square and hexagonal into one PD (d,e), and hexagonal unit cell design (f). MQW

PT PDs designs include structures that target NIR spectrum between 1-3 μm that operate at ultra-fast performance.

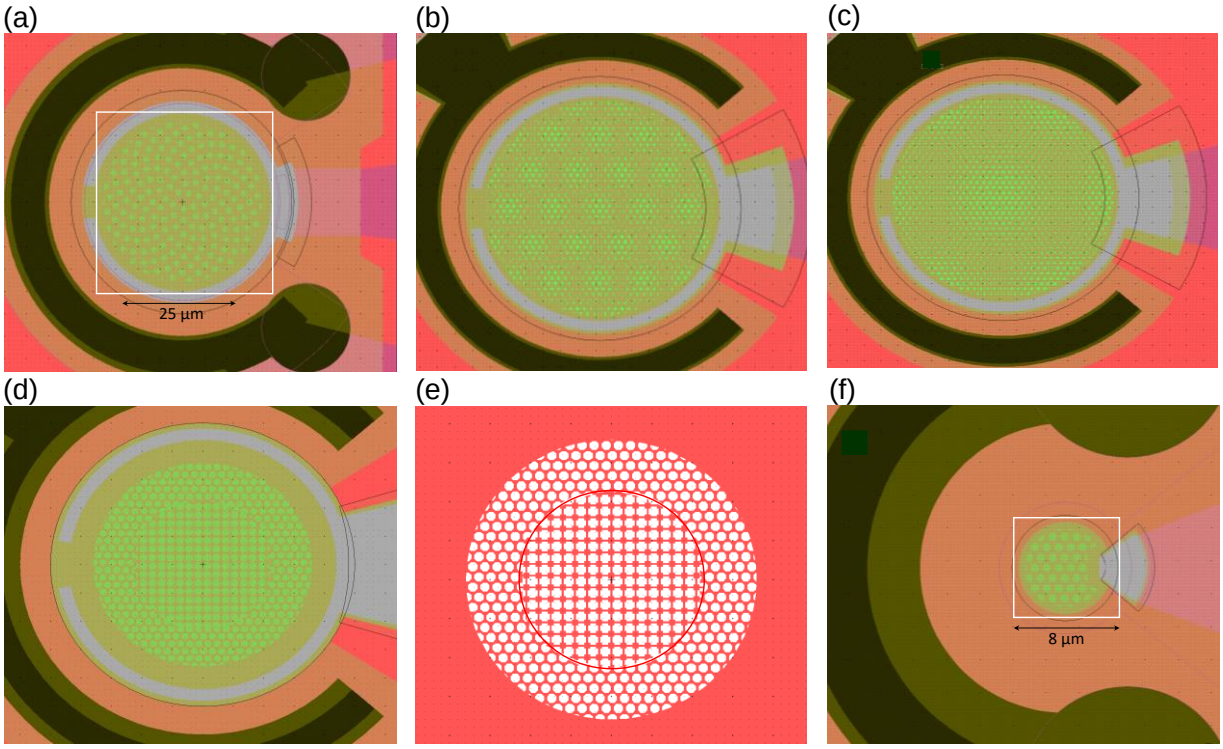


Fig. 11.11. Optical mask designs for photon-trapping MQWs PDs. (a) spiral photon-trapping design. (b,c) photon-trapping aperiodic design. (d,e) Inner square pattern, and outer hexagonal pattern PD. (f) hexagonal pattern design in 8 um PD.

Hence, many designs are incorporated with pattern's holes diameter ranging between 800 nm – 3000 nm, while the pattern periodicity ranging between 1000 nm- 3500 nm. Square, hexagonal, spiral, and aperiodic photon-trapping design optical mask are developed and designed for examining and studying their performances. Devices diameters are ranging between 50 μm down to 8 μm. Small diameter devices such as 12-8 μm can be utilized for ultra-fast optical operation. Figure 11.12 shows the layout of the designed optical mask for MQW photon-trapping photodetectors.

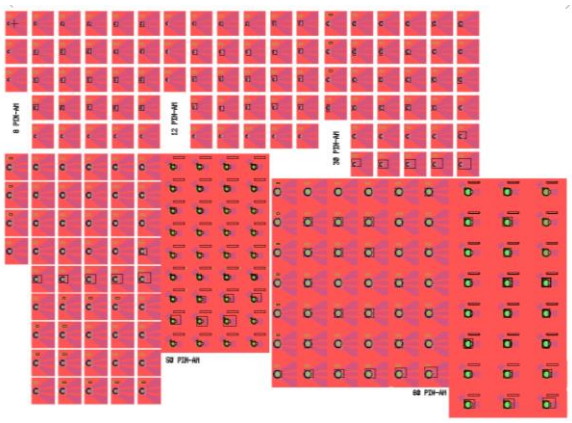


Fig. 11.12. Complete optical mask layout for photon-trapping MQWs PDs. Devices diameter ranges between 100 µm-8 µm with a variation of photon-trapping designs.

Once the optical mask gets printed, we expect to complete fabrication of photon-trapping MQWs PD will be fabricated, passivated, and characterized and the results will be reported in subsequent manuscript.

References

[1] S. Pirotta *et al.*, "Fast amplitude modulation up to 1.5 GHz of mid-IR free-space beams at room-temperature," *Nature communications,* vol. 12, no. 1, pp. 1-6, 2021.

[2] P. Sutton, D. Roberts, C. Elvidge, and H. Meij, "A Comparison of Nighttime Satellite Imagery," *Photogrammetric Engineering & Remote Sensing,* vol. 63, no. 11, pp. 1303-1313, 1997.

[3] I. Amenabar *et al.*, "Structural analysis and mapping of individual protein complexes by infrared nanospectroscopy," *Nature communications,* vol. 4, no. 1, pp. 1-9, 2013.

[4] L. Bellamy, *The infra-red spectra of complex molecules*. Springer Science & Business Media, 2013.

[5] J. B. Soole and H. Schumacher, "InGaAs metal-semiconductor-metal photodetectors for long wavelength optical communications," *IEEE journal of quantum electronics,* vol. 27, no. 3, pp. 737-752, 1991.

[6] R. LaPierre, M. Robson, K. Azizur-Rahman, and P. Kuyanov, "A review of III–V nanowire infrared photodetectors and sensors," *Journal of Physics D: Applied Physics,* vol. 50, no. 12, p. 123001, 2017.

[7] W. P. McCray, "MBE deserves a place in the history books," *Nature nanotechnology,* vol. 2, no. 5, pp. 259-261, 2007.

[8] J.-Y. Yeh *et al.*, "Characteristics of InGaAsN-GaAsSb type-II “W” quantum wells," *Journal of crystal growth,* vol. 287, no. 2, pp. 615-619, 2006.

[9] J. Huang *et al.*, "Design and characterization of strained InGaAs/GaAsSb type-II ‘W’quantum wells on InP substrates for mid-IR emission," *Journal of Physics D: Applied Physics,* vol. 42, no. 2, p. 025108, 2008.

[10] M. Fox and R. Ispasoiu, "Quantum wells, superlattices, and band-gap engineering," *Springer Handbook of Electronic and Photonic Materials,* pp. 1-1, 2017.

Chapter 12 Photon-trapping in ultra-thin PD for high-performance IR detection

12.1 PbSe and HgCdTe PDs for high-performance IR detection

The performance of mid- and long-wavelength infrared (IR) detectors is still restricted with the dark current characteristics and associated noise behavior [1, 2]. In this chapter, dark current and related noise of the IR detectors to elevate high operating temperature reduction and the detectors' external quantum efficiency (EQE) enhancement is studied by utilizing a thin absorption layer of materials like lead selenide (PbSe) and mercury cadmium telluride (HgCdTe) [3, 4]. A photon bending and trapping mechanism based on integrated micro/nanoscale holes was employed to ensure high quantum efficiency despite of a thin absorbing layer. Using the finite-difference time-domain (FDTD) method [5], the effect of embedded hole arrays on the optical absorption enhancement of ultra-thin PbSe and HgCdTe has been investigated. The calculated optical absorptions in ultra-thin IR structures without holes were compared with that of similar structures embedded with hole arrays. The optical absorption in 2μm thin PbSe film without holes is less than 5% in the range of 3-5 μm, mid-IR wavelengths. Although applying conventional anti-reflecting (AR) coatings leads to a slightly higher absorption, it can cause higher dark current due to increased surface traps. Integration of hole arrays in 2μm thin PbSe film has shown a significant optical absorption enhancement, up to 20% at 4.5 μm wavelength. This is equivalent to more than 2- and 4- folds enhancement compares to 2 μm thin control (planar-surface structure) with AR and without AR, respectively. In addition, embedding the hole arrays in 1.2 μm thick HgCdTe IR films enhances the optical absorption up to 75% at 4.5 μm, which is more than 4 times higher than that in HgCdTe film without holes. Additionally, the optical absorption in 1.2 μm thick HgCdTe film with a periodic array of photon-trapping micro-holes enhances to 27% at 10 μm long-IR wavelength. This is more than 3 times higher than that in HgCdTe film without holes. This study revealed that the embedding hole arrays not only enhance the optical absorption in IR ultra-thin

structures but also can provide a method to reduce the material filling ratio to > 50%, which leads to a lower dark current, ensuring the temperature operation of the IR detectors[6].

12.2 Optical simulation

FDTD simulations was used to study the micro-holes array and to find the optical coupling with normal incident light. Using a short pulse Gaussian profile-plane wave and applying periodic boundary conditions in x and y directions, it was found that each hole in the array can couple light into the parallel-to-the-interface modes. Subsequently, the effect of the micro-holes array and coupling the parallel optical light to the interface into the guided resonant modes (the leaky modes) theoretically was calculated and analyzed. An enhanced optical absorption was observed due to the longer photons-matter interaction. The optimization of hole parameters was done based on theoretical calculation.

12.3 PbSe photon-trapping PD

12.3.1 Modeling PbSe PD with photon-trapping holes (1-2 μm thicknesses)

PbSe is used for designing infrared (IR) detectors for thermal imaging, operating at wavelengths between 1.5–5.2 μm. This material does not require cooling but performs better at lower temperatures. The peak sensitivity depends on temperature and varies between 3.7–4.7 μm and offers a fast response. PbSe and the polycrystalline nature of active thin film play a key role in both the reduction of the Auger mechanism and the reduction of the dark current associated with integrated multiple inter-grain depletion regions and potential barriers inside the polycrystalline thin films [3].

The photodetector consists of an array of holes of a depth d_h = 1μm and 2μm in PbSe film, as shown in fig. 12.1. The absorption efficiency for both 1μm and 2μm thin control PD, PT PD compared with and without anti-reflection (AR) coating are in fig. 12.1 (a). The simulations were done for the cylindrical hole with a diameter of d=3.2μm placed as arrays with period p=4μm. The perfect matched layer (PML) boundary conditions were used in the z-direction, normal to the

detector surface. Incident light is a plane wave in the z-direction. In the x and y directions (lateral directions), the periodic boundary conditions were applied. Absorption was calculated by subtracting reflected (R) and transmitted (T) energy from incident energy and normalizing by incident energy. The simulations were done for 2µm to 6µm mid-IR wavelength. The results showed that there is a noticeable increase in optical absorption for the PT PD compared to the control or AR-coated control PD. The light leaks from the holes into PbSe and has a much longer path compared with the flat PbSe slabs of the same thickness where the vertically incident light has a path only through the slabs.

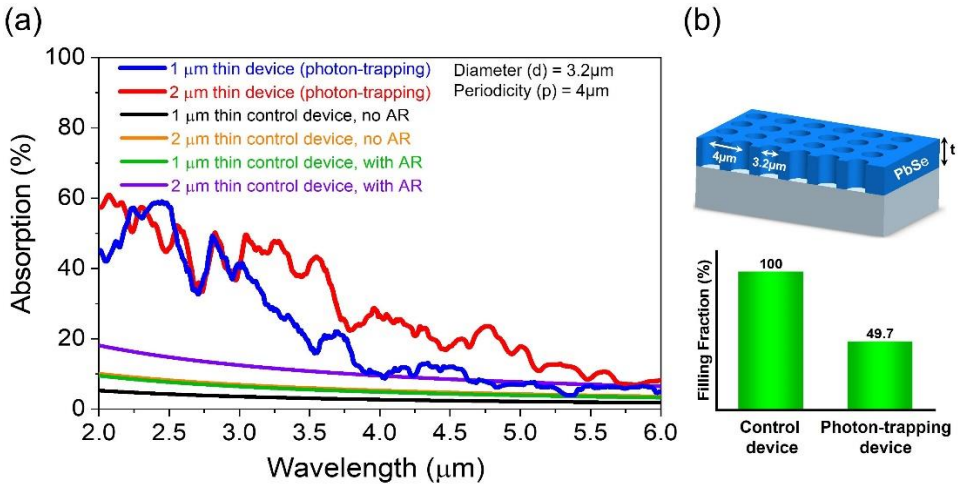


Fig. 12.1. Enhanced optical absorption enabled by PT PbSe with 1µm and 2µm thicknesses of absorbing materials. (a) Numerical simulation of the absorptance versus wavelengths for the mid-IR (2-6 µm) in PT PD vs. control PD (with and W/O AR coating). (b) Device filling ratio in the structures with PT holes and without hole arrays.

12.3.2 Modeling PbSe PD with photon-trapping holes (holes depth variation)

Figure 12.2 shows optical responses with varying depth of the etched holes. It can be noted that, PT with holes depth ~1.5µm and 1.9µm offer better absorption for wide spectral ranges. The absorption was about 20% for the structures with micro-holes compared to 2% for the structure without holes at 4.5µm. The optical unique response also revealed that, photon-trapping structures have the ability to be designed specifically for a targeted application wavelengths and could be efficiently optimized.

As presented studies and results showed in earlier chapters, periodic arrays exhibit enhanced absorption in semiconductor thin films [7-12]. Although some enhancement can be explained based on the fact that the disorder in photonic crystal destroys band gaps, the FDTD simulations showed that there is a significant enhancement in the wide wavelength range for the arrays without band gaps as FDTD simulations confirmed the lateral modes in the array.

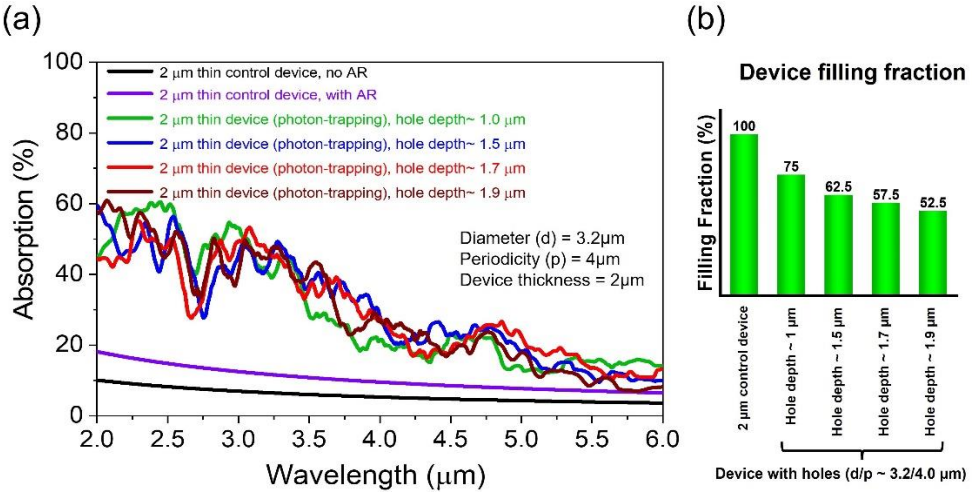


Fig. 12.2. FDTD optical enhancement in PT PbSe vs. PT holes depth. (a) Numerical simulation of the absorptance versus wavelengths for the mid-wave infrared, a unique response showing the impact of PT holes depth variation. (b) Material filling ratio in the structures with hole and without hole arrays.

12.3.3 Modeling PbSe PD with photon-trapping holes (funnel and inverted conical frustum geometries)

Unique optical responses can be obtained through designing a variation of photon-trapping geometries in addition to the PT diameter, depth, pattern units and periodicity. Hence, optical response in thin Mid-IR PDs can be maximized by employing such photon-trapping holes. Figure 12.3 shows the optical response of a variety of PT holes profiles (sidewall). PD thickness was designed to be around 2μm, holes dimeter 4 μm, holes depth 1.5 μm and tapered hole's angle 54°. As can be seen in Fig. 12.3 (a), the optical response peaks shift according to the specific PT design. Additionally, all designs showed a broadband optical enhancement and higher absorption than the control PbSe (no holes). Figure 12.3 (b) shows the cross-sectional schematic of the inverted conical frustum and funnel-shaped photon-trapping profiles.

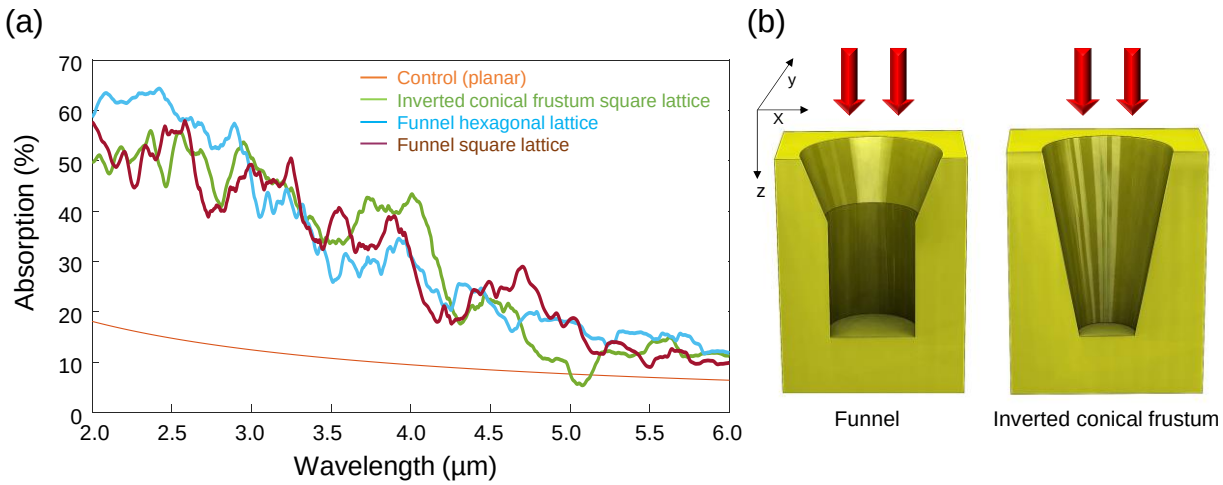


Fig. 12.3. FDTD optical simulation for different photon-trapping profiles. (a) Optical response of different holes pattern geometries in PbSe PT PD (λ =2-6 μm). (b) Cross-sectional schematic of PT geometries.

12.4 HgCdTe photon-trapping PD

HgCdTe can detect infrared radiation in the atmospheric windows including 3 to 5 μm Mid-Wave IR (MWIR) and from 8 to 12 μm Long-Wave IR (LWIR). It is the most important material for infrared photodetectors. Different combinations of its alloy work over a wide spectral range, including the Short-Wave IR (SWIR: 1–3 μm), Mid-Wave IR (MWIR: 3–5 μm), Long-Wave IR (LWIR: 8–14 μm), and Very-Long-wave IR (VLWIR: 14–30 μm) bands. Despite its superior performance, such as high detectivity, high quantum efficiency, and relatively fast response time, HgCdTe IR detectors are expensive because they need low operating temperature. By reducing the leakage current, the operating temperature can be increased considerably. Photon-trapping approach of integrating holes contributes to reduced leakage current by reducing the bulk dark current.

12.4.1 Modeling HgCdTe PD with photon-trapping holes for Mid-Wave IR (MWIR)

Optical simulations show that the lateral modes in a thin film of HgCdTe with integrated holes can enhance absorption in the photodiodes and improve the EQE of the photodiodes, allowing a relatively thin i-layer to absorb the incoming photons efficiently. The cylindrical micromoles were optimized based on the modal analysis. As can be depicted in Fig. 12.4, PT cylindrical holes PD

with a size comparable to the wavelength provided higher absorption than the control PD (planar). Simulations were done for the cylindrical hole with a diameter of d=3.6 µm placed as arrays with period p=5.0 µm arranged in the square lattice. The wavelength window of interest in this simulation was 3.5 µm to 7 µm. The absorption was observed to increase to around 65% for the structure with micro-holes compared to 17% for the structure without holes at the wavelength of 4.5 µm. Additionally, an optical absorption enhancement to around 60% for the PT HgCdTe compares to 2.7% for the control HgCdTe at the wavelength of 5.25 µm.

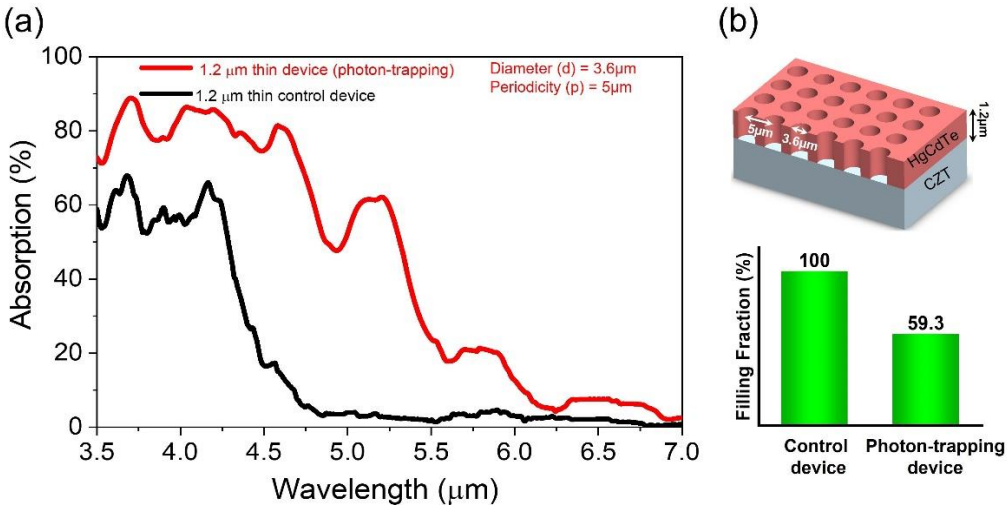


Fig. 12.4. Enhanced absorption enabled by integrated PT holes in HgCdTe infrared for MWIR. (a) Calculated optical absorption in 1.2 µm thin HgCdTe for PT holes vs. thin HgCdTe for control (planar). (b) Schematic of device with cylindrical micromole arrays, diameter/period (d/p) of 3.6 µm/5.0 µm, a comparison between material filling ratio in the structures with hole and without hole arrays.

12.4.2 Modeling HgCdTe PD with photon-trapping holes for Long-Wave IR (LWIR)

In this section, a set of simulations were done for the cylindrical hole with a diameter of d=6.5 µm placed as arrays with period p=8 µm and another structure with d=7 µm and p=9 µm arranged in square lattice and the wavelength of interest for this simulation was 8 µm to 13 µm as can be seen in Fig. 12.5. The optical absorption responses for the simulated structures are varying according to the incident wavelength, specially between λ= 8-10 µm. The absorption was about 30% and 58% for the structure with hole sizes of d/p~6.5/8.0 µm and d/p~7.0/9.0 µm, respectively, compared to 10% for the structure without holes at 10 µm. The results indicate that, optical

response in thin LWIR HgCdTe IR photodetector with holes can be maximized by optimizing the hole size, period, and pattern geometry. It should be noted that, both PT designs revealed a higher optical absorption than control HgCdTe PD.

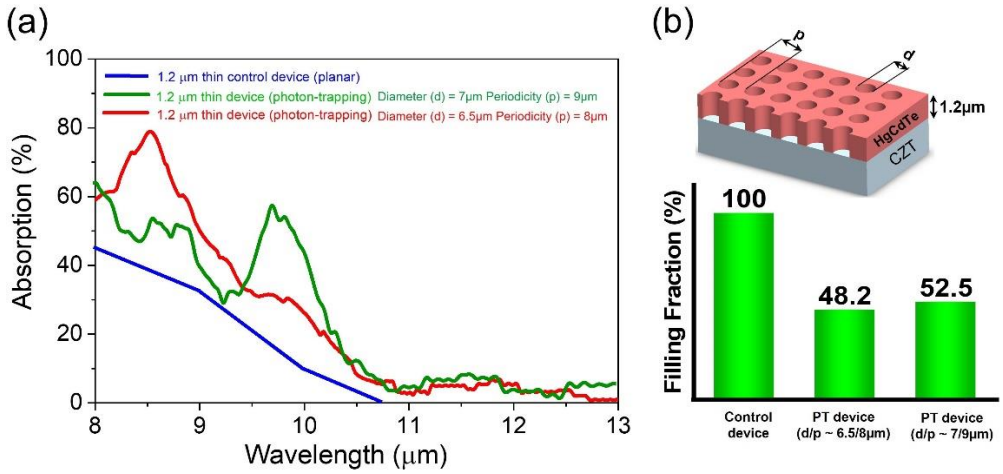


Fig. 12.5. Comparison of different PT designs thin HgCdTe PD vs. incident wavelengths. (a) FDTD optical enhancement for different PT designs. (b) A comparison between HgCdTe filling ratio in the structures with hole and without hole arrays

12.4.3 Modeling HgCdTe PD with dielectric filled photon-trapping holes for Long-Wave IR (LWIR)

A set of simulations were done for the cylindrical hole with a diameter of d=6.5 μm placed as arrays with period p=8 μm arranged in square lattice and the wavelength of interest for this simulation was 8μm to 13 μm, as can be seen in Fig. 12.6. The absorption was found to increase to 30% for the structure with unfilled (air) holes and 42% for the structure with filled holes (filled with dielectric, n=1.5) compared to 10% for the control PD (planar) at the wavelength of 10 μm. Dielectric filled holes can provide an additional parameter to design photon-trapping PDs to induce a uniqueness and enhanced optical response. It is also obvious from Fig. 12.5 (b) that the embedding of hole arrays reduces the material filling ratio to ~ 50% in IR ultrathin HgCdTe structures, which leads to a much lower dark current, therefore, elevating the operation temperature of the IR detectors.

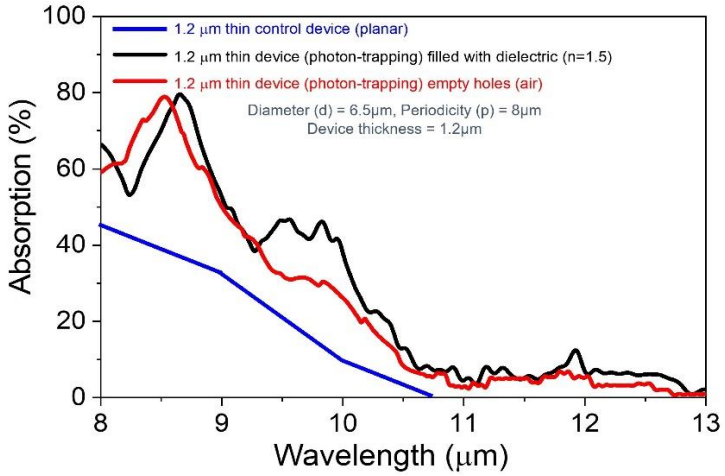


Fig. 12.6. Optical absorption for PT holes filled with dielectric (n=1.5) vs. PT empty holes (air)

12.4.4 HgCdTe Photon-trapping holes etching process.

Since high-density plasma etching process is preferred for the etching process in HgCdTe [13], inductively coupled plasma etching (ICP RIE) was used to etch anisotropic holes profile in HgCdTe. The etching mechanism was used as commonly used plasma gases with a variation of different ratios of $CH_4/H_2/Ar/N_2$ for etching HgCdTe. The pressure during the etching process was set to 10 mTorr and the gas mixture during the etching process contains CH_4:H_2:Ar ~ 200:80:30 sccm. The ICP power was set to 1000 W, and the RF power was set to 300 W. It is recommended to use a hard mask such as SiO_2 since it has a high etching selectivity with HgCdTe [13, 14]. As can be seen in Fig. 12.7, SEM images show a photon-trapping holes etched in HgCdTe with a depth of ~ 300 nm. The photon-trapping holes diameter is ~5 μm with periodicity ~8 μm.

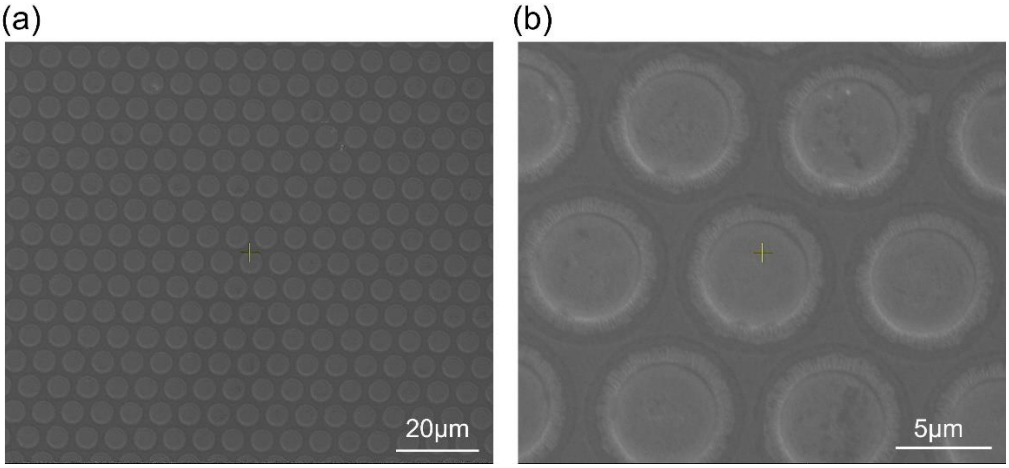


Fig. 12.7. SEM of photon-trapping holes in HgCdTe. (a) PT holes array. (b) zoomed image of a hexagonal PT unit cell.

References

[1] A. Rogalski, "Recent progress in infrared detector technologies," *Infrared Physics & Technology,* vol. 54, no. 3, pp. 136-154, 2011.

[2] A. Rogalski, J. Antoszewski, and L. Faraone, "Third-generation infrared photodetector arrays," *Journal of applied physics,* vol. 105, no. 9, p. 4, 2009.

[3] A. Munoz *et al.*, "PbSe photodetector arrays for IR sensors," *Thin Solid Films,* vol. 317, no. 1-2, pp. 425-428, 1998.

[4] C. L. Tan and H. Mohseni, "Emerging technologies for high performance infrared detectors," *Nanophotonics,* vol. 7, no. 1, pp. 169-197, 2018.

[5] L. Inc, "The Finite-Difference Time-Domain (FDTD): 3D Electromagnetic Simulator," ed.

[6] J. A. Montoya, Z.-B. Tian, S. Krishna, and W. J. Padilla, "Ultra-thin infrared metamaterial detector for multicolor imaging applications," *Optics express,* vol. 25, no. 19, pp. 23343-23355, 2017.

[7] C. Bartolo-Perez *et al.*, "Maximizing Absorption in Photon-Trapping Ultrafast Silicon Photodetectors," *Advanced Photonics Research,* vol. 2, no. 6, p. 2000190, 2021.

[8] H. Cansizoglu *et al.*, "Dramatically enhanced efficiency in ultra-fast silicon MSM photodiodes via light trapping structures," *IEEE Photonics Technology Letters,* vol. 31, no. 20, pp. 1619-1622, 2019.

[9] Y. Gao *et al.*, "High speed surface illuminated Si photodiode using microstructured holes for absorption enhancements at 900–1000 nm wavelength," *ACS Photonics,* vol. 4, no. 8, pp. 2053-2060, 2017.

[10] S. Ghandiparsi *et al.*, "Up to 1700nm broadband high-efficiency surface-illuminated Ge/Si photodiode with microhole array," in *Integrated Photonics Research, Silicon and Nanophotonics*, 2019: Optica Publishing Group, p. IT3A. 3.

[11] S. Ghandiparsi *et al.*, "High-speed high-efficiency photon-trapping broadband silicon PIN photodiodes for short-reach optical interconnects in data centers," *Journal of Lightwave Technology,* vol. 37, no. 23, pp. 5748-5755, 2019.

[12] A. S. Mayet *et al.*, "Surface passivation of silicon photonic devices with high surface-to-volume-ratio nanostructures," *JOSA B,* vol. 35, no. 5, pp. 1059-1065, 2018.

[13] L. Liu, Y. Chen, Z. Ye, and R. Ding, "A review on plasma-etch-process induced damage of HgCdTe," *Infrared Physics & Technology,* vol. 90, pp. 175-185, 2018.

[14] Y. Chen *et al.*, "Dry etched SiO2 Mask for HgCdTe Etching Process," *Journal of Electronic Materials,* vol. 45, no. 9, pp. 4705-4710, 2016.

Chapter 13 Conclusion and future work

This chapter discusses the conclusion of this dissertation and provides some future research opportunities.

13.1 Summary

This project aims to investigate and develop photon-trapping nanostructure designs to enhance the optical efficiency and speed characteristics of a variation of photodetectors that can operate in the visible and near-infrared spectrum. During this journey, we have designed, simulated, fabricated, and characterized many photodetectors to study and analyze their performances. In addition, we studied photon-trapping nanostructures theory and analyzed it further in working photodetectors and photovoltaics devices.

Optical communication, imaging, and sensing applications are rapidly growing in data centers, free space optical communication (FSO), quantum communication, CMOS imaging sensors, spectroscopy, biomedical imaging, and emerging applications.

Highly sensitive and ultrafast photodetectors and CMOS compatibility on a silicon platform are critical for cost-effective and widely adopted emerging applications in quantum computing, biomedical imaging, biosensing, security, surveillance, artificial intelligence, LiDAR-assisted autonomous vehicles, communication, interconnects, and IoTs integrated datacom networks. However, silicon is inherently weak absorbing material in the near-infrared (NIR) wavelengths, which is highly important for emerging applications in the existing CMOS foundry framework. In contrast, GaAs and their alloys are used as mainstream materials for light detection in many emerging applications due to their high optical absorption coefficient and carrier mobilities. Yet, incompatibility with the CMOS fabrication processes contributed to tedious and costly hybrid integration with CMOS electronics. Therefore, innovative techniques to enhance light-material interaction are crucial to designing photodetectors with thinner silicon film.

Therefore, we have facilitated a photon-trapping approach to address the trade-off challenges between optical absorption efficiency and high-speed (bandwidth). We started the project with Si PDs since it is CMOS compatible and can detect the visible spectrum up to NIR 1100 nm. Next, we explored Ge PDs, which are also CMOS compatible to enhance the effectivity and cover the wavelengths up to 1800 nm. Finally, we explored the PT approach in III-V PDs (short (850 nm) and long-reach (1310-1550 nm) communications), MQW PDs (1-3 µm), and IR detectors:

First, we developed the PT concept in Si photodetector, APD, and SPAD to enable monolithically PD integration in the CMOS platform. However, the formation of nanoholes on the Si PD active region induced an extremely high leakage current of ~ 11 mA. Chapter 3 presents different Si PDs surface passivation schemes that allowed us to successfully inhibit Si device degradation caused by RIE etching of nanoholes [1, 2].

Chapter 4 presents photon-trapping nanostructure PDs enable ultra-fast and high-efficiency Si vertical PIN PDs. Additionally, the chapter discusses many designs and approaches to maximize the efficiency of photon-trapping ultra-fast Si [3-5].

Next, chapter 5 presents photovoltaic characteristics of light-trapping in thin Si solar cells that could be utilized for indoor and outdoor IoT self-standing applications.

Extremely sensitive and high-gain Si APDs and SPADs are discussed in chapter 6. The light penetration depth engineering approach is also developed and enabled via careful photon-trapping nanostructures designs. The unique responsivity of different photon-trapping designs paves the way to develop on-chip spectroscopy/computational imaging application. The fabricated Si PDs can be utilized in optical communication, LIDAR, quantum communication, and biomedical applications.

Chapter 7 presents lateral Si PT MSM design with the thinner active region that enhances the optical efficiency of silicon PDs to achieve higher photoabsorption than group III-V semiconductors in silicon using photon-trapping nanoholes. Additionally, such Si photon trapping

structures help reduce the photosensor's capacitance compared to the planar counterpart, enhancing the device's ultra-fast photoresponse capability.

The next step was to explore such an approach in Si CMOS image sensors and model different photon-trapping in the image sensors. Chapter 8 presents the modeling approach of a single microhole per pixel in Si CMOS Image sensors with enhanced optical sensitivity in near-infrared. The effect of deep trench isolation is discussed subsequently. Finally, the photon-trapping approach is utilized in Ge-on-Si CMOS image sensors to extend the imaging capability and enhance sensitivity to longer wavelengths up to 1700 nm.

In chapter 9, we explore photon-trapping approaches further in vertical Ge-on-Si PIN PDs. It should be noted that Ge-on-Si PDs are also CMOS compatible and can be operational at 1310 nm and 1550 nm, where Si is not responsive due to its bandgap limitations. Photon-trapping Ge PDs show enhanced response for a wider spectrum range and even showed an acceptable ability to respond at 1750 nm where conventional Ge is not responsive. Additionally, Ge PT PD presents an ultra-fast optical response, as discussed in chapter 9.

We further explored and studied the PT approach in III-V PDs in chapter 10. GaAs and InGaAs PDs integrated with PT nanostructures are modeled and simulated. GaAs PDs are utilized for short-reach communication 850 nm, while InGaAs PDs are utilized for long-reach optical communication. Due to their high absorption and carrier mobilities, the thinner absorbing layer can be designed with PT nanoholes to confirm ultra-fast response (high bandwidth) without losing absorption efficiency. InGaAs PD layer MBE growth, fabrication, and characterization with projected ultra-fast response are also discussed.

To detect longer wavelengths in the NIR region, such as 1-3 μm, we have developed type -II Multi quantum wells (MQWs) PDs integrated with PT designs for high-efficiency, high-temperature, and ultra-fast operation. Multi-quantum wells design facilitates a bandgap engineering mechanism that helps design an artificial semiconductor to detect a desired wavelength. The optical simulation, modeling, and fabrication of MQWs PDs are discussed in chapter 11.

Finally, to extend the detection capabilities of wavelengths that range between (2-13 μm), we have further explored the PT approach in PbSe and HgCdTe IR detectors. The modeling of photon-trapping holes with different designs and their impact on the optical absorption efficiency are investigated and discussed in chapter 12. Our simulations demonstrated that the lateral modes of infrared photons that propagate along the detector's surface could enhance the optical absorption capability of ultrathin high-performance infrared detectors.

13.2 Applications opportunities

High-efficiency and ultra-fast photodetectors are highly demanded in optical communications, sensing, and imaging applications. This section presents some existing and emerging applications in quantum communication, biomedical imaging, artificial intelligence, LiDAR-assisted autonomous vehicles, optical communication, interconnects, and IoTs integrated datacom networks.

13.2.1 Optical communications in datacenters

Our highly efficient and ultra-fast photon-trapping CMOS-compatible Si and Ge-on-Si PDs can work as optical interconnects in the short-reach (λ=850nm) and long-haul (λ=1300, 1550nm) communication windows. Our approach not only enhanced the optical absorption but also reduced junction capacitance, which enhanced the PDS's speed characteristics and allowed the development of an on-chip ultra-fast CMOS-compatible data center receiver. Furthermore, III-V PDs integrated with photon trapping structures modeling also reveal that with the thinner active region, the optical absorption can be enhanced compared to the conventional counterpart, and the bandwidth of the PDs could be further improved for higher bandwidth communications.

13.2.2 Free space optical communications

Free space communication (FSO), such as light detection and ranging systems (LIDAR) and 3D imaging systems, have been highly developed in the recent past due to the interest in implementing these systems in autonomous cars. This application needs to be able to sense and

quickly respond to objects at distances over 100 m to avoid car collisions. Atmospheric transmission loss, environmental noise, fog, air turbulence, and the restrictions on maximum laser power result in only a small number of photons reaching the LIDAR receiver [6]. Long-range detection (>200m) is required to be measured by LIDAR, and only APDs and SPADs can achieve that range. Receivers based on Silicon PDs can operate at 905 and 940 nm. Ge-on-Si/ $In_{0.53}Ga_{0.47}As$ operating at 1550 nm are the current technologies that depend on laser power requirements, sensitivity, maturity of fabrication, and atmospheric transmission. As mentioned earlier, the photon-trapping approach has been investigated in the semiconductor, and enhanced sensitivity was achieved with a higher signal-to-noise ratio, as discussed in chapter 6.

13.2.3 Quantum communication

Big data and information interchanging increase security challenges, especially insecure data transmission; quantum communication are projected to be the most secure technology for data transmission. Since tapping into the transmission line will destroy the quantum states of entangled photons, immediate detection of a tapped line will be possible in a quantum communication system (QCS). Single-photon detectors SPADs are the main component in the receiver of a QCS [7]. Therefore, highly sensitive and extremely low-noise photodetectors are needed to detect a very low number of photons down to a single photon detection. Photon-trapping Si APD and SPAD present high-gain and low dark current ~ 30 pA, which can be further reduced with an effective passivation process to detect a low number of photons, as discussed in chapter 6.

13.2.4 CMOS image sensors

Si CMOS image sensor modeling shows that a single funnel hole in a device provides better efficiency than a conventional image sensor in visible and NIR. A funnel-shaped hole with a size comparable to the wavelength converts the propagation direction of light into lateral and provides a better light trapping effect and reduces the reflection with higher resolution that implemented this technique for high-speed Si photodetectors. While Ge-on-Si CMOS image sensor modeling

revealed that cylindrical holes per pixel enhance NIR efficiency compared to the conventional image sensor. Therefore, employing such designs in image sensors can enhance their resolution and performance.

13.2.5 Biomedical imaging applications

Higher detection efficiency and time resolution in photodetectors in the entire visible range are crucial to improving the image quality of time-of-flight (TOF)-based biomedical imaging systems and fluorescence lifetime imaging (FLIM) [8]. Furthermore, our approach to designing PT allows us to engineer the optical penetration depth in APDs and SPADs [9]. This leads to a higher gain bandwidth required in various emerging applications, including biomedical imaging systems and other emerging applications.

13.2.6 computational imaging (AI-assisted imaging) applications

Photonic spectroscopy utilizes dispersive components such as prisms, diffraction gratings, or filters to split wavelengths. Then, these wavelengths are guided to an array of identical PDs to record their intensities. This system is bulky and costly. However, reconstructive computational imaging depends on a few unique response PDs. The unique response of each detector can be computationally reconstructed to replicate the complete spectrum. Our unique optical response for different photon-trapping PDs can be utilized to replace this bulky and expensive system. Such imaging systems reduce the number of PDs to fewer and facilitate system miniaturization. Moreover, these unique response detectors are designed to respond to ultra-fast signals to simultaneously acquire spectral (wavelength), temporal responses, and (time-of-flight) ToF information in a single measurement run. Such development enables system miniaturizing, and advances to application-specific integrated circuit (ASIC) based systems-on-chip (SoC) PDs.

13.3 Future research opportunities

This section discusses a few future research opportunities, with some preliminary results that can be developed and explored further.

13.3.1 Photon-trapping designs

Many photon-trapping designs can be explored; they could be periodic or aperiodic pattern nanostructures. For instance, a sunflower seed pattern could confine the photons in devices and reflect a unique optical response. Figure 13.1 (a) shows a pattern as a spiral design with angles proportional to 137.5°. This angle is known as the Golden angle and follows a Fibonacci series. It ensures the most efficient packing of the structure, which has the potential to further enhance the optical efficiency in PDs. Figure 13.1 (b,c) shows different spiral photon-trapping PDs designs created in optical mask layout.

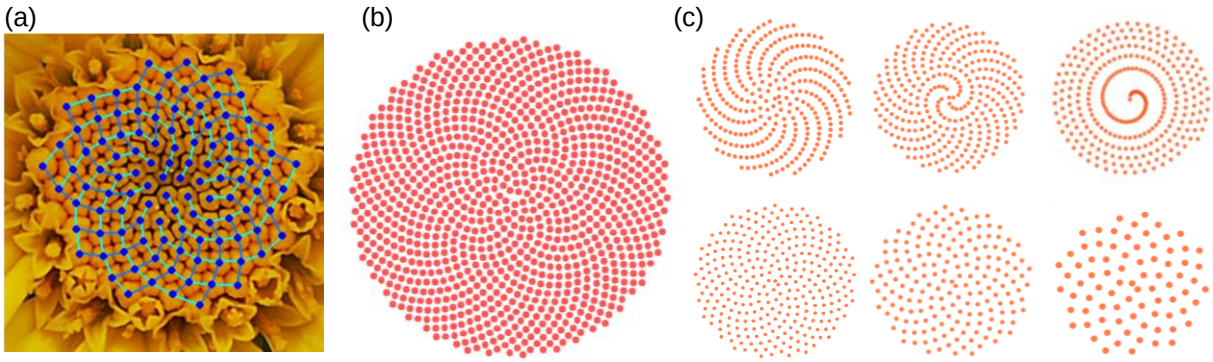


Fig. 13.1. spiral photon-trapping designs. (a) Sunflower seed pattern. (b,c) Different spiral photon trapping designs were created in the optical mask layout of PDs.

13.3.2 Flexible photon-trapping photodetectors

Light-weight and flexible sensors are needed for smart devices, such as smart wearables, smart gadgets, and wearable optics, for augmented reality (AR) and virtual reality (VR). In addition to the smart medical wearables, and all other small gadgets that we can use and have some connectivity, and requires sensing, and power sources (PV). Therefore, to develop a flexible sensor, thinner PDs are required, which again suffer from low efficiency. Our photon-trapping designs can enhance the efficiencies of such thin devices. Furthermore, such small-scale devices

can be released and transferred from the mother substrate to various platforms, such as the tips of fiber optic cables for realizing fiber receivers and probing applications in vivo studies. A simple process was developed by dissolving the buried oxide in diluted HF in DI water (1:10) to release the fabricated Si PDs and transfer them to glass and aluminum-coated glass. The transferred PDs were characterized, and the results are shown in Fig. 13.2.

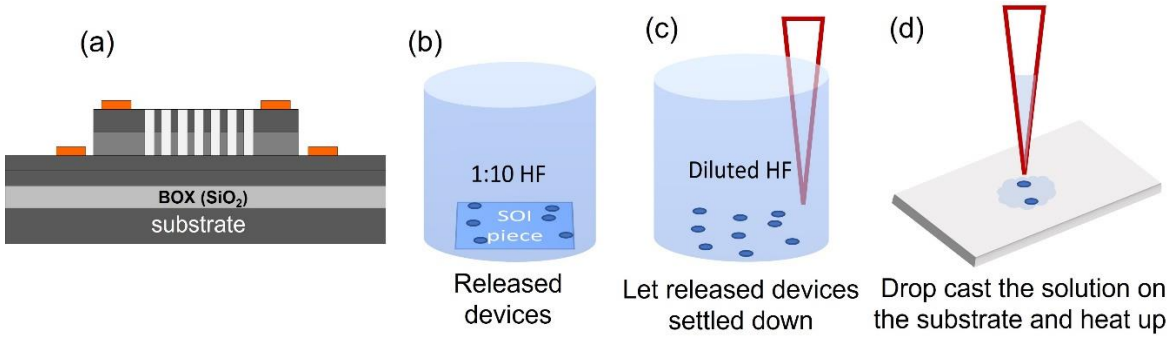


Fig. 13.2. (a) Si PD on SOI wafer. (b) Dissolve BOX in HF and release PDs. (c) Remove the substrate, dilute with DI water, and let PDs settle. (d) Drop cast the solution on the substrate and heat it to evaporate the solution.

HF damages the metal contact; therefore, HF vapor is recommended, and/or PDs coated with the polymer prior to the HF release process. The quantum efficiency of devices transferred to aluminum-coated glass was observed to get enhanced compared to the ones on glass substrate due to the back reflection, as can be seen in Fig. 13.3. Although the EQE values are lower compared the ones before releasing, which is expected due to degradation in PDs during releasing/transferring process.

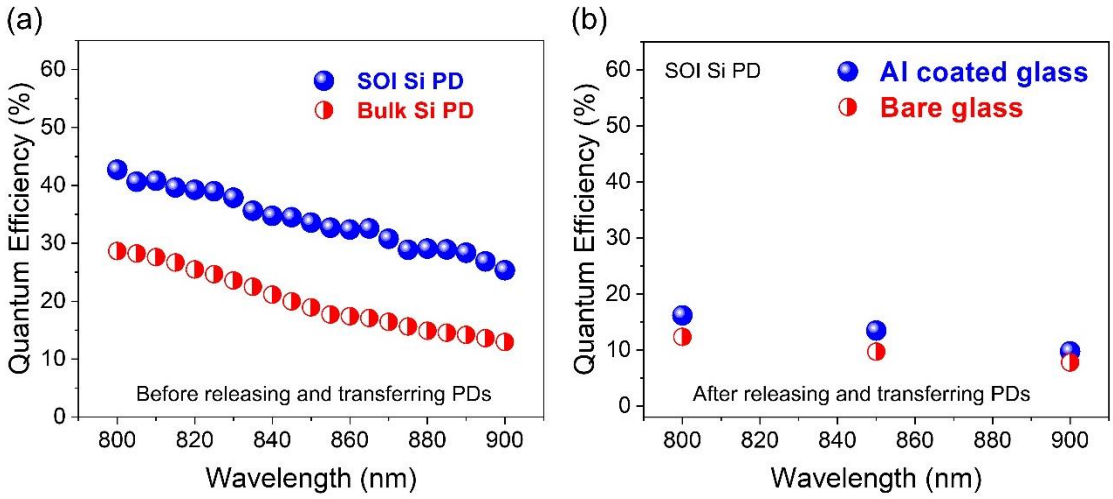


Fig. 13.3. (a) EQE of PDs before releasing for Si on SOI and bulk Si PD. (b) EQE of the transferred Si PD on bare glass vs. on Al-coated glass.

Figure 13.4 (a) shows the transferred Si PD on a glass substrate, while Fig. 13.4 (b,c) shows the released PD is attached to the optical fiber tip. Therefore, Si PD can be placed on the tip of a catheter or endoscope, and with a photon-trapping unique response, AI-assisted imaging can be facilitated for biomedical imaging.

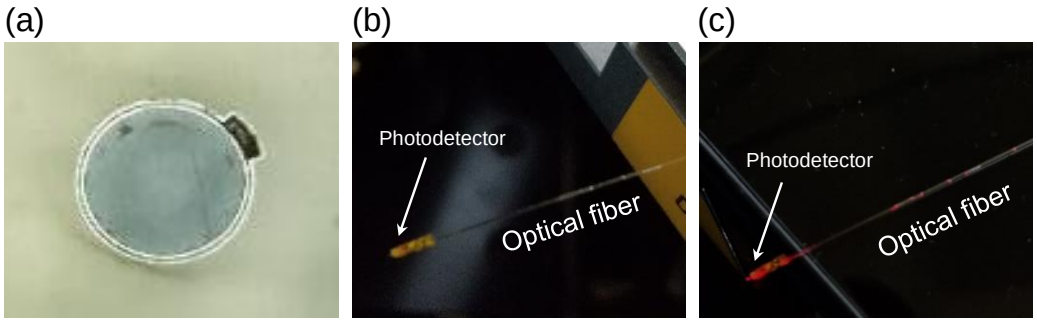


Fig. 13.4. (a) Released Si PD microscopic image on bare glass. (b) Si PD is transferred and attached to the optical fiber tip (no illumination). (c) Si PD is attached to an optical fiber tip (with illumination)

13.3.3 Waveguide edge illuminated Si PIN photon-trapping for 1310 nm optical communication based on assisted tunneling.

Although Si does not absorb at 1310 nm wavelength, Intel labs demonstrated a high-speed PN-junction silicon waveguide photodetector based on a combination of effects of two-photon absorption (TPA), surface state absorption (SSA), and photon-assisted tunneling (PAT) in the PN junction [10]. As a result, 50 Gb/s optical signal detection with a responsivity of 0.6 A/W for 1310

nm wavelength, a dark current of 850 nA, and an eye signal-to-noise ratio (SNR) of 7.3 was achieved. This device can be further improved for higher bandwidth (above 100 Gb/s) and lower dark current by reducing the device length, enabling lower RC time, and reducing leakage current. Based on our photon-trapping design [Fig. 13.5 (b)] the efficiency limitation of a shorter waveguide can be addressed using integrated one-dimensional periodic slow light structures that can enhance light-matter interaction [Fig. 13.5 (c)] in a way similar to optical resonators but retaining the large bandwidth of traveling wave devices. These structures are simple to fabricate, and the optical propagation losses are low. This contributes to the reduced footprint of waveguide detectors while improving efficiency by 40%-80%. On the other hand, the structures with integrated holes can increase internal reflections, leading to slower propagation along the waveguide. A linear approximation shows slow-light structure can offer the desired quantum efficiency (Responsivity) with a 40% shorter waveguide. Designing a shorter waveguide with sufficient optical absorption is promising to push the bandwidth limits to higher values. A similar approach can also be employed in optical modulators for enhanced modulation while miniaturizing the devices. Such design enables ultra-fast waveguide photodetectors and Mach-Zehnder modulators with the performance parameters using low-cost, high-volume manufacturing (HVM), CMOS, and silicon photonics (SiPh) compatible processes for a broad operating temperature range between -30C to 70C.

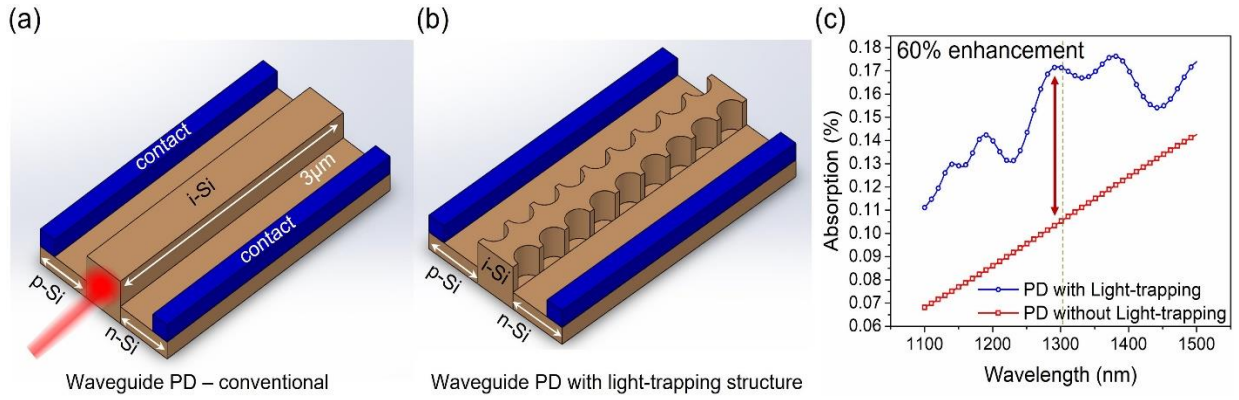


Fig. 13.5. (a) Edge-illuminated conventional Si PD (without photon-trapping design). (b) Edge-illuminated photon-trapping Si PD. (c) Slow-light structures enabling absorption enhancement in Mach-Zehnder

waveguide for wavelengths below silicon bandgap. The absorption is shown for a 3 μm long segment of a waveguide. More than 60% enhancement is possible with light-trapping slow-light structures.

13.3.4 Waveguide edge illuminated Ge PIN photon-trapping for 1310 nm and 1550 nm optical communication.

Heterogeneous integration with other semiconductor materials with smaller bandgaps, such as germanium (Ge), has been envisioned for photodetection for wavelength above 1.1 μm in the Si photonics platforms. Rapid progress over the past decade in this field has realized highly responsive and high-speed Ge-on-Si photodetectors (PDs). As discussed in chapter 9, Ge-on-Si surface-illuminated PIN detectors integrated with photon-trapping designs have enhanced efficiency with ultra-fast operation up to an incident wavelength of 1800 nm. As a result, Waveguide edge illuminated high efficiency and ultra-fast Ge-on-Si PIN photon-trapping can be utilized for 1310 nm and 1550 applications in optoelectronic integrated circuits (OEICs). Our designed simulation results show higher efficiency for waveguide-based Ge photodetector than its conventional counterpart. The device schematic and simulation results can be seen in Fig. 13.6.

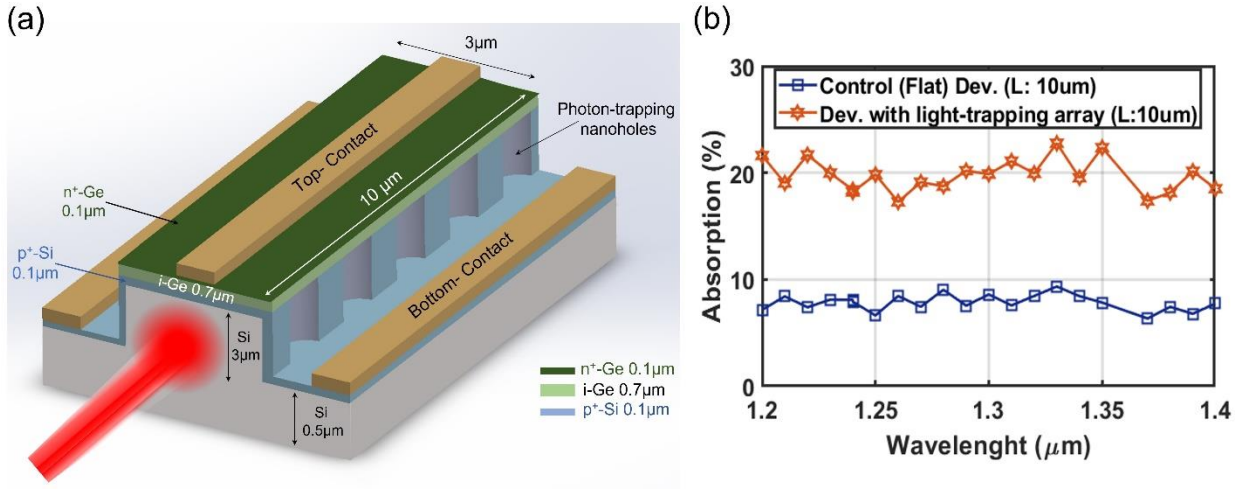


Fig. 13.6. Schematic of designed waveguide photon-trapping Ge-on-Si PD. (b) Enhanced optical absorption efficiency in waveguide photon-trapping Ge-on-Si PD compared to its conventional counterpart.

13.3.5 Suspended Photon-trapping Si and Ge-on-Si CMOS-compatible PDs

In our fabricated Si photon-trapping PDs on SOI wafers, Photon-trapping holes allow hydrofluoric acid (HF) to flow through the holes and reach the bottom buried oxide (BOX) layer. This utilizes fast etching underneath the holes than etching SiO_2 under bulk Si elsewhere. Hence, a suspended Si and Ge-on Si photon-trapping PD can be developed and investigated for different applications. Figure 13.7. shows the schematics of Si PT PDs cross-section before immersing in the HF (a), while in (b), the schematic shows air-Si-air suspended Si PT PD after immersing the wafer in HF solution.

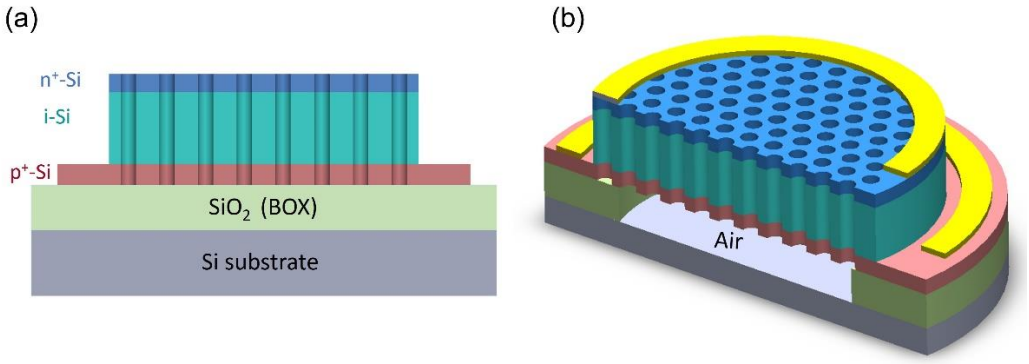


Fig. 13.7. (a) Schematic of the cross-sectional view of Si PT PD before etching SiO_2 underneath the holes. (b) Schematic of Si PT PD after etching SiO_2 underneath the holes with the suspended structure on air. The PD is still attached to the wafer and stabled with surrounding mechanical support.

Figure 13.8. shows the SEM images of the suspended Si PT PDs, which indicate photon-trapping holes can assist in creating such suspended structures.

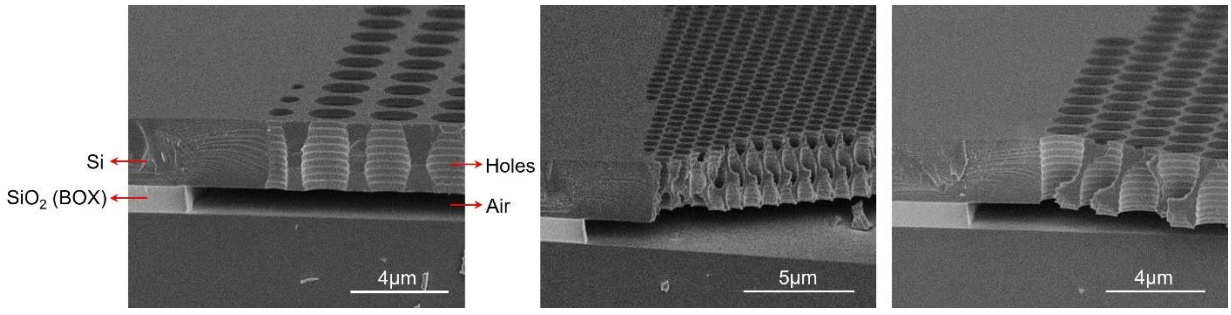


Fig. 13.8. SEM images of the suspended Si photon-trapping PD.

Current-voltage measurements of the suspended devices show an enhanced response for the photon-trapping Si PD photocurrent compared to the control Si PD. Both PDs were immersed in HF for the same period. The quantum efficiency of the suspended Si PT PD at 850 nm illumination was measured to be around 34% at -3V, whereas the EQE of the control Si PD was measured to be around 19% at -3V, as can be seen in Fig. 13.9. The results of the suspended Si PT PD was lower than what was measured before suspending process but still better than its conventional counterpart, which could be attributed to some holes damage during the sonication process in addition to back-reflection vanishing which was caused by the SiO_2 underneath the holes.

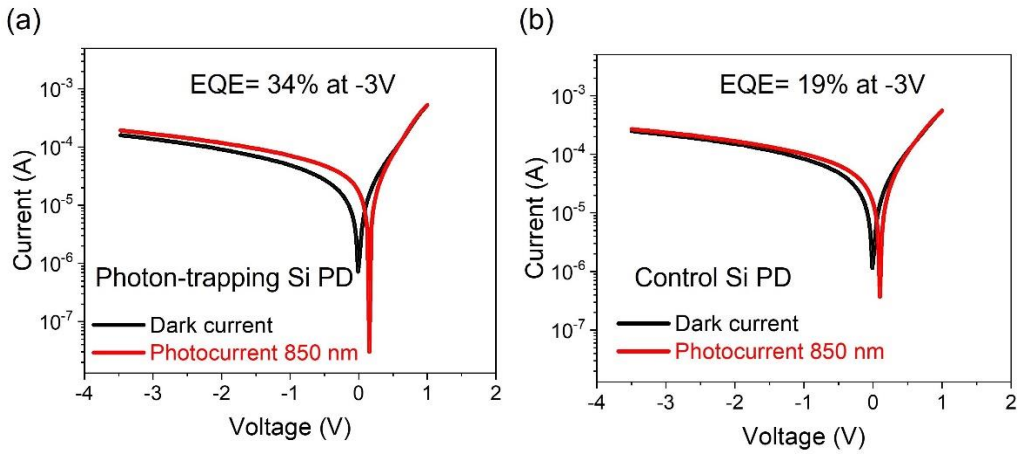


Fig. 13.9. Current-voltage and EQE characterization for (a) Suspended photon-trapping Si PD. (b) Control Si PD.

Suspended photon-trapping design in Ge or SiGe PD can be utilized for edge-illuminated waveguide PDs. Figure 13.10 shows the suspended air-Ge-air PT PD design for Si photonics chips, which can be fabricated according to the discussed process. The SiO_2 facet can act similarly to a semi-reflecting mirror to enhance the evanescent optical coupling to the PD. Additionally, a mirror can be mounted on the detector, further enhancing the optical absorption of the SiGe or Ge PD with the photon-trapping optimized designs.

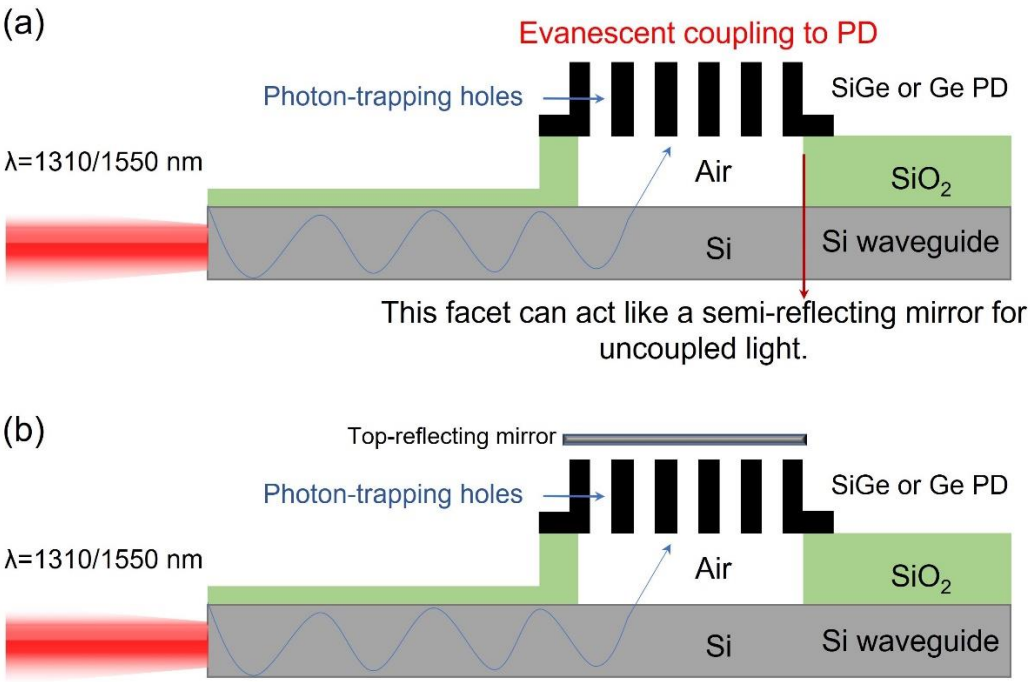


Fig. 13.10. Edge-illuminated air-Ge/SiGe-air waveguide PD for Si Photonics ICs (a) Suspended Ge/SiGe PT waveguide PD enabled by photon-trapping holes. (b) Top-reflecting mirror is placed on top of the PT PD to further enhance optical absorption in the device.

13.3.6 Photon-trapping Si PD and Ge-on-Si PD CMOS foundry integration on Si photonics platform by developing process design kit (PDK)

Silicon photonics (SiPh) is a technology that integrates tons of optical devices on an IC chip employing the fabrication technology of the CMOS manufacturers to offer a guideline towards mass production for the growing market at possibly low cost. PDK is a generic fabrication library defined by CMOS foundries. The designers should follow the fabrication steps and the provided library list so that industries can accommodate new designs. However, customizing a new PDK design process is very costly, and hard to find a foundry that can accept changing its well-established process for desired specifications. Therefore, photon-trapping designs on Si or Ge-on-Si PDs PDK designs must be developed so the CMOS industry can adopt them in their processing platform. CMOS foundry standards and quality are exceptionally high, so we expect with optimized PDK designs, our photon-trapping designs in Si and Ge-on-Si can perform better once the CMOS foundry adopts them in their production line.

13.3.7 Photon-trapping unique responsivity for spectroscopy on a Chip

Chapter 6 presents and discusses the unique responsivity of different photon-trapping design APDs. These unique responses with AI-assisted algorithms and computational imaging can enable miniaturized and highly compact spectroscopy on a chip for biomedical imaging. Our group is developing techniques to adopt miniaturized spectroscopy that could be mounted on a catheter, FLIM, and endoscope for real-time diagnosis during medical surgeries [Fig. 13.11]. Low light illumination and detection ensure the safety of human tissues, which can be enabled by such imaging for early disorder diagnosis.

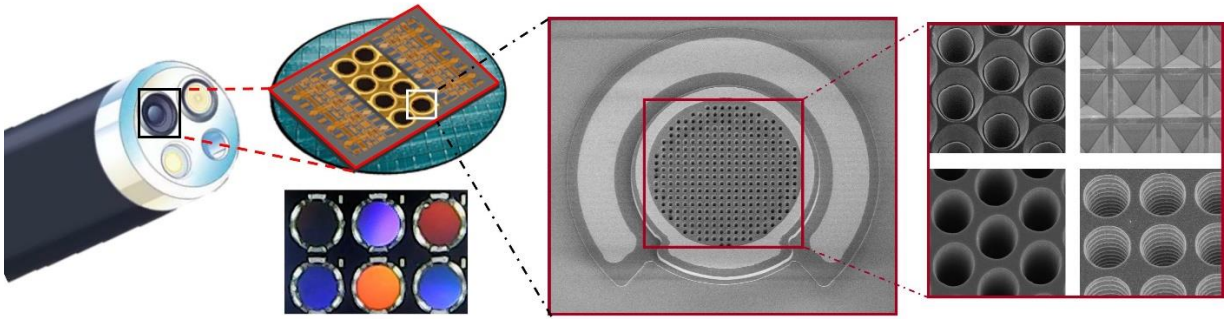


Fig. 13.11. Unique response of different photon-trapping designs, Si APDs enable miniaturized computational imaging on a chip.

13.3.8 Sensing in food and agriculture

Ultra-fast photon-trapping (PT) detectors can also sense nutrition uptake, health, and disorders in plants, crops, and fruits by correlating wavelength profiling. High-performance PT CMOS FLIM sensors can assist in identifying and locating mature fruits and vegetables in sustainable controlled environment agriculture (CEA). Real-time sensing will allow us to explore the nutrient elements' influence on crops' aroma, taste, health, and overall quality. Our group is also developing a system that integrates photon-trapping and other sensing approaches for the CEA real-time imaging and sensing to improve the quality of the products.

References

[1] A. S. Mayet *et al.*, "Surface passivation of silicon photonic devices with high surface-to-volume-ratio nanostructures," *JOSA B,* vol. 35, no. 5, pp. 1059-1065, 2018.

[2] A. S. Mayet *et al.*, "Inhibiting device degradation induced by surface damages during top-down fabrication of semiconductor devices with micro/nano-scale pillars and holes," in *Low-Dimensional Materials and Devices 2016*, 2016, vol. 9924: SPIE, pp. 36-42.

[3] C. Bartolo-Perez *et al.*, "Maximizing Absorption in Photon-Trapping Ultrafast Silicon Photodetectors," *Advanced Photonics Research,* vol. 2, no. 6, p. 2000190, 2021.

[4] S. Ghandiparsi *et al.*, "High-speed high-efficiency broadband silicon photodiodes for short-reach optical interconnects in data centers," in *2018 Optical Fiber Communications Conference and Exposition (OFC)*, 2018: IEEE, pp. 1-3.

[5] Y. Gao *et al.*, "Photon-trapping microstructures enable high-speed high-efficiency silicon photodiodes," *Nature Photonics,* vol. 11, no. 5, pp. 301-308, 2017.

[6] M. Ghioni, A. Gulinatti, I. Rech, F. Zappa, and S. Cova, "Progress in silicon single-photon avalanche diodes," *IEEE Journal of selected topics in quantum electronics,* vol. 13, no. 4, pp. 852-862, 2007.

[7] L. Calderaro *et al.*, "Towards quantum communication from global navigation satellite system," *Quantum Science and Technology,* vol. 4, no. 1, p. 015012, 2018.

[8] C. Bartolo-Perez *et al.*, "Avalanche photodetectors with photon trapping structures for biomedical imaging applications," *Optics Express,* vol. 29, no. 12, pp. 19024-19033, 2021.

[9] C. Bartolo-Perez *et al.*, "Engineering the gain and bandwidth in avalanche photodetectors," *Optics Express,* vol. 30, no. 10, pp. 16873-16882, 2022.

[10] M. Sakib, J. Sun, R. Kumar, J. Driscoll, K. Yeung, and H. Rong, "Demonstration of a 50 Gb/s all-silicon waveguide photodetector for photonic integration," in *CLEO: Applications and Technology*, 2018: Optica Publishing Group, p. JTh5A. 7.

List of publications

Journals

[1] Gao, Yang, Hilal Cansizoglu, Kazim G. Polat, Soroush Ghandiparsi, Ahmet Kaya, Hasina H. Mamtaz, **Ahmed S. Mayet et al**. "Photon-trapping microstructures enable high-speed high-efficiency silicon photodiodes." Nature Photonics 11, no. 5 (2017): 301-308.

[2] **Mayet, Ahmed S.,** Hilal Cansizoglu, Yang Gao, Soroush Ghandiparsi, Ahmet Kaya, Cesar Bartolo-Perez, Badriyah AlHalaili et al. "Surface passivation of silicon photonic devices with high surface-to-volume-ratio nanostructures." JOSA B 35, no. 5 (2018): 1059-1065.

[3] Cansizoglu, Hilal*, **Ahmed S. Mayet***, Soroush Ghandiparsi, Yang Gao, Cesar Bartolo-Perez, Hasina H. Mamtaz, Ekaterina Ponizovskaya Devine et al. "Dramatically enhanced efficiency in ultra-fast silicon MSM photodiodes via light trapping structures." IEEE Photonics Technology Letters 31, no. 20 (2019): 1619-1622. (*equal contribution)

[4] Bartolo-Perez, Cesar, Soroush Chandiparsi, **Ahmed S. Mayet**, Hilal Cansizoglu, Yang Gao, Wayesh Qarony, Ahasan AhAmed et al. "Avalanche photodetectors with photon trapping structures for biomedical imaging applications." Optics Express 29, no. 12 (2021): 19024-19033.

[5] Bartolo-Perez, Cesar, Ahasan Ahamed, **Ahmed S. Mayet**, Amita Rawat, Lisa McPhillips, Soroush Ghandiparsi, Julien Bec et al. "Engineering the gain and bandwidth in avalanche photodetectors." Optics Express 30, no. 10 (2022): 16873-16882.

[6] Ghandiparsi, Soroush, Aly F. Elrefaie, **Ahmed S. Mayet**, Taha Landolsi, Cesar Bartolo-Perez, Hilal Cansizoglu, Yang Gao et al. "High-speed high-efficiency photon-trapping broadband silicon PIN photodiodes for short-reach optical interconnects in data centers." Journal of Lightwave Technology 37, no. 23 (2019): 5748-5755.

[7] Bartolo-Perez, Cesar, Wayesh Qarony, Soroush Ghandiparsi, **Ahmed S. Mayet**, Ahasan Ahamed, Hilal Cansizoglu, Yang Gao et al. "Maximizing Absorption in Photon-Trapping Ultrafast Silicon Photodetectors." Advanced Photonics Research 2, no. 6 (2021): 2000190.

[8] Cansizoglu, Hilal, Aly F. Elrefaie, Cesar Bartolo-Perez, Toshishige Yamada, Yang Gao, **Ahmed S. Mayet**, Mehmet F. Cansizoglu, Ekaterina Ponizovskaya Devine, Shih-Yuan Wang, and M. Saif Islam. "A new paradigm in high-speed and high-efficiency silicon photodiodes for communication—Part II: Device and VLSI integration challenges for low-dimensional structures." IEEE Transactions on Electron Devices 65, no. 2 (2017): 382-391.

[9] Devine, Ekaterina Ponizovskaya, Wayesh Qarony, Ahasan Ahamed, **Ahmed Surrati Mayet**, Soroush Ghandiparsi, Cesar Bartolo-Perez, Aly F. Elrefaie, Toshishige Yamada, Shih-Yuan Wang, and M. Saif Islam. "Single microhole per pixel in CMOS image sensors with enhanced optical sensitivity in near-infrared." IEEE Sensors Journal 21, no. 9 (2021): 10556-10562.

[10] Devine, E. Ponizovskaya, Ahasan Ahamed, **Ahmed S. Mayet**, Soroush Ghandiparsi, Cesar Bartolo-Perez, Lisa McPhillips, Aly F. Elrefaie, Toshishige Yamada, Shih-Yuan Wang, and M. Saif Islam. "Optimization of CMOS image sensors with single photon-trapping hole per pixel for enhanced sensitivity in near-infrared." arXiv preprint arXiv:2110.00206 (2021).

[11] Ponizovskaya-Devine, Ekaterina, **Ahmed S. Mayet**, Amita Rawat, Ahasan Ahamed, Shih-Yuan Wang, Aly F. Elrefaie, Toshishige Yamada, and M. Saif Islam. "Single Micro-hole per Pixel for Thin Ge-on-Si Image Sensor with Enhanced Sensitivity upto 1700 nm." *arXiv preprint arXiv:2209.14242* (2022).

[12] Yamada, Toshishige, Ekaterina Ponizovskaya Devine, Soroush Ghandiparsi, Cesar Bartolo-Perez, **Ahmed S. Mayet**, Hilal Cansizoglu, Yang Gao, Ahasan Ahamed, Shih-Yuan Wang, and M. Saif Islam. "Modeling of nanohole silicon pin/nip photodetectors: Steady state and transient characteristics." Nanotechnology 32, no. 36 (2021): 365201.

[13] Gou, Jun, Hilal Cansizoglu, Cesar Bartolo-Perez, Soroush Ghandiparsi, **Ahmed S. Mayet**, Hossein Rabiee-Golgir, Yang Gao et al. "Rigorous coupled-wave analysis of absorption enhancement in vertically illuminated silicon photodiodes with photon-trapping hole arrays." Nanophotonics 8, no. 10 (2019): 1747-1756.

[14] Kaya, Ahmet, K. Gurkan Polat, **Ahmed S. Mayet,** Howard Mao, Şemsettin Altındal, and M. Saif Islam. "Manufacturing and electrical characterization of Al-doped ZnO-coated silicon nanowires." Materials Science in Semiconductor Processing 75 (2018): 124-129.

Conferences

[1] **Mayet, Ahmed S**., Hilal Cansizoglu, Yang Gao, Ahmet Kaya, Soroush Ghandiparsi, Toshishige Yamada, Shih-Yuan Wang, and M. Saif Islam. "Inhibiting device degradation induced by surface damages during top-down fabrication of semiconductor devices with micro/nano-scale pillars and holes." In *Low-Dimensional Materials and Devices 2016*, vol. 9924, pp. 36-42. SPIE, 2016.

[2] Bartolo-Perez, Cesar, Soroush Ghandiparsi, **Ahmed S. Mayet**, Ahasan Ahamed, Wayesh Qarony, Hilal Cansizoglu, Yang Gao et al. "Controlling the photon absorption characteristics in avalanche photodetectors for high resolution biomedical imaging." In Nanoscale Imaging, Sensing, and Actuation for Biomedical Applications XVIII, vol. 11658, pp. 5-10. SPIE, 2021.

[3] Ghandiparsi, Soroush, Aly F. Elrefaie, **Ahmed S. Mayet**, Cesar Bartolo-Perez, Hilal Cansizoglu, Yang Gao, Ekaterina Ponizovskaya Devine et al. "Up to 1700nm broadband high-efficiency surface-illuminated Ge/Si photodiode with microhole array." In Integrated Photonics Research, Silicon and Nanophotonics, pp. IT3A-3. Optica Publishing Group, 2019.

[4] Bartolo-Perez, Cesar, Soroush Ghandiparsi, **Ahmed S. Mayet**, Hilal Cansizoglu, Yang Gao, Ekaterina Ponizovskaya Devine, Nibir Dhar, Shih-Yuan Wang, and M. Saif Islam. "Photodetectors with photon-trapping surface nanostructures for short range LIDAR systems." In 2019 IEEE Photonics Society Summer Topical Meeting Series (SUM), pp. 1-2. IEEE, 2019.

[5] Ahamed, Ahasan, Cesar Bartolo-Perez, **Ahmed S. Mayet,** Soroush GhandiParsi, Xiangnan Zhou, Julien Bec, Nibir K. Dhar et al. "Controlling light penetration depth to amplify the gain in ultra-fast silicon APDs and SPADs using photon-trapping nanostructures." In Low-Dimensional Materials and Devices 2021, vol. 11800, p. 118000F. SPIE, 2021.

[6] Ahamad, Ahasan, Soroush Ghandiparsi, Cesar Bartolo-Perez, **Ahmed S. Mayet,** Hilal Cansizoglu, Ekaterina P. Devine, Aly F. Elrefaie et al. "Smart nanophotonics silicon spectrometer array for hyperspectral imaging." In CLEO: Science and Innovations, pp. STh3M-2. Optica Publishing Group, 2020.

[7] Ghandiparsi, Soroush, Aly F. Elrefaie, Hilal Cansizoglu, Yang Gao, Cesar Bartolo-Perez, Hasina H. Mamtaz, **Ahmed Mayet et al**. "High-speed high-efficiency broadband silicon photodiodes for short-reach optical interconnects in data centers." In 2018 Optical Fiber Communications Conference and Exposition (OFC), pp. 1-3. IEEE, 2018.

[8] Kaya, Ahmet, Jianyi Gao, Hilal Cansızoglu, **Ahmed S. Mayet**, Hasina H. Mamtaz, Soroush GhandiParsi, Srabanti Chowdhury, and M. Saif Islam. "Ga2O3 as both gate dielectric and surface passivation via sol-gel method at room ambient." In Wide Bandgap Power Devices and Applications, vol. 9957, pp. 16-23. SPIE, 2016.

[9] Bartolo-Perez, Cesar, Hilal Cansizoglu, Yang Gao, Soroush Ghandiparsi, **Ahmed S. Mayet**, Ekaterina Ponizovskaya Devine, Aly F. Elrefaie, Shih-Yuan Wang, and M. Saif Islam. "Enhanced photon detection efficiency of silicon single photon avalanche photodetectors enabled by photon trapping structures." In 2018 IEEE Photonics Society Summer Topical Meeting Series (SUM), pp. 143-144. IEEE, 2018.

[10] Cansizoglu, H., Gao, Y., Ghandiparsi, S., Kaya, A., Perez, C.B., **Mayet, A.,** Devine, E.P., Cansizoglu, M.F., Yamada, T., Elrefaie, A.F. and Wang, S.Y., 2017, August. Improved bandwidth and quantum efficiency in silicon photodiodes using photon-manipulating micro/nanostructures operating in the range of 700-1060 nm. In Low-Dimensional Materials and Devices 2017 (Vol. 10349, pp. 45-49). SPIE.