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17.5 A 0.8mm³ Ultrasonic Implantable Wireless Neural Recording System with Linear AM Backscattering

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Miniaturization of implantable neural recording systems to micron-scale volumes will enable minimally invasive implantation and alleviate cortical scarring, gliosis, and resulting signal degradation. Ultrasound (US) power transmission has been demonstrated to have high efficiency and low tissue attenuation for mm-scale implants at depth in tissue [1,2,3], but has not been demonstrated with precision recording circuitry. We present an US implantable wireless neural recording system scaled to 0.8mm³, verified to safely operate at 5cm depth with state of the art neural recording performance an average circuit power dissipation of 13µW, and 28.8µW including power conversion efficiency. Sub-mm scale is achieved through single-link power and communication on a single piezocrystal (Lead Zirconate Titanate, PZT) utilizing linear analog backscattering, small die area, and eliminating all other off-chip components.

A simplified block diagram of the system is shown in Fig. 17.5.1, which consists of an external interrogator and a free-floating mote comprised of only a 0.42mm³ PZT, a 0.25mm² IC, and a flex PCB interposer. The mote is encapsulated with a 10µm layer of parylene-C. The interrogator (Cephasonics, cQuest Cicada) sends a pulse in transmit (TX) mode, which arrives at the mote after one time of flight (ToF). The interrogator then switches to receive (RX) mode to receive the reflected amplitude-modulated (AM) wave from the mote after another ToF. The RX chain then amplifies, filters, and digitizes the received signal for demodulation. Interrogation is performed in a pulse-echo fashion to relax the dynamic range requirements on the RX chain by TX-to-RX acoustic leakage and eliminate the need for a circulator. Thus, to avoid TX/RX interference, the pulse width is set to <2 ToF. Since implant depth can vary, a mote placed close to the interrogator (e.g. ~1cm) would have 2xToF~13µs, too short for wake-up and robust multi-bit digital modulation in a single pulse. To overcome this limitation, the IC performs analog AM backscattering which carries higher information per cycle. The analog signal may be transmitted even if only a few cycles are available per pulse. The addition of a unique subcarrier frequency in each mote can enable simultaneous multi-mote interrogation.

The PZT starts harvesting energy upon the arrival of an incident US wave. To eliminate the need for a large off-chip storage capacitor, the mote wakes up when each pulse arrives and sleeps in absence of a pulse. AC voltage generated across the PZT is rectified and regulated by the IC. At its series resonance frequency (f_r=1.78MHz), the PZT can be modeled as an AC source (V_s) and a series resistance (R_s~4kΩ). The acoustic reflection coefficient (Γ) at the boundary of the mote PZT and tissue can be modulated by tuning the impedance in shunt with the PZT (R_m), as shown in Fig. 17.5.2. However, $\Gamma \propto R_m/(R_m+R_s)$ and is therefore nonlinear with respect to R_m making this method impractical for analog backscattering. Linear backscatter modulation is possible as long as the peak voltage across the piezo terminals (V_{PZ}) is modulated linearly. This can be achieved by connecting synchronously upconverted baseband message current (I_m) to the PZT terminals (Fig. 17.5.2). To save area and complexity, the upconversion is implemented by reusing the available active rectifier on-chip, which automatically synchronizes the conduction period to f_r. During each half cycle, I_m generates a voltage drop across R_s linearly modulating $V_{PZ}=V_{PZ}^+-V_{PZ}^-$. The modulation depth of V_{PZ} is designed such that the rectified voltage is always higher than 1.1V, allowing the LDO to continuously regulate the 1V supply ($V_{DD,1V}$). A small on-chip capacitor (C_{store}=130pF) reduces voltage ripple on the rectified voltage (V_{RECT}). At the highest signal frequency of interest (55kHz subcarrier+5kHz neural signal), the impedance of C_{store} is ~5× larger than the impedance of the PZT, which results in I_m being supplied by the PZT rather than C_{store}. Therefore, in steady state, when the active rectifier pass transistor turns on, the peak voltage across V_{PZ} is, to first order, linearly modulated by I_m.

The IC block diagram is shown in Fig. 17.5.3. As V_{RECT} rises, a power-on reset (POR) is triggered and $V_{DD,1V}$ is generated within 10 cycles (~5µs) after the arrival of the incident wave. Control and timing signals are synchronized by a clock, which is extracted from the PZT voltage (T_{CK}=1/f_r). The low-noise amplifier is implemented by an auto-zeroed current-reuse capacitive feedback OTA (Gain 24dB, 250kHz BW required for passing a chopper/subcarrier (~55kHz)). Fast reset switches (ϕ_1, ϕ_2, and ϕ_3) and a power-gated low impedance voltage source are used to quickly charge the input terminals of the OTA to V_{CM}=0.5V in 4T_{CK} at the start of the sample. Chopper switches upmodulate the signal to simultaneously reduce 1/f noise of the amplifier and to act as a subcarrier frequency for communication. The kT/C noise sampled on C_s by the reset switches is modulated out of band when the subcarrier is downmodulated on the Rx side in digital. The chopper/subcarrier frequency (f_{CH}) is divided down from the main clock, while its phase is maintained from sample-to-sample by a reset triggered by the POR signal. The amplifier initialization completes in 12T_{CK} and the output of the AFE is valid after 22T_{CK} (~11µs). 11µs of wakeup time allows backscatter modulation for ~83% of the power-on time at a depth of 5cm. The LNA differential output is forced across a PMOS in triode by means of super source followers generating a linear current over ±200mV of LNA output voltage range. In absence of incident US pulse, the mote PZT is no longer actuated and the circuit turns off gradually as C_{store} discharges (in <10µs), and POR returns to the off state.

The IC was fabricated in a 65nm LP CMOS process. Figure 17.5.4 shows five measured interrogation events of modulated V_{PZ} in response to a 20mV$_{PP}$ input sine wave. The 11µs start-up time and subcarrier modulation at f_{CH} is observable on each pulse. The demodulated output signal and its corresponding spectrum are plotted for a 300Hz, 20mV$_{PP}$ input sine wave whose measured SFDR and THD are -50dB and -44dB, respectively. No harmonic tones are observed in the spectrum for a 10mV$_{PP}$ signal.

The measured static input-output characteristic is shown in Fig. 17.5.5 (output defined as the envelope of V_{PZ}). A 23dB voltage gain over 20mV$_{PP}$ of input range with <1.2% static nonlinearity is achieved. PEDOT:PSS coated electrodes (200x200µm², electroless nickel immersion gold plating) present <10mV DC offset, which is within the V_{IN} range. The demodulated input-referred noise spectral density with and without subcarrier modulation is plotted in Fig. 17.5.5. The total input-referred noise spectral density is 328nV/√Hz, and is dominated by carrier noise, which contributes 319nV/√Hz, therefore the noise contributed by the chip is 76nV/√Hz.

An *in vitro* measurement is shown in Fig. 17.5.6, where the assembled mote is suspended at a distance of 5cm away from the interrogator in water. Backscatter modulation and demodulated signal are shown for a 300Hz, 20mV$_{pp}$ sine wave applied at the input. A comparison with recently published fully integrated sub-mm³ neural recording implants is shown in the table in Fig. 17.5.7. We introduce a linearization technique for AM backscattering in ultrasonic implants. This design occupies the same volume as the smallest neural recording implant, but improves performance by combining low-noise, power-efficient, and linear neural recording with a PEF 2× lower, a depth 2.5×, and a static nonlinearity 40× lower than state of the art [1,4,5].

References:
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[2] T. C. Chang, et al., "27.7 A 30.5mm3 fully packaged implantable device with duplex ultrasonic data and power links achieving 95kb/s with <10E–4 BER at 8.5cm depth," IEEE *ISSCC Dig. Tech. Papers*, pp. 460-461, Feb. 2017.
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[5] P. Yeon, et al., "Towards a 1.1 mm2 free-floating wireless implantable neural recording SoC," *IEEE CICC*, pp. 1-4, 2018.
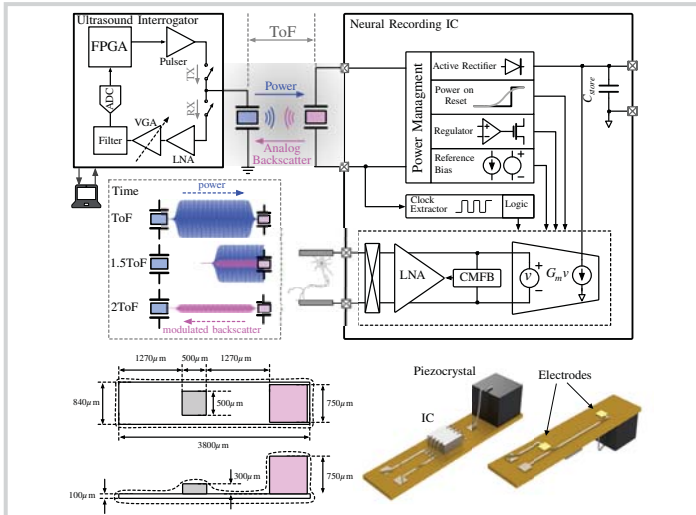
Figure 17.5.1: Simplified system block diagram, time-space conceptual diagram of power transmission and modulated backscattered waves. Assembled mote diagram.

Figure 17.5.2: Backscatter uplink: nonlinear Γ vs. Rm. Linear Γ vs. V_{pz}. Reusing available active rectifier as a synchronous base-band I_m up-converter.
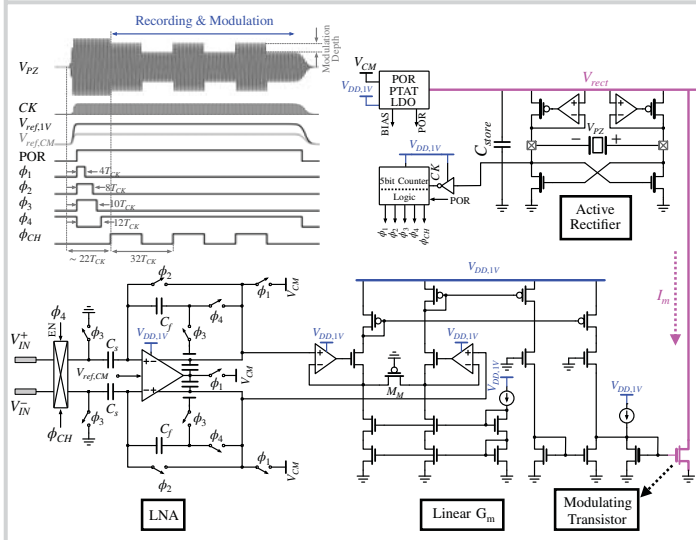

Figure 17.5.3: IC circuit schematics and timing diagram for a single sample pulse. Front-end LNA, subcarrier generation, and linear modulation are shown.
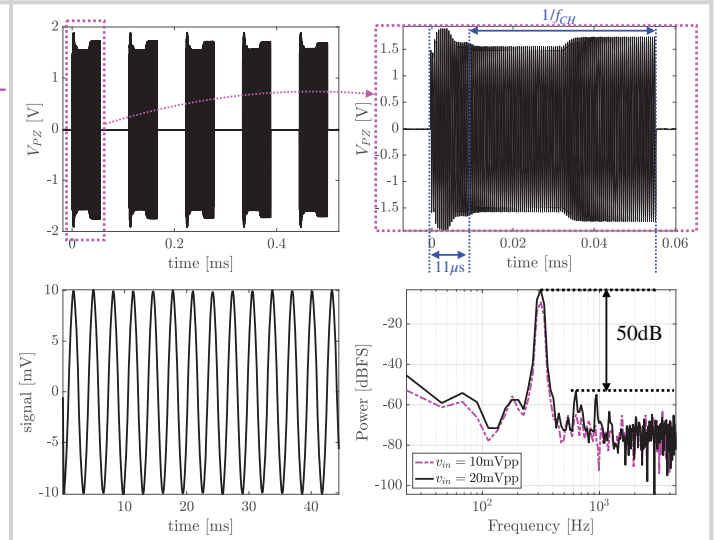
Figure 17.5.4: Five consecutive sample pulses for a 300Hz, 20mVpp input signal, the demodulated input-referred signal, and its corresponding spectrum.
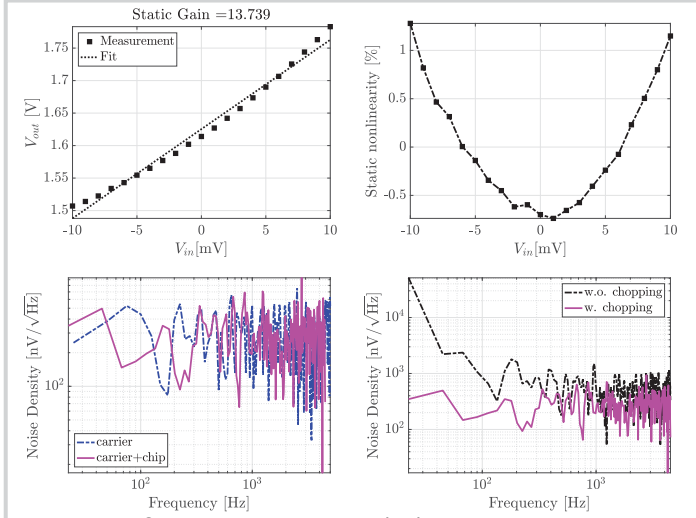

Figure 17.5.5: Static gain and nonlinearity (top); input-referred noise compared with the noise of the carrier alone, with and without chopping/subcarrier (bottom).
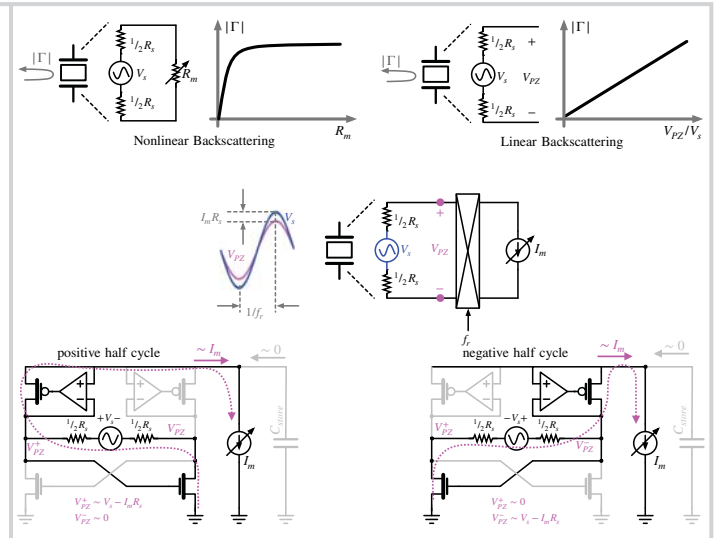

Figure 17.5.6: In vitro measurement results at 5cm depth: two individual backscatter signals, their corresponding AM demodulation and reconstructed 300Hz signal.

17

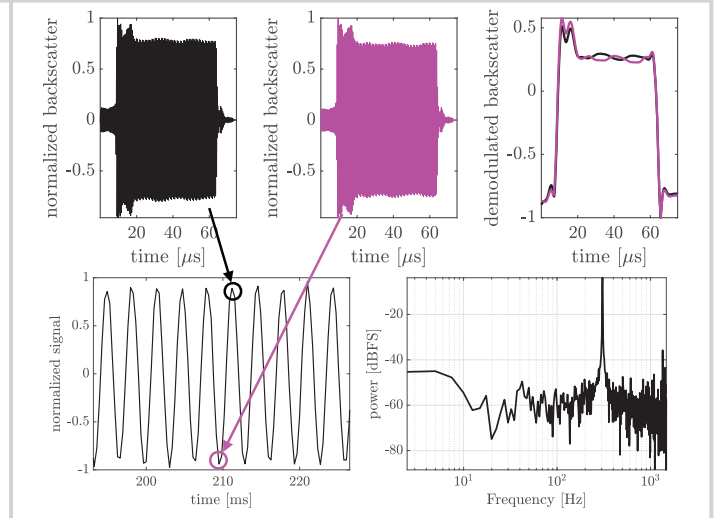|	Neuron'16	ISSCC'18	CICC'18	This work
Link	Ultrasound	Optical	RF	Ultrasound
Back telemetry	AM Backscatter	Analog PPM	IR-UWB	AM Backscatter
Implant depth (mm)	8.8	–	20	50
Total Volume (mm^3)	0.8	–	<1	0.8
Fully packaged	Yes	–	Yes	Yes
Depth/Volume (mm^2)	11	–	30.3	61.7
Technology (nm)	65	180	350	65
Total power (μW)	–	0.9	296*	28.8
IC area (mm^2)	500×450	90×330	1050×1050	500×500
Wake-up time (μs)	3.3	1000	110	11
THD (dB) @10mV$_{pp}$/ @20mV$_{pp}$	–	–	–	-52/-44
Static nonlinearity (%)	–	49†@6mV$_{PP}$	–	1.2@20mV$_{PP}$
LNA noise floor (μV$_{rms}$)	180	42	3.78	5.3
Bandwidth (kHz)	5	10	12	5
power (μW)	–	0.52	42.9	4
NEF/ PEF	–	12.3/136	6.6/78.4	5.87/34.55
Gain (dB)	0	24	53	24

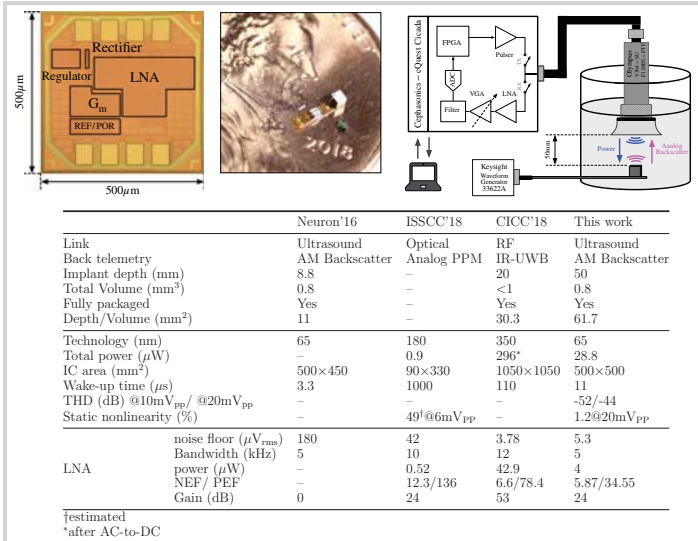†estimated
*after AC-to-DC

Figure 17.5.7: Chip and assembled mote micrograph. In vitro measurement setup and performance comparison table.