# Substrate cooling efficiency during cryogenic ICP polymer etching for diffractive optics on membranes

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## Abstract

We fabricate high-resolution diffractive optics on membranes using a bilayer resist system consisting of HydrogenSilsesQuioxane as a negative e-beam imaging layer and hardbaked AZPN114 as the underlay. To minimize sidewall etching of the polymer, the AZPN114 layer was etched at –100 °C in a cryogenically cooled ICP Etcher. Features fabricated on Si supported membrane wafers, where the areas of interest are separated from the platen by the wafer thickness, provide an additional challenge to the low-temperature dry etch process due to low cooling efficiency (and thus membrane heating). Using cooling theory and experimental verification, we look at membrane cooling efficiency for different hardware and membrane size combinations. Diffusive cooling in membranes less than 140 μm wide maximize membrane cooling during the etch process. With these small membranes we have fabricated high efficiency x-ray zoneplates with linewidths as small as 30 nm and 6:1 aspect ratios.

## I. Introduction

Patterning of sub-100 nm features has become essential for advanced research and development in electronics, optics, and material science applications. At LBNL we use the Nanowriter, an ultra-high resolution 100 keV gaussian electron beam lithography system, to expose electron-sensitive resist materials. In maximizing resolution, we are generally limited to 1:1 resist height-to-width aspect ratios by electron beam/substrate interactions. Dry etching provides a means for overcoming this limitation by allowing lithographically defined patterns to

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be transferred into underlying layers. However, highly anisotropic pattern transfer with minimal sidewall etching rates requires precise substrate temperature control,[1] and low substrate temperatures.[2] Etching that is typically isotropic in ion bombarding type plasmas can be made anisotropic by lowering the substrate temperature. This reduces vertical sidewall etching by reactive radicals relative to lateral surface etching by ion bombardment. Hence, critical dimensions are less compromised. Particularly for oxygen etching of polymers, Tachi *et. al.* [2] showed that the sidewall etching ratio (width/depth) is continually reduced from 0.1 at –20 °C until it is undetectable around –100 °C.

Our etcher, a state-of-the-art ICP dry etch system, achieves temperature control via conductive cooling whereby the wafer is clamped firmly to a liquid nitrogen cooled platen and He gas aids the backside heat conduction. In the He backside pressure regime in which we operate (10-40 mtorr as measured within the platen), increasing the gap between the platen and the etched substrate decreases the cooling effectiveness. Features fabricated on membrane wafers, where the area of interest are separated from the platen by the wafer thickness and thus have reduced cooling efficiency, provide an additional challenge to the low-temperature dry etching process. In the case of high-resolution, high-aspect ratio zoneplate etching, sidewall etching ratios of just five percent will reduce zoneplate focusing efficiency and in the worst case facilitate pattern collapse. In this paper, we describe how we overcome the difficulties of cryogenic etching diffractive optics on membrane wafers, and using a bilayer resist "mold" and electroplating, fabricate efficient, high-resolution diffractive optics with linewidths as small as 30 nm.

**II. Experimental**

Membrane wafers were prepared by depositing 100 nm of LPCVD $Si_3N_4$ on the back and front side of Si wafers. The backside was then patterned and on opening etched into the $Si_3N_4$. Using the remaining $Si_3N_4$ as a mask, the exposed Si was wet etched through the full thickness of a wafer using a hot KOH etch. The front-side $Si_3N_4$ acts as an etch stop and thus becomes a Si supported membrane.

Fig. 1 summarizes the diffractive optic processing using a bilayer process,[3] cryogenic etching, and plating. Plain Si or membrane wafers were coated with 5 nm Ti and 10-12 nm of Ge. Then, these wafers were coated with Sumitomo AZPN114 photoresist. A 30% solution was spun at 2000 rpm on a 4" and hardbaked at 250 °C for 5 minutes producing a 180 nm film. Next, a 1.8% solution of HSQ (Fox-15, Dow Corning, 18% solids) was spun at 2000 rpm and oven baked in glass dish at 170 °C oven for 30 minutes producing a 37 nm film.

The wafers were exposed using a modified Leica VB6HR, the Nanowriter, at 100 keV with 450 pA beam current and 5 nm spot size. The Nanowriter is optimized to provided accurate curvilinear shapes using an LBNL developed pattern generator.[4] Lines were printed at 1:1 and with negative bias. Optimum doses for 30 nm 1:1 lines on Si were approximately 2000 μC/cm2. The wafers were developed in 100% Shipley LDD 26-W for 1min, rinsed in DI water and blown dry.

In the course of this study, we found the HSQ electron sensitivity drifts. At the extreme, we found after 8 months of cold storage, sensitivity improved 400%, but at the expense of resolution. Thus, testing the HSQ sensitivity periodically is critical to insuring repeatable lithographic results.

The AZPN114 was etched in an Oxford Plasmalab 100 ICP 380 etcher. This etcher is equipped with an inductively coupled plasma source, a platen large enough to etch 8" wafers,

and a $LN_2$ cooled platen that can reach temperatures as low as –150 ºC with temperature control of ±1° C. The etching conditions used were 1.5 mtorr pressure, 10 sccm $O_2$, 20 W RF power, 350W ICP power, 15 Torr He on the backside of the wafer and –100 °C for the platen.

Etching rates on blanket wafers showed a rate of 120nm/min for AZPN114, and 1.5 nm/min on HSQ giving a 100:1 selectivity in $O_2$ plasma. For a 180 nm AZPN114 layer, etching time was 1min 20 sec, indicating a slightly higher etching rate on patterned wafers. Before etching, wafers were cooled 5 min on the platen, and after etching, were transferred to a second chamber and warmed to room temperature in vacuum. This warm-up prevents water condensation on cold wafers, and possible resist collapse upon exposure to air. When carrier plates were used, the wafers were attached to the plates with vacuum grease.

After etching, wafers were plated with Ni using a Nickel Sulfate solution (Sulfamex from Enthone-OMI) at 35 °C and a current density of 1 mA/cm2. This results in a plating rate of about 10nm/min. The plating rate has been optimized to give the lowest stress and small grains.

**III. Cryogenic Etching Experiments**

The HSQ bilayer etching process was first developed on a plain silicon wafer. Fig. 2 shows that after etching we were able to fully clear 30 nm lines at a 60nm period, and partially clear 25 nm lines at a 50 nm period. Aspect ratios in this case are better than 6:1. Unbiased isolated lines have been achieved at 16 nm at a 6:1 aspect ratio.

We then transferred the process to a $Si_3N_4$ membrane wafer. Membrane wafers are necessary to allow sufficient x-ray transmission through the patterned optic. In addition, since we are using e-beam lithography for patterning, membranes have the advantage of reducing exposure non-uniformities due to backscatter from the substrate (proximity effects). The test membrane wafer consisted of 3.5 mm square membranes separated by 0.5 inches on a 500 μm

thick 4 inch Silicon wafer. Figure 3a (right) shows the lithographically patterned 40 nm 1:1 lines collapsed and had a high degree of sidewall etching. In trying to improve the cooling between the membrane and the platen, we attempted to fill in the platen-to-membrane gap with various liquid substances which upon cooling produced stress in the membrane causing it to break. We then designed gap reducing carrier plates with 400 μm raised sections (Fig. 3b left), approximately the width of the membrane to reduce the gap between the cold carrier plate and the membrane and hopefully improve the conduction. These plates included He conduction holes. The 3.5 mm membranes etched on a carrier plate showed a marked improvement over membrane wafers etched with no carrier plate (Fig 3b right).

We then conducted several experiments to look the optimum membrane wafer and carrier plate combinations for different membrane sizes and Si wafer thicknesses. In the course of these experiments, we found that our wafer lift mechanism (Fig. 4) was to blame for the poor etching results in Fig. 3a. Any membrane lying above the wafer lift mechanism, which is recessed below the platen surface during etching, had significantly increased sidewall etching rates relative to membranes that were above the platen itself. However, we did not observe a difference in sidewall etch rate between membranes directly over a He feed hole, and those just over the platen. Fortunately, we found a flat carrier plate (without the gap reducing raised section) improved the membrane-to-membrane cooling uniformity over a bare platen by covering over the wafer lift mechanism

Contrary to our expectations, gap reducing carrier plates did not measurably improve the sidewall etching rate over flat carrier plates. Furthermore, we found that 1 cm membranes etched on these gap reducing carrier plates had differing sidewall etching rates of identical features depending on whether the feature was on an area directly above a He transfer hole in the carrier

plate or on a different part of the membrane. This was not consistent with our experiences with the bare platen. To clear up some of these ambiguities we looked more closely at the theory of wafer cooling.

**IV. Substrate Cooling Model**

Parry[5] has analyzed the process of wafer heating during implantation and found good agreement between calculations and experimental conditions. Using this approach and adding a term for lateral conduction, we equate the heat absorbed by the a $Si_3N_4$ membrane to the heat input minus the heat losses and get the following equation (for simplicity we assume a circular membrane area):

$$CAl\rho\frac{\partial T}{\partial t} = PA + \kappa_{SiN}\frac{\partial^2 T}{\partial r^2}2r\pi l - \frac{A\kappa_{He}}{d}(T - T_{wh}) - \alpha A(T^4 - T_{surr}^4) - \beta A(T^4 - T_{wh}^4) \qquad \text{Eqn. 1}$$

where C is the specific heat of the material in J/(g C), A is the area over which it is being heating in $cm^2$, r is the density of the material in $g/cm^3$. T is the temperature of the material being heated, P is the power input from the plasma in J/(s $cm^2$), $\kappa_{SiN}$ is the heat conductivity of silicon nitride in J/(m °C), r is the membrane radius in cm, l is the membrane thickness in cm, $\kappa_{He}$ is the heat conductivity of the He gas responsible for backside cooling, d is the membrane-to-platen gap, $T_{wh}$ is the temperature of the wafer holder, $T_{surr}$ is the temperature of the surroundings above the wafer, and $\alpha$ and $\beta$ are constants which depend on the emmissivities of the wafer and the surroundings or wafer holder.

The term on the left side of the equation accounts for the heat absorption in the material. The first term on the right accounts for the heat input from the plasma; the second term allows for lateral conduction in the membrane to the surrounding silicon; the third term accounts for He heat conduction between the wafer and the wafer holder; the fourth term allows for radiation to

the surroundings and reflection back; and the fifth term allows for radiation the wafer holder and reflection back.

Ignoring radiation effects and solving for the steady state membrane temperature (where the membrane edge is held at the platen temperature), we arrive at an equation that describes the dependence of membrane temperature rise as a function of membrane and gap dimensions:

$$T_{SiN} - T_{wh} = \frac{P}{\frac{l\kappa_{SiN}\pi^2}{R^2} - \frac{\kappa_{He}}{gap}} \qquad \text{Eqn. 2}$$

Figure 5 shows plots of the temperature rise ($T_{SiN}$-$T_{wh}$) versus the membrane radius at 4 gap widths. (A $Si_3N_4$ conductivity of 4 J/(m °C) is used here). From these calculations we can conclude that for 140 μm membrane widths and below, lateral diffusion dominates even at large gap sizes, and the membrane temperature rise is kept below 10 °C. Thus, sidewall etching rates are not significantly increased even at large gap sizes. For moderate gaps and larger membrane sizes, He backside cooling dominates. In this regime, it is important to achieve the smallest gap possible. For both large membranes and larger gaps, as is the case above the wafer lift mechanism, the wafer heating is large. (However, not accounting for radiation, our calculations exaggerate the temperature rise at the largest gap size.) This is why carrier plates improved the cooling for membranes positioned over the wafer lift mechanism. These calculations, however, do not explain why gap reducing carrier plates and flat carrier plates produced similar sidewall etching rates nor why we saw differences between the same sized features etched either over or far away from He transfer holes in the carrier plates. In Eqn. 2, we assumed that we were in a regime where He conductivity was constant (gap larger then He mean free path and higher backside pressures). If our carrier plate design reduces He conductance, we are operating towards the molecular regime where the He conductivity decreases with decreasing pressure.

Decreased conductivity would counteract the gap reduction effects in the gap reducing carrier plate. This needs to be investigated further to improve large membrane cooling efficiency using gap reducing carrier plates.

**V. Etching on small membranes**

We successfully etched a 100 μm thick wafer with 60 μm windows on a bare platen. As shown in Fig. 6., we were able to etch both 30 nm and 40 nm zone plates with 1:1 line to space ratios and 6:1 aspect ratios. As predicted in Fig. 5, diffusion cooling is dominant in small membranes and thus the large backside gap above the wafer lift mechanism is not problematic. Fig. 6c shows images of 40 and 30 nm lines and spaces taken at the LBNL X-Ray Microscope (XRM-1) using a 40 nm line zoneplates. Because of the very high aspect ratios and thus high focusing efficiency, sub-30 nm theoretical resolution was achieved.

**VI. Conclusions**

Using the HSQ bilayer cryogenic etching process, we have successfully produced high aspect ratio, high resolution diffractive optics. Using sub-100 μm membranes, which minimize membrane heating during etching and thus minimizes sidewall etching rates, we fabricated x-ray zoneplates with outerwidths as small as 30 nm and 6:1 aspect ratios. Gaps of 500 μm in combination with millimeter sized membranes gave higher but tolerable sidewall-to-lateral etching ratios. In addition, etching hardware should be chosen carefully so that the membrane to platen gap is uniform across the backside of the wafer. Carrier plates offer a remedy for modifying platens that do not cool uniformly and with careful design for backside pressure and gap may offer a mechanical way to minimize the platen-to-membrane gaps. In the future, we plan to investigate working with plain Si wafers and forming membranes after etching, so that we are working with easily cooled solid wafers during the cryogenic etching process.

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**Figure Captions**

FIG. 1. Diffractive optic fabrication. The gap referred to in the cooling section is shown in C.

FIG. 2. 30 nm lines (top) and 25 nm lines (bottom) etched in 210 nm thick HSQ bilayer on Si. Anisotropic etching proceeds in polymer layer.

FIG. 3. A) Membrane wafer etched directly on the plate. High sidewall etching rates produced thin collapsing lines. Using the gap reducing cooling plate (B), the sidewall etching rate is reduced.

FIG. 4. Platen inside the etching chamber. Wafer lift mechanism is recessed below the platen surface.

FIG. 5. Membrane cooling efficiency. Plots of membrane temperature rise as a function of membrane radius at four membrane-to-platen gaps.

FIG. 6. Top shows 40 nm Ni plated zoneplate. Middle shows 25 nm Ni plated zoneplate resolved to 30 nm lines. Imaging and polymer layer is not yet stripped and there are bridges between the

lines. This bridging is a result of incomplete line resolution in the imaging layer. Bottom shows images from XRM-1 microscope of 40 nm lines (left) and 30nm lines (right) using the 40 nm zoneplate lens.