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Monolithic Mode-Locked Laser and Optical Amplifier for Regenerative Pulsed Optical Clock Recovery

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Abstract—We experimentally demonstrate optical clock recovery using a novel mode-locked laser (MLL) monolithically integrated with an output semiconductor optical amplifier. The laser's mirror placement is determined using lithography, allowing for mode locking and clock recovery at the exact frequency of the design (35.00 GHz), which is easily scalable to 40 GHz or higher. The design is compatible with other photonic integrated circuit components, enabling integrated signal processing with MLLs. The device generates pulses at 35.0-GHz repetition rate with 6-ps pulsewidth, over 12-dB extinction ratio (ER), and 8.3-dBm output power. Among other regenerative capabilities, the device performs optical clock recovery with 50% jitter reduction from a degraded input signal with low ER.

Index Terms—Mode-locked lasers (MLLs), optical fiber communication, optical signal processing, photonic integrated circuits (PICs).

I. INTRODUCTION

MODE-LOCKED lasers (MLLs) can be useful for various applications in optical signal processing, including 3R regeneration and optical time-division multiplexing [1]–[5]. Some qualities of MLLs utilized in optical clock recovery are their ability to perform jitter reduction, pulse reshaping, and amplification [3]–[5]. Since the frequency of mode locking is determined by the cavity length, traditional MLLs with cleaved facets are not reproducible at a specific frequency. It is also desirable to perform integration of MLLs with other components on a single chip for complex photonic integrated circuits (PICs). This could allow for new, high performance, and cost-effective PICs for optical signal processing, such as regeneration.

In this letter, we present an InP MLL monolithically integrated with a semiconductor optical amplifier (SOA) at the output and its application as a regenerative optical clock recovery circuit. The device generates high-quality clock pulses suitable for transmission through fiber or for on-chip processing. The SOA has negligible negative effects on the output

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Color versions of one or more of the figures in this letter are available online at <http://ieeexplore.ieee.org>.

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Fig. 1. Scanning electron micrograph of the device.

pulse quality, while it increases the output power by 10 dB. Optical clock recovery is demonstrated over a 10-dB input signal dynamic range, with retiming and reshaping of degraded input data.

II. DEVICE DESIGN AND FABRICATION

Fig. 1 shows an electron micrograph of the device. The input and output waveguides are curved and flared to reduce reflections. This is critical since reflections back into the MLL can cause instability and disrupt mode locking. From input to output facet, the device is 3.5 mm long. The MLL is a self-colliding pulse design, consisting of a back distributed Bragg reflector (DBR) mirror, a 50- μm saturable absorber (SA), a 550- μm gain section, a 290- μm gain section, a 100- μm phase control section, and a front DBR mirror. The back mirror is 41.5 μm long, resulting in a 90% power reflectivity given a 90-nm etch depth. The front mirror is 15.5 μm , with 40% reflectivity. The output SOA is 550 μm long.

With 10- to 20- μm -long isolation regions between sections, the cavity length between mirrors is 1080 μm . Five hundred $k \cdot \Omega$ of isolation is typical between adjacent sections. Accounting for the effective lengths of the mirrors, which are 10.3 and 6.6 μm , the effective length of the cavity is 1097 μm . The group index was measured from similar previously fabricated lasers to be approximately 3.9. These numbers indicate that the laser cavity should be resonant at 35.06 GHz. Since the bias conditions can be changed to alter the group index in the laser, mode locking can occur over a 300-MHz range. Thus, operation at exactly 35.00 GHz was possible and repeatable in several device designs. During clock recovery, the device has a locking range of 60 to 200 MHz for fixed bias conditions.

The device was fabricated on an InP substrate with InGaAs–InGaAsP offset quantum wells. This allows for selective removal of active regions in passive areas of the device. The epitaxial structure and fabrication process are similar to those described in [6]. This platform also allows for integration with other components including low-loss passive regions,

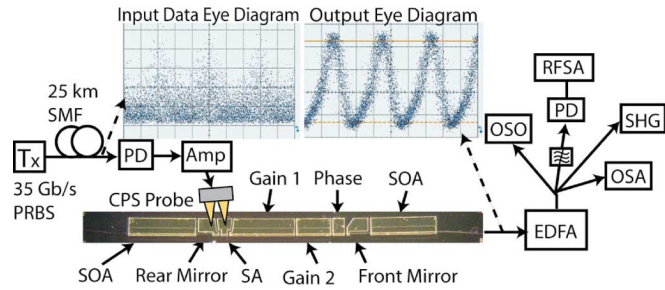


Fig. 2. Experimental setup, with eye diagrams of the input and output signals and photograph of the device. The recovered clock appears to have high jitter because of poor OSO triggering. The actual jitter is 1.14 ps [Fig. 3(d)].

high-speed photodetectors (PDs), electroabsorption modulators, and deeply etched waveguide bends [7]. The output facet was antireflection-coated to reduce reflections.

III. EXPERIMENTAL RESULTS

The experimental setup is shown in Fig. 2. The device was soldered to an AlN carrier and placed on a copper stage cooled to 18 °C using a thermoelectric cooler. The fiber-to-chip coupling loss is estimated to be 4 dB. For testing, hybrid optical clock recovery was performed, meaning the input optical data signal is converted to an electrical signal which modulates the SA section of the MLL. A 35-Gb/s $2^{31} - 1$ pseudorandom binary sequence pattern return-to-zero optical signal was sent to a PD and electrical amplifier. The electrical signal from the amplifier was sent to a coplanar stripline probe placed on the MLL's SA. The optical input power was measured to be -1.5 to 8.5 dBm, resulting in measured electrical powers of 5 – 15 dBm at the SA, limited by saturation of the amplifier for optical input above 5 dBm.

The amplifier is not necessary for clock recovery, but improves the locking range due to the increased power modulating the absorber [Fig. 3(c)]. The input signal was intentionally degraded to test the device's regenerative capabilities. To accomplish this, the input optical signal was passed through 25 km of SMF-28 fiber, resulting in 2.23-ps jitter as measured in Fig. 3(d), and an extinction ratio (ER) less than 3 dB.

Since the device was not specifically designed with top-side n-contacts or optimized for hybrid mode locking, the injection of the electrical data signal in this manner is expected to be very inefficient. With an optimized device, we expect that optical powers below -10 dBm could be used for hybrid mode locking or clock recovery [8], [9]. The output was sent to an erbium-doped fiber amplifier, and then split to an optical sampling oscilloscope (OSO), a second-harmonic-generation (SHG) autocorrelator, an optical spectrum analyzer (OSA), and finally an optical filter connected to a PD and RF spectrum analyzer (RFS).

The laser was biased with the SA at 0 V, long gain section at 72 mA, short gain section at 99 mA, phase section at 10 mA, front SOA at 130 mA, and all other sections open. Fig. 4 shows the RF spectra of the free running device, input signal, and output signal during hybrid clock recovery. The output noise is lower than the input noise, indicating jitter reduction has occurred (discussed later). The weak resonance of the free running device shows that it is not passively mode locked. However, the

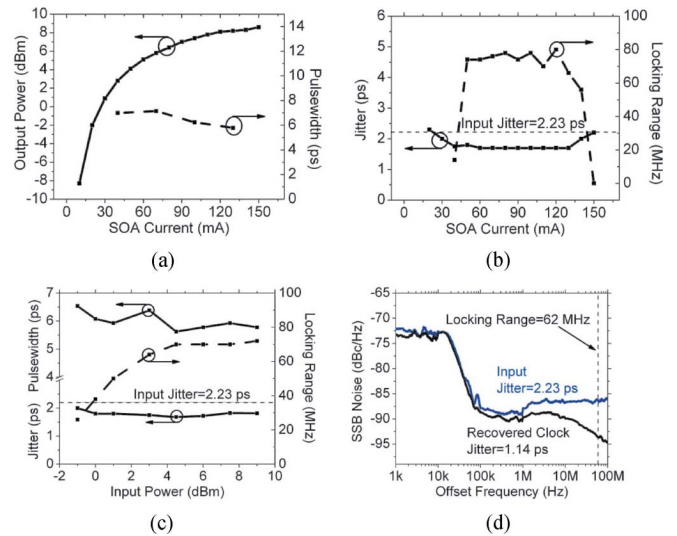


Fig. 3. (a) Output power and pulsetwidth versus SOA current. (b) RMS jitter and locking range versus SOA current. (c) Pulsetwidth, rms jitter, and locking range versus optical input power. (d) SSB noise measurements.

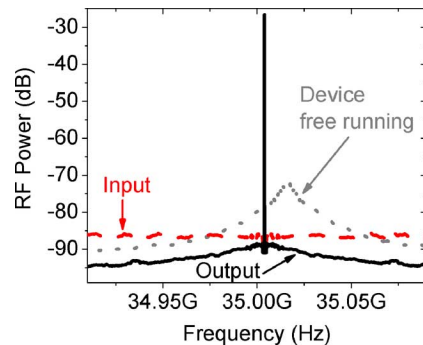


Fig. 4. RF spectrum of the free running device, input data signal, and output of the device. The input and output signal peaks are overlapping: the peak for the input signal is at -29.8 dB and the output signal peak is at -26.7 dB.

additional SA modulation introduced by the input signal induces mode locking [8]. The device can undergo passive mode locking under different bias conditions.

Next we measured the output pulsetwidth of the device, using the SHG, with the resulting autocorrelation pulse shown in Fig. 5(a). This output pulse most closely fits a Gaussian curve, indicating the deconvolved pulse full-width at half-maximum is 6.3 ps for the output and 10.2 ps for the input pulse. The output pulsetwidth can be varied between 3.5 and 8.5 ps by changing the dc bias conditions. In agreement with [9], the shorter pulses more closely fit a sech^2 curve, while the longer pulses were Gaussian. Fig. 5(b) shows the optical spectrum corresponding to the pulse in Fig. 5(a), as measured on an OSA with 0.06-nm resolution. The spectral width is 0.7 nm, so the time bandwidth product is 0.51. The ER was measured by sending the device's output directly to the OSO. It was over 12 dB and this measurement was limited by the power reaching the OSO (the ER increased when the power reaching the OSO was increased, even when all other conditions remained the same). With packets of data injected, the locking time was 800 ps to 3 ns depending on bias conditions, indicating packet clock recovery is possible.

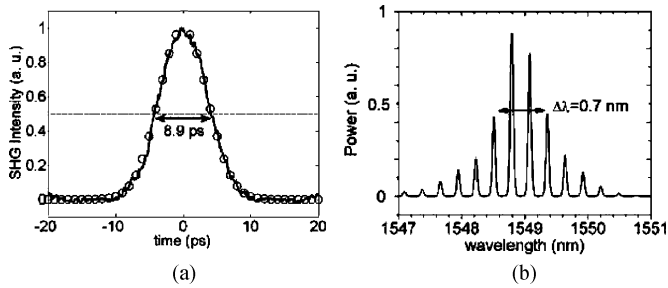


Fig. 5. (a) SHG trace of the output pulses. The solid line is the data and the open circles are a Gaussian fit. (b) Optical spectrum of the output pulses.

Next we tested the effects of the output SOA on the signal quality by applying different currents to the SOA. In these measurements, the device bias conditions were chosen to optimize performance with 130 mA of current on the SOA, and only the SOA current was altered for the different measurements. Fig. 3(a) shows the output power and the pulsewidth versus the SOA current. Fig. 3(b) shows the jitter and locking range as a function of SOA current. The root-mean-square (rms) jitter was measured on an OSO, and the locking range was defined as the frequency range of the injected signal over which the device could generate pulses with less than 2-ps jitter. For biases above 150 mA, the MLL becomes unstable even with optimized bias conditions.

As shown, the characteristics are steady between 40 and 140 mA, except for the output power. The characteristics are also similar to devices without an SOA. As shown in Fig. 3(a), when the SOA is biased at transparency (20 mA), the output power is -2 dBm. When biased at 130 mA, the output power is 8.3 dBm. Thus, the SOA adds 10 dB of power to the signal without noticeably degrading the signal quality. The changes in the pulsewidth, locking range, and jitter are due to the SOA's spontaneous emission entering the MLL and the differences in heat generated by the SOA. As the SOA current changes, the heat and group index in the MLL change. This alters the MLL cavity, causing the changes we observed.

The pulsewidth, jitter, and locking range are also stable over a 10-dB dynamic range in the input power, shown in Fig. 3(c). The input only enters the SA and does not affect other parts of the laser, which contributes to the large dynamic range, as seen in [9]. This is also why input signal degradation will not affect the output pulsewidth or ER. It only affects the MLL's ability to lock to the input, which affects the jitter and locking range. There is very little input wavelength dependence within the C-band, and very low polarization dependence. All-optical clock recovery was also performed using this device [10], with the potential advantage of high-speed operation without a PD [4], [5], but with disadvantages of increased polarization and wavelength sensitivity, and less dynamic range.

As shown in Fig. 3(b) and (c), the output jitter is lower than that of the input. To accurately measure the jitter, we measured

the single sideband (SSB) noise of both signals using an RFSA. Integrating the SSB noise of the traces in Fig. 3(d) from 1 kHz to 100 MHz offset indicates the input jitter is 2.23 ps and the recovered clock jitter is 1.14 ps. Strong jitter reduction occurs in the high-frequency region beyond 60 MHz, outside of the locking range of the device [4]. This shows that the laser is capable of reducing the high-frequency noise of the input signal. The physical mechanism for jitter reduction is explained well in [8].

IV. CONCLUSION

We have demonstrated a novel PIC consisting of an MLL and an output SOA. Lithographic placement of the MLL's DBR mirrors allows for mode locking at the exact frequency of the design, implying manufacturability of MLLs is possible. The output SOA amplifies the output signal by 10 dB without degrading the signal quality. The material platform enables integration of other types of optoelectronic components for complex PICs for optical signal processing. Under hybrid clock recovery, the device has 6.3-ps pulsewidth, an output power of 8.3 dBm, and ER over 12 dB. The output characteristics are consistent for severely degraded input signals and over a 10-dB input power dynamic range. Jitter reduction from 2.23 to 1.14 ps was also demonstrated. The device's excellent regenerative capabilities indicate its potential for 3R applications.

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