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High efficiency mm-wave power amplifier design methodology

A dissertation submitted in partial satisfaction
of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

Kang Ning

Committee in charge:

Professor James Buckwalter, Chair
Professor Mark Rodwell
Professor Upamanyu Madhow
Professor Umesh Mishra

March 2020

The Dissertation of Kang Ning is approved.

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Professor James Buckwalter, Committee Chair

February 2020

High efficiency mm-wave power amplifier design methodology

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by

Kang Ning

To my wife Yuan Ma

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I would like to thank to Prof. Mark Rodwell who taught me courses and taught me how to think the IC design from mm-wave perspective through several projects. Professor also supported me for using the measurement equipment.

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Curriculum Vitæ

Kang Ning

Education

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Publications

1. M. Tanio, K. Ning and J. F. Buckwalter, "A 60-GHz Symmetric Doherty Power Amplifier with 20.4% 6-dB Back-off Efficiency," 2019 49th European Microwave Conference (EuMC), Paris, France, 2019, pp. 559-562.
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3. N. Hosseinzadeh, A. Jain, K. Ning, R. Helkey and J. F. Buckwalter, "A Linear Microwave Electro-Optic Front End With SiGe Distributed Amplifiers and Segmented Silicon Photonic Mach-Zehnder Modulator," in IEEE Transactions on Microwave Theory and Techniques, vol. 67, no. 12, pp. 5446-5458, Dec. 2019.
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7. K. Ning and J. F. Buckwalter, "An 18-dBm, 57 to 85-GHz, 4-stack FET Power Amplifier in 45-nm SOI CMOS," 2018 IEEE/MTT-S International Microwave Symposium - IMS, Philadelphia, PA, 2018, pp. 1453-1456.

Abstract

High efficiency mm-wave power amplifier design methodology

by

Kang Ning

In the demand of high data rate wireless transformation, bandwidth is a expensive resource. Thanks to the modern process that improves the f_t and f_{max} beyond several hundreds gigahertz, the wireless communication could transfer data with wide bandwidth by using mm wave carrier frequency. In the coming fifth generation (5G) wireless communication system that using mm wave band as carrier frequency, the number of base station increases to 3 times or even more comparing to the 4G. And in this system, the most power consumption is dominated by the power amplifier.

This dissertation describes the design methodology of mm wave PA. In order to improve the peak efficiency, an inductive coupling neutralization method is demonstrated in class-B stack FET PA design with measurement result in chapter 3. To improve the average drain efficiency, a constant envelope outphasing PA is described in chapter 4 with showing the limitation on outphasing topology for mm-wave band. To further improve the PAE, a 39GHz CMOS SOI PA is described in chapter 5. For sixth generation (6G), an InP HBT common-base PA with record peak efficiency is demonstrated.

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Chapter 1

Introduction

The 7 billion worldwide mobile subscriptions which include mobile PC, tablets and smart phones are increasing with an average 2% per month. Meanwhile, the data traffic per smart phone is increasing from 3 GB/month in 2017 to 5.6 GB/month in 2018 projecting to 20 GB/month in 2024 [1]. The enormous increasing data demand on wireless communication requires wide frequency bandwidths with efficient modulation schemes that tighten the spectrum, such as higher order quadrature amplitude modulation (QAM) [2]. To address the wide frequency bandwidth requirement and due to the band utilization congestion in the sub 6GHz bands, moving the carrier frequency to mm-wave bands (30-300 GHz) is a promising choice for 5G networks. However, a mm-wave band carrier has lower transportation distance compared to a 4G carrier (sub 6GHz) because of higher free space loss and higher atmospheric gaseous loss. Thus, more base stations need to be set up to fully cover the area and the total power consumption from each base station becomes high. Additionally, QAM signals have high peak to average power ratio (PAPR) and therefore operate the power amplifier(PA) at output power back-off (OBO) most of time. This tremendously reduces the average power efficiency because in a linear class-A PA, the 6dB back-off efficiency is only 1/4 of the peak efficiency.

1.1 Energy Limits on 5G

Determining the number of base stations required for 5G is based on evaluating how far the signal could be transmitted under a certain power level at mm-wave band frequency. The free space loss is defined as:

$$L_{fs} = \left(\frac{4\pi R}{\lambda}\right)^2 \quad (1.1)$$

This equation is the loss from two isotropic antennas where R is the distance between two antennas and λ is the wavelength of carrier signal. Converting to decibels while using kilometers for distance and gigahertz for frequency,

$$L_{fs,dB} = 92.4 + 20\log(freq) + 20\log(R) \quad (1.2)$$

LTE signals are on a carrier frequency of 2.6GHz and the planned mm-wave 5G carrier frequency is 28GHz. This has a free path loss difference as $20\log(28) - 20\log(2.6) = 20.6dB$, in other words, the free space loss from using mm-wave frequency is equal to the loss of 10km transmission distance. In reality, 3G/4G macrocell covers a range of 5-30km, microcell covers 1-2km and the planned 5G cell has only 200-300m coverage distributed through a city. This results at least 3 times of base stations required for 5G compared to 4G to get full coverage for wide signal bandwidth and fast data speed.

Fig. 1.1 shows the atmospherical gaseous loss up to THz frequencies. From the figure, the attenuation from dry air absorption and water vapor at 28GHz is less than 0.2dB/km, negligible for the 5G carrier and make the 28GHz to be a good carrier candidate. The attenuation at 60GHz is about 15dB/km which constrains 60GHz carrier to be a great indoor carrier candidate because the attenuation helps to reduce the in band interference

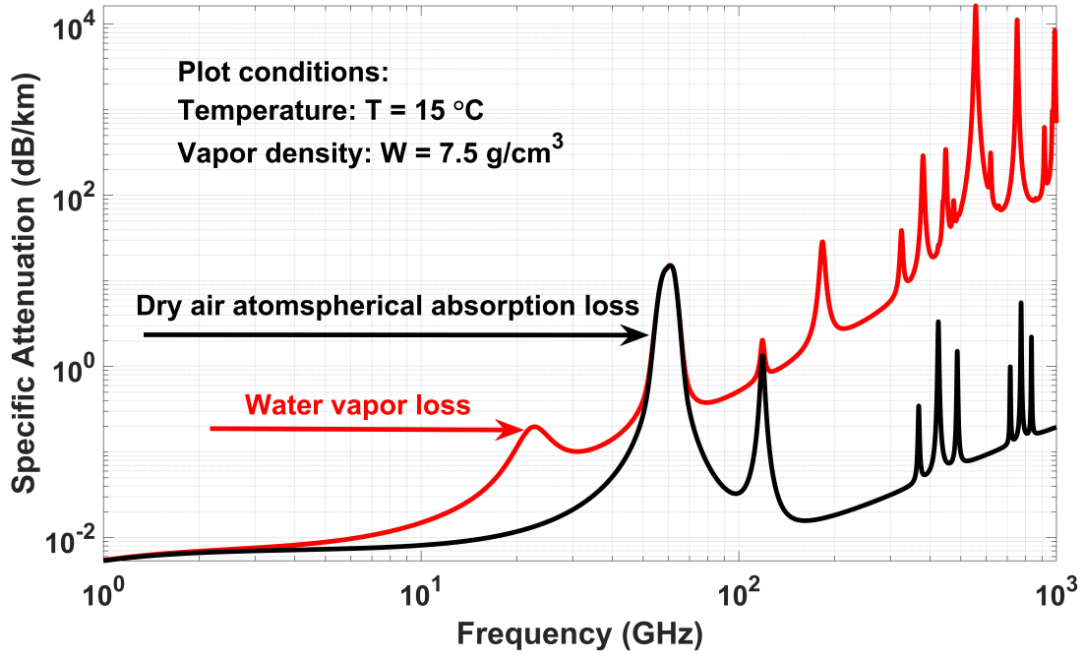


Figure 1.1: Atmospheric gaseous loss up to THz

signals.

To utilize the bandwidth efficiently, QAM signals must be applied. Fig. 1.2 and Fig. 1.3 show the probability density function versus normalized output power for 16QAM and 64QAM signals with root raise cosine filtering. In theory, the peak to average power ratio (PAPR) is 3.7dB for 64QAM but in reality, it's closer to 6dB. These figures demonstrate that at most of the time signals are transmitted they are at 6dB back off from peak output power. The black curve shows an ideal class-B PA power added efficiency (PAE) versus normalized output power. In class-B PA, the drain/collect efficiency (η) drops by half every 6dB power back-off. Therefore, at 6dB back-off, the efficiency is less than 40% although the peak efficiency is 78%. In other words, the average efficiency of PA is much lower than the peak efficiency when using QAM signals. Furthermore, the PAPR could be 12dB when using Orthogonal frequency-division multiplexing (OFDM).

To improve the average efficiency, four main methods were used in the past decades.

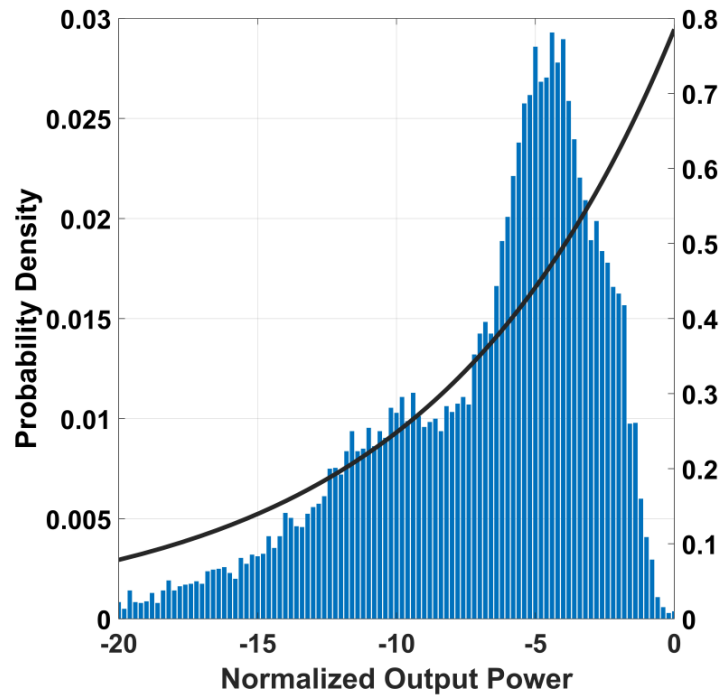


Figure 1.2: PDF versus P_{out} for 16QAM signals comparing to class-B PA PAE

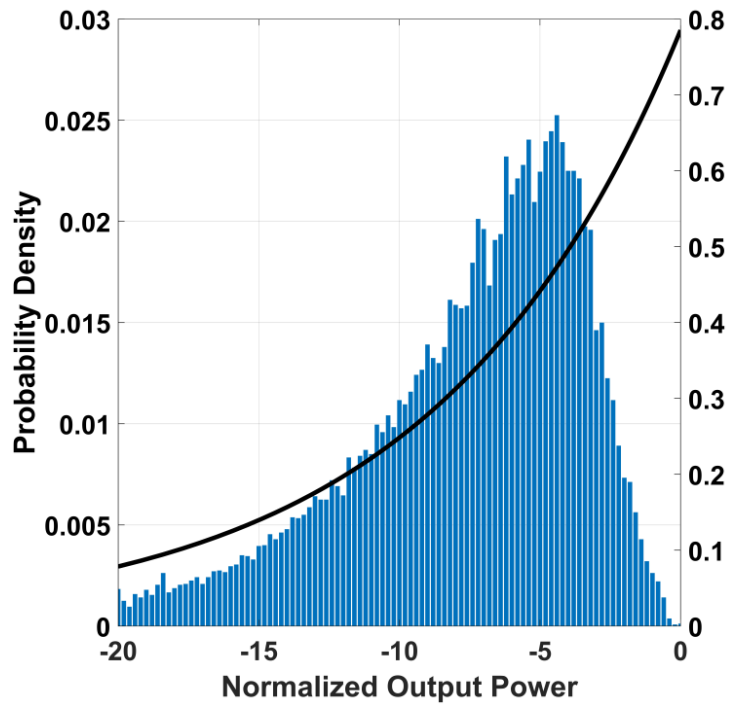


Figure 1.3: PDF versus P_{out} for 64QAM signals comparing to class-B PA PAE

In 1935, H. Chireix proposed an outphasing amplifier which using two identical PAs as a base cell and combined with two phase compensation components, the Chireix's power combiner, to form a high back off efficiency PA [3]. However, two quarter wavelength transmission lines are used in Chireix's power combiner and the loss of the integrated transmission line is very high which detracts from the back-off efficiency heavily. Detailed outphasing theory, design difficulties and solutions at mm-wave band will be addressed in Chapter 4.

In 1936, W.H. Doherty proposed an amplifier that comprised by a main amplifier and an auxiliary amplifier to improve the back off efficiency and linearity of PA [4]. This type of high efficiency PA was widely used in 4G base station. However, this type of PA also uses lengthy transmission lines at the output which reduce the output power and the back off efficiency. A combiner-less Doherty PA is demonstrated in Chapter 5.

Another two types of back-off efficiency improvement PAs are switched capacitor PA and envelope tracking PA. However, switched capacitor PA requires good switching performance from a NMOS and it is very difficult to implement in modern technology at mm-wave band. The envelope tracking PA requires a limiter which can modulate the power source of the PA with the envelope of modulated signals. A high efficiency power source is difficult to design at mm-wave band as well. The theory of the PA operation and the design difficulty are demonstrated in Chapter 2.

This thesis focuses on the peak efficiency and average efficiency improvement in mm-wave PA design.

1.2 Thesis Objectives and Organization

The thesis is organized with demonstrate the PA basics, methods of improving peak efficiency, methods of improving drain efficiency at power back off, and methods of im-

proving power added efficiency at power back off.

Chapter 2 introduces the basic merits of PA in different classes and the design challenge at mm-wave bands. The PAs are demonstrated from efficiency improvement perspective. The following PA designs described in other chapters are based on these fundamentals.

Chapter 3 introduces the design of a 2-stack FET PA at 30 GHz with an inductive coupled neutralization method between drains of two NFET in 45nm SOI CMOS technology. Conventional neutralization methods are discussed and compared to show the pro and cons.

Chapter 4 introduces a constant envelope high back-off drain efficiency (DE) outphasing PA design at 30 GHz. Comparing to conventional Chireix's power combiner, a hybrid mode outphasing PA is implemented with neutralization and unilaterization for removing the impact of device parasitics. The challenge and limitation of outphasing PAs at mm-wave bands are discussed.

Chapter 5 introduces a high back-off power added efficiency (PAE) combiner-less Doherty PA at 37/39 GHz. The current-limited large signal PA model is demonstrated and the simulation results are showed.

Chapter 6 introduces a 120-140 GHz InP HBT common base PA using sub-quarter wavelength balun. A new matching method is demonstrated to improve the load line impedance matching in common base topology and a high efficiency InP HBT PA is designed based on the theory.

Chapter 7 concludes the thesis and discusses future work.

Chapter 2

PA Basics and mm-wave Design Challenge

This chapter introduces the basic concepts and tradeoffs of power amplifier design. In the first section, basic PA cells of class ABCDEFG , envelope tracking PA and switched capacitor PA are discussed. High back-off efficiency PAs, such as outphasing and Doherty architectures, are designed based on two PA cells. Understanding different types of single PA cells is a critical foundation of designing high performance complex PAs. In the second section, the challenges in mm-wave high efficiency PA design are demonstrated from device performance to PA architecture.

2.1 PA Basics (Class ABCDEFG)

The linear, Class-A PA has been widely used in the past. A basic class A PA topology is shown in Fig. 2.1. The load inductor is used to tune out all the capacitances seen at the output drain node that is comprised by device intrinsic parasitics C_{gd} and C_{ds} . If the parasitics are small enough to be negligible, the inductive load could be replaced by a

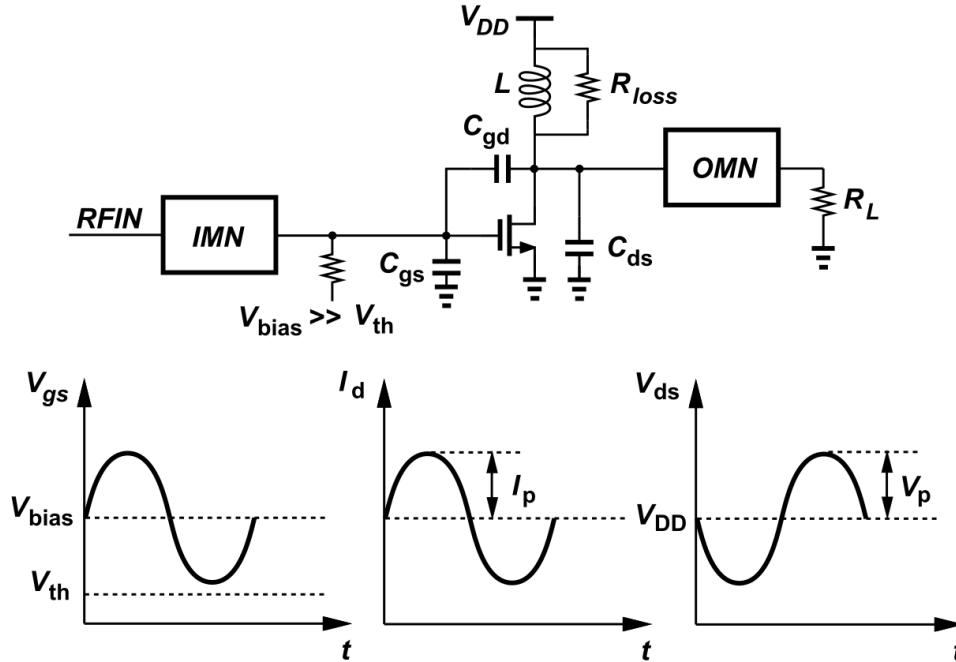


Figure 2.1: Schematic of class A PA

quarter wavelength transmission line as RF choke. The impedance seen from the drain is comprised of the loss from an inductive load, which is typically hundreds of Ohms in modern process, and the load that power is transferred to, normally an antenna of 50Ω .

Loadline theory is a powerful tool to predict the performance of a PA [5]. Fig. 2.2 shows DC-IV curve of an NMOS device driving a load, R_L . The device could provide maximum power with a load Z_{opt} which can be controlled by sizing the transistor in a certain technology. The Z_{opt} does not need to be the same as R_L to transfer high output power. For example, the transistor can be chosen so that it offers a high current and therefore the load impedance could be much smaller than 50Ω for optimum power transfer. An output matching network needs to be designed to match the device load line impedance Z_{opt} to antenna impedance R_L as shown in Fig. 2.1. To simplify the analysis, an assumption is made in the following calculation that the device is sized to have $Z_{opt} = R_L$, the device optimum power load fits the antenna impedance so the output matching network can be

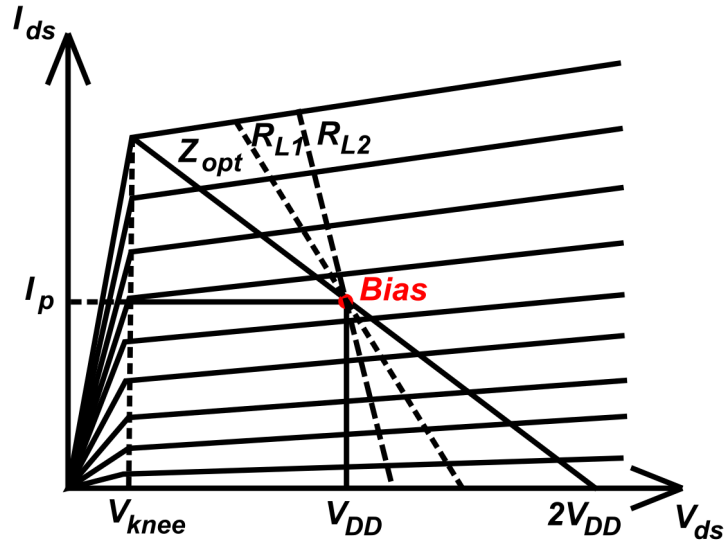


Figure 2.2: I-V curve for NMOS and loadline concept

removed. The maximum voltage amplitude and current amplitude are given by:

$$V_p = V_{DD} - V_{knee} \quad (2.1)$$

$$I_p = V_p / R_L \quad (2.2)$$

then the maximum output power is:

$$P_{sat} = 0.5 * \left(\frac{V_p^2}{R_L} \right) = 0.5 * V_p * I_p \quad (2.3)$$

and the DC power is:

$$P_{DC} = V_{DD} * I_{DC} \cong V_p * I_p \quad (2.4)$$

so the peak drain efficiency η is:

$$\eta = \frac{P_{sat}}{P_{DC}} = 50\% \quad (2.5)$$

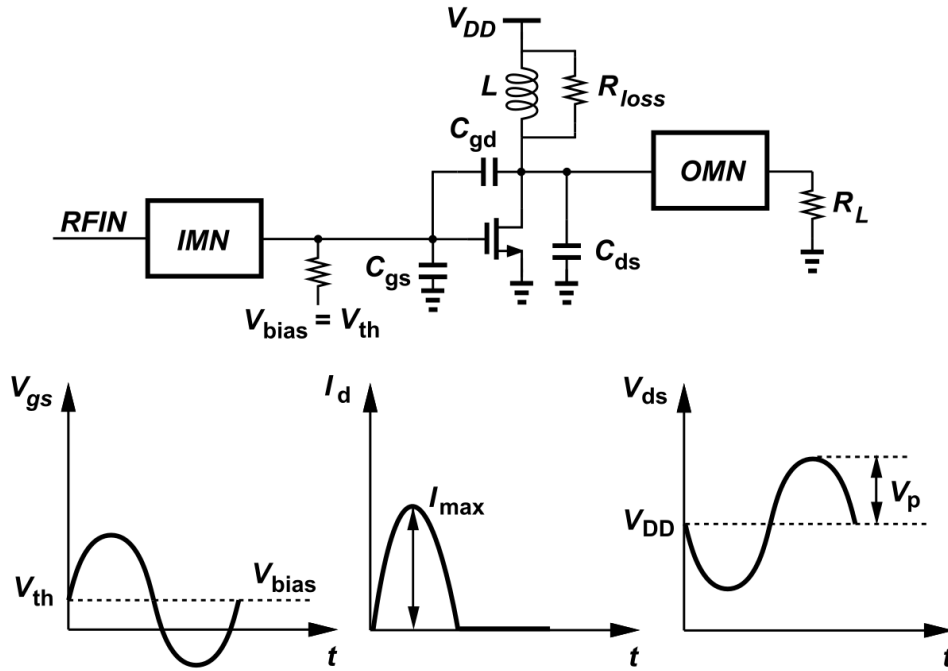


Figure 2.3: Schematic of class B PA

For the power back-off region, replacing the subscript ‘p’, which represents for peak output power to ‘o’ which represents to output power, gives the efficiency as:

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{0.5 * V_o * I_o}{V_p * I_p} = 0.5 * \frac{\frac{V_o^2}{R_L}}{\frac{V_p^2}{R_L}} = 0.5 \left(\frac{V_o}{V_p} \right)^2 \quad (2.6)$$

From the equation. 2.6, if the V_o drops to half of its peak, then the efficiency drops to a quarter of peak η . This corresponds to η dropping to a quarter every 6dB power back-off. The DC power does not change with the output power.

The basic topology of a class-B PA is shown in Fig. 2.3. V_{gs} is biased at the threshold voltage V_{th} . The transistor is turned on for half of the period and turned off for the other half period. The drain current in a half cycle is a cosine waveform and in the other half cycle is zero. Similar to the class A PA, the following derivation assumes NMOS

$Z_{opt} = R_L$. As shown in Fig. 2.4, assume the maximum current is I_{max} . The current waveform can be expressed as:

$$i_D = \begin{cases} I_{max} \cos \omega t & \text{for } -\frac{\pi}{2} < \omega t < \frac{\pi}{2} \\ 0 & \text{for } \frac{\pi}{2} < \omega t < \frac{3\pi}{2} \end{cases} \quad (2.7)$$

Using a Fourier series, the amplitude of the fundamental component in drain current can be calculated as:

$$\begin{aligned} I_{1st} &= \frac{1}{\pi} \int_{-\pi}^{+\pi} i_D \cos \omega t d(\omega t) * \cos \omega t \\ &= \frac{1}{\pi} \int_{-\frac{\pi}{2}}^{+\frac{\pi}{2}} I_{max} \cos^2 \omega t d(\omega t) * \cos \omega t \\ &= \frac{1}{2} I_{max} * \cos \omega t \end{aligned} \quad (2.8)$$

As shown in Fig. 2.4, the V_{DS} swing of class-B PA has an amplitude of $V_{DD} - V_{th}$, the same as the class-A PA. The fundamental voltage and current amplitudes follow the equation:

$$V_p = I_{1st} * R = \frac{1}{2} I_{max} * R \quad (2.9)$$

Comparing to class-A PA, above equation shows $\frac{1}{2} I_{max} = I_p$. So $I_{max} = I_{pp}$. This demonstrates that the fundamental voltage, current waveforms and the loadline impedance in a class-B PA are exactly same as a class-A PA. The loadline of class-B PAs is plotted in Fig. 2.4. The output power of class-B PAs is given by:

$$P_{out} = 0.5 * V_o * I_{1st} = 0.5 * V_o * 0.5 * I_o \quad (2.10)$$

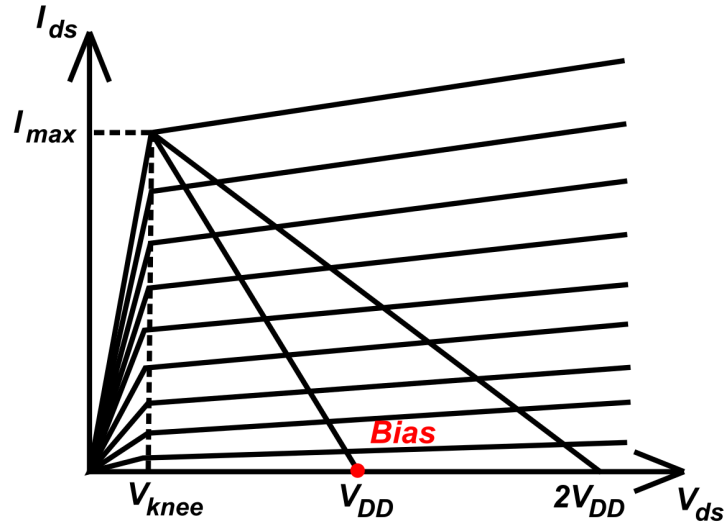


Figure 2.4: I-V curve for NMOS and loadline concept at class-B bias

The DC power can be calculated from average DC current at different power levels:

$$\begin{aligned}
 I_{DC} &= \frac{1}{2\pi} \int_{-\pi}^{+\pi} i_{Dd}(\omega t) \\
 &= \frac{1}{2\pi} \int_{-\frac{\pi}{2}}^{+\frac{\pi}{2}} I_o \cos \omega t d(\omega t) \\
 &= \frac{I_o}{\pi}
 \end{aligned} \tag{2.11}$$

And the DC power consumption is:

$$P_{DC} = V_{DC} * I_{DC} \cong V_p * \frac{I_o}{\pi} \tag{2.12}$$

The drain efficiency could be expressed as:

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{0.25 * V_o * I_o}{V_p * \frac{I_o}{\pi}} = \frac{\pi V_o}{4 V_p} \tag{2.13}$$

From equation. 2.13, the maximum η is $\pi/4 = 78.5\%$ at $V_o = V_p$. For 6dB power back off, output voltage becomes to half of the V_p , and the efficiency drops to $0.5 * 78.5\% \cong 39\%$.

This shows that η drops to half for every 6dB power back-off and the DC power changes with the output power. Compared to the class-A PA, the class-B PA has the same output power but smaller DC power consumption. This is a direct trade off between linearity and efficiency. In fact, high efficiency comes from non-linearity.

Reviewing Fig. 2.1 and Fig. 2.3, for class-A PA, the output current has a full sine waveform and for class-B PA, only half the cycle is sine waveform. Conduction angle is introduced to describe the bias condition. In a class-A PA, the transistor is biased far beyond threshold voltage V_{th} , the transistor is always on for the whole period and the conduction angle is 360° . Looking at the class-B PA, the transistor is turned on only half of the period, so the conduction angle is 180° . In a class-C PA, the transistor is biased less than V_{th} , so the conduction angle 2θ is less than 180° . The schematic, voltage and current waveforms for class C biasing are shown in Fig. 2.5. The DC current and RF current could be found [5]:

$$I_{DC} = \frac{I_{max}}{2\pi} \frac{2\sin(\theta/2) - \theta\cos(\theta/2)}{1 - \cos(\theta/2)} \quad (2.14)$$

$$I_{1st} = \frac{I_{max}}{2\pi} \frac{\theta - \sin\theta}{1 - \cos(\theta/2)} \quad (2.15)$$

Similar to the class-B derivation, the DC power consumption is:

$$\begin{aligned} P_{DC} &= V_{DC} * I_{DC} \\ &\cong V_p * \frac{I_{max}}{2\pi} \frac{2\sin(\theta/2) - \theta\cos(\theta/2)}{1 - \cos(\theta/2)} \end{aligned} \quad (2.16)$$

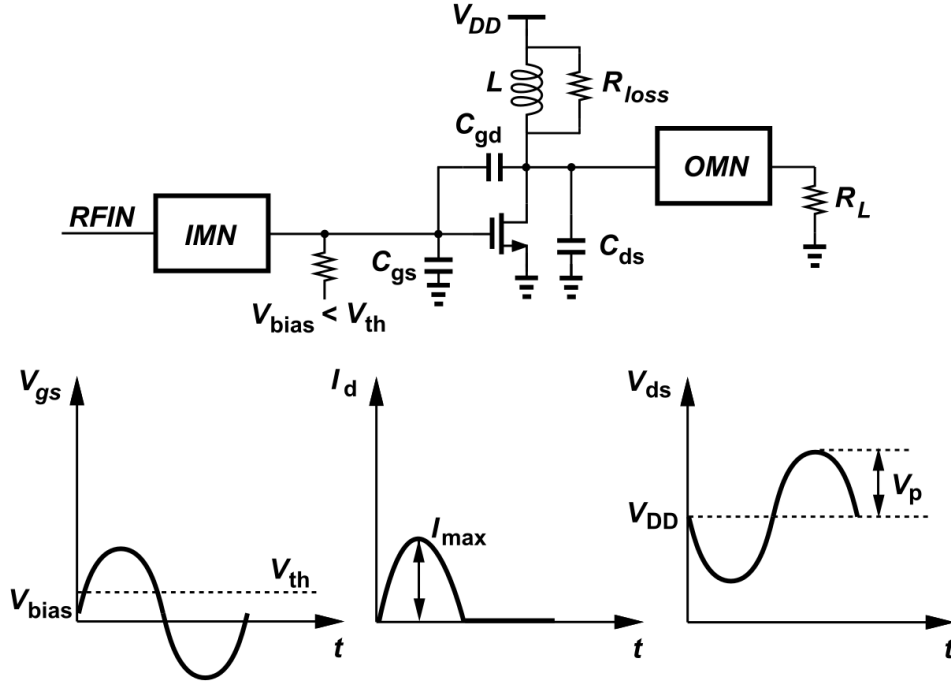


Figure 2.5: Schematic of class C PA

and the output power is:

$$\begin{aligned}
 P_{out} &= (1/2)V_o * I_{1st} \\
 &= 0.5 * V_o * \frac{I_{max}}{2\pi} \frac{\theta - \sin\theta}{1 - \cos(\theta/2)}
 \end{aligned} \tag{2.17}$$

so the efficiency is:

$$\begin{aligned}
 \eta &= \frac{P_{out}}{P_{DC}} \\
 &= 0.5 * \left(\frac{V_o}{V_p}\right) * \frac{\theta - \sin\theta}{2\sin(\theta/2) - \theta\cos(\theta/2)}
 \end{aligned} \tag{2.18}$$

Theoretically, the η of a class C PA could be 100% when $\theta = 0$, however, no current and therefore no output power are transferred to the load. One interesting thing about the class-C PA is that the efficiency at back off also falls to half for every 6dB of power back-off. This is the same as class-B with different peak efficiency.

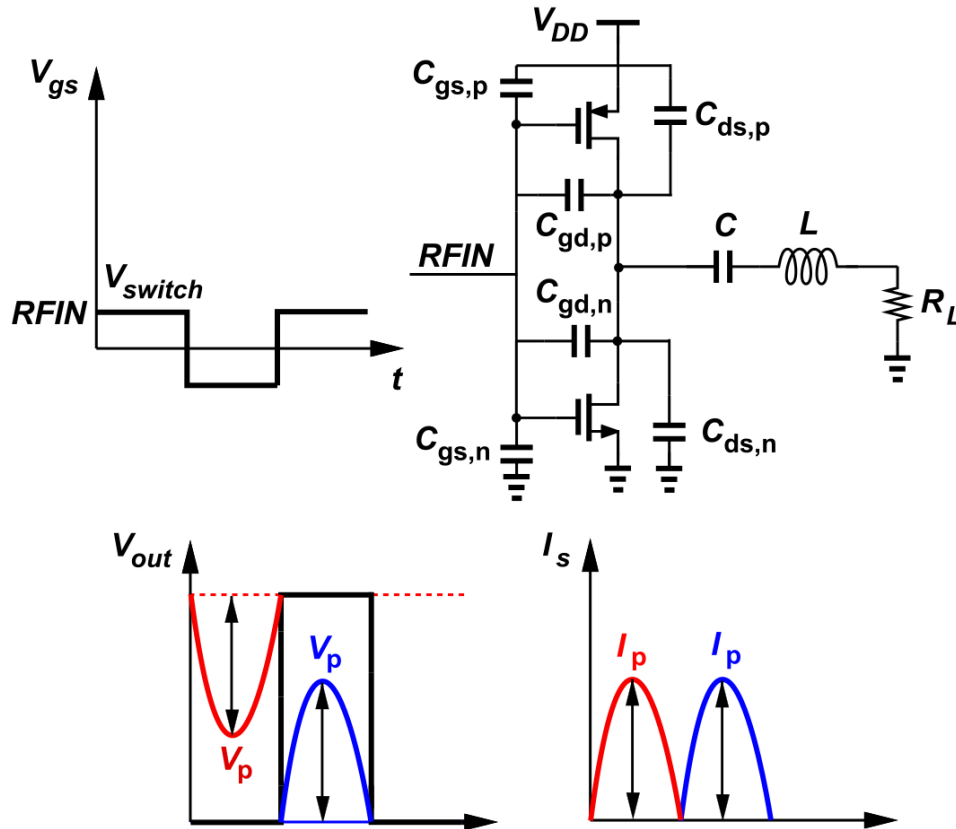


Figure 2.6: Schematic of class D PA

A lot of research has been done on class-D and class-E PA which are recognized as switching PAs, shown in Fig. 2.6 and Fig. 2.7. The input signal of switching PA is a sequence of bits, using the voltage waveform on the gate of NMOS as in digital circuits. In a class-D PA, a NMOS and a PMOS pulls down or pulls up the output voltage to follow the input signals. Normally, the NMOS and PMOS are sized to have equal speed in terms of transconductance G_m . Ideally, the output voltage and current waveforms are non-overlapped as shown in Fig. 2.6. As a result, there is no power consumption on the transistor and all the DC power is turned to RF output power. However, this RF power has abundant harmonics. In other words, although the DC to RF efficiency is 100%, the DC to RF fundamental is 82%.

In class-E PA, a series L-C resonant circuit is added at the output to ensure zero voltage

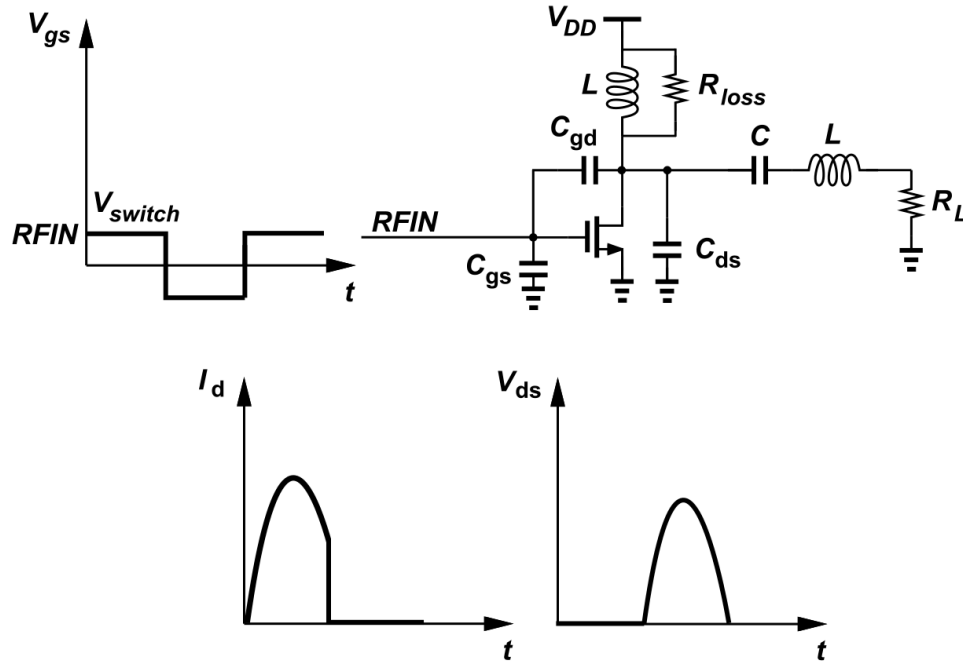


Figure 2.7: Schematic of class E PA

switching (ZVS) or zero current switching (ZCS) and zero-derivative switching (ZDS) conditions for efficiency improvement [6].

Although the switching power amplifiers provide the highest theoretical 100% DC to RF efficiency with good gain, the prerequisite condition of switching PA is that input signal should be the square wave. This requires the prior circuit block to provide abundant harmonics to form the sequence of bits. At mm-wave frequency, the fundamental frequency could be 28GHz and generating even 3rd order harmonics is very challenge.

Class-F or inverse class-F is another set of power amplifiers take the advantage of harmonics waveform shaping. Recent work [7–11] has shown 43% PAE at 39-42GHz using $0.13 \mu m$ SiGe Technology. This harmonic control techniques could be used at mm-wave design. As shown in Fig. 2.8, the class-F PA is comprised of a class-B biased NMOS with a series odd order harmonic tanks at the output. The inverse class-F PA is similar to class-F PA while using the even order harmonics at the output. Harmonic tanks present

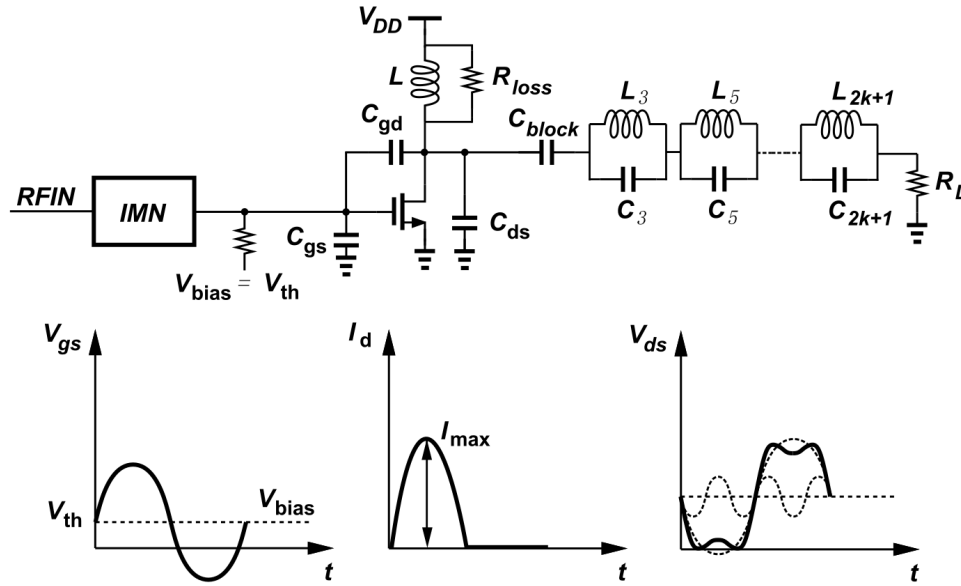


Figure 2.8: Schematic of class F PA

an open circuit or very high impedance at harmonic frequencies which block the current at harmonics from flowing to the load and help to hold the voltage waveform at harmonic frequencies. Thus, a square wave like output voltage waveform is achieved. As shown in the waveform plot of Fig. 2.8, which adds the third order harmonics on the fundamental signal, the output voltage waveform V_{ds} is shaped to have less overlap with the drain current I_d to reduce the DC power consumption and improve the efficiency. Harmonics comes from the class-B bias which for the output voltage waveform could be expanded as [6]:

$$v_{DS} = V_p - V_m \cos \omega t + \sum_{n=3,5,7}^{\infty} V_{mn} \cos n \omega t \quad (2.19)$$

Switching signals also could be added at the gate of the NMOS to provide more harmonics for the design. Theoretically, infinite harmonic tanks could be added in series at the output. Again, at mm-wave bands, design and control high order harmonics are very challenge and usually the harmonics are controlled up to 3rd order.

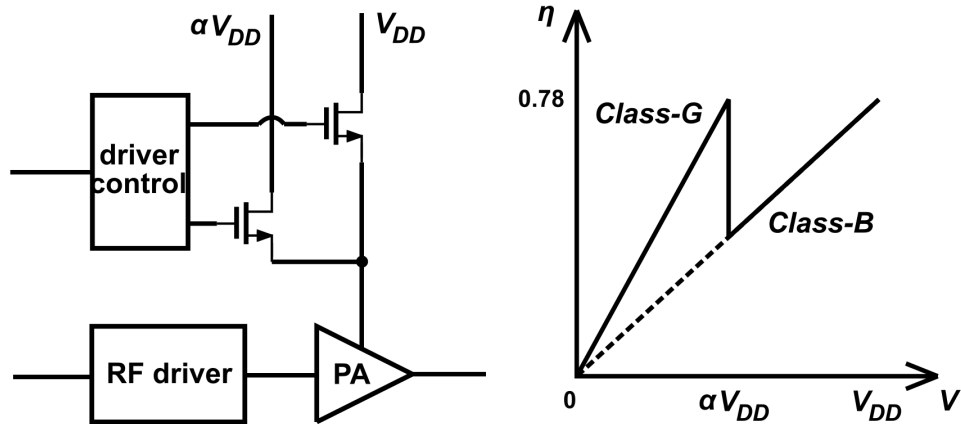


Figure 2.9: Schematic of class G PA

The basic PA cells that have been discussed so far can also be used in a more complex PA topology to achieve better linearity or efficiency improvements. A re-plot of a class-G modulator for PA in [12] is shown in Fig. 2.9. The class-G PA is comprised by a class-B PA with a supply modulator. To transmit a small power signal, the lower supply is turned on and higher supply is turned off to provide low or moderate output power. At larger output power ranges, the PA supply is switched to a high voltage. In both cases, the circuit could reach similar peak efficiency. Thus, the class-G could not only maintain high efficiency at peak output power, but also at power back off range. This technique is used to improve the average efficiency. However, a glitch on the power supply requires additional calibration circuitry to assure the output power from the high power supply and low power supply are same at the switching point. Additionally, reference [13] shows that the switching glitches would increase the white noise and reduce the SNR of the transmitted output signal.

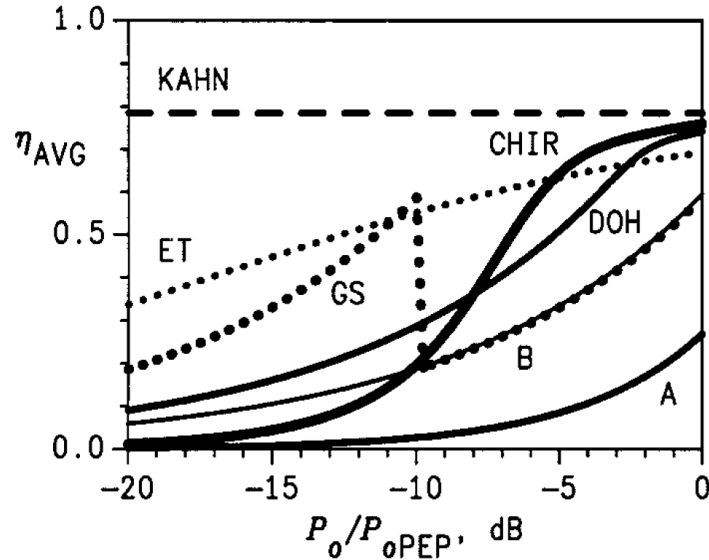


Figure 2.10: Efficiency vs output power for different PA topologies

2.2 High linearity and high average efficiency PA

As demonstrated in the chapter 1, due to the limitation of expensive spectrum resources, complex modulation as QAM or OFDM are used to improve the usage efficiency of a frequency band. These signals have very large peak to average power ratio (PAPR) and leave two expectation on PA performance:

1. The PA could transmit high output power.
2. The PA could maintain high efficiency at power back-off.

Since the PAPR is usually around 6dB in QAM signal and about 12dB in OFDM, different PA topologies such as Doherty, outphasing, switched capacitor, and envelope elimination and restoration (EER) power amplifiers have been proposed in the past to improve the 6 or 12 dB output power back-off (OBO) [14]. A reprint figure of efficiency comparison of these topologies are shown in Fig. 2.10.

In this section, switched capacitor PAs and EER PAs are introduced with their

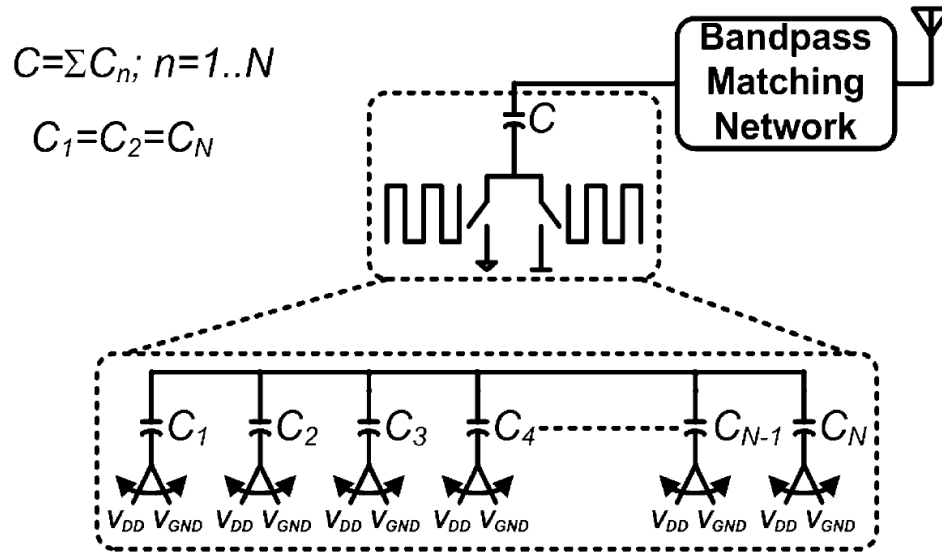


Figure 2.11: Schematic of class SCPA

limitations. In Chapter 4, conventional and new outphasing PAs are discussed, with Chapter 5 covering conventional and new Doherty PAs.

The topology of a switched capacitor PA (SCPA) is shown in Fig. 2.11 [15]; a bank of switched capacitors comprise the PA. The baseband digital signal bits control which switches are active and which are not. The output power level decides the number of switches that should be driving the load with direct power combining as shown in Fig. 2.12. The remarkable characteristic feature of the SCPA is that the back-off efficiency is much higher comparing to a linear PA. As shown in Fig. 2.13, a reprint from [15], at 6dB back-off, the PAE is 1.4 times higher than a class-B PA. And unlike Doherty PA or outphasing PA, the SCPA can cover a larger back-off range such that at 12dB back-off, the PAE is 2.8 times higher if the load has high Q.

An envelope elimination and restoration power amplifier (EER PA) is shown in Fig. 2.14 that reprints from [14]. The concept is to split the signal paths of phase modulation and amplitude modulation. The phase modulated signal flows through a high efficiency non-linear PA (class-C as first proposed but any basic type could be used). The amplitude

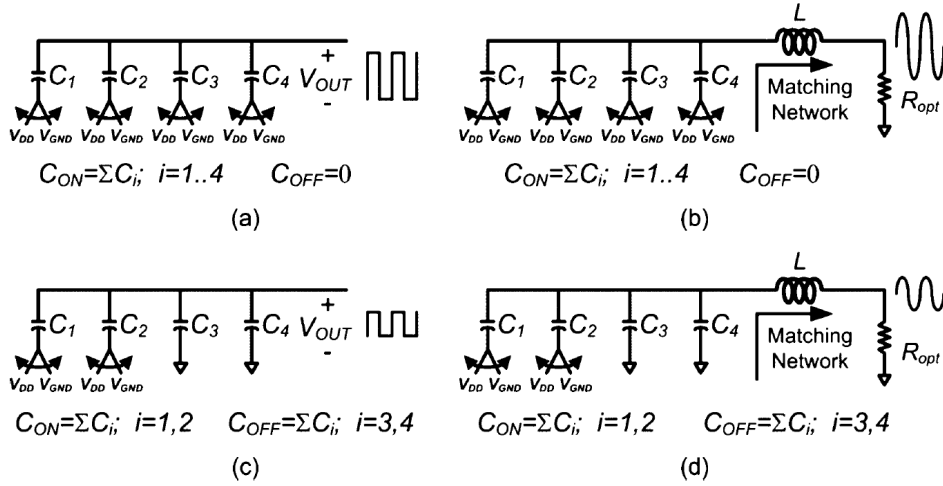


Figure 2.12: Power combining of SCPA

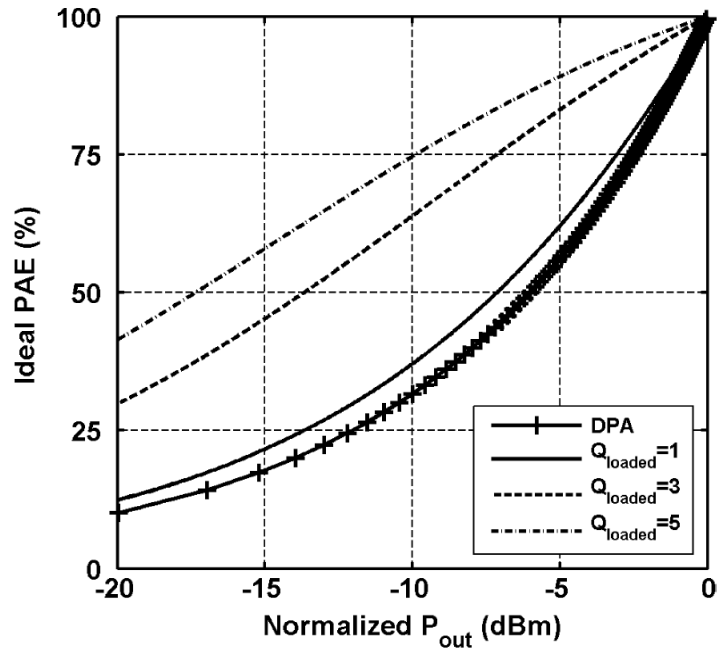


Figure 2.13: Efficiency of SCPA comparing to digital PA (DPA)

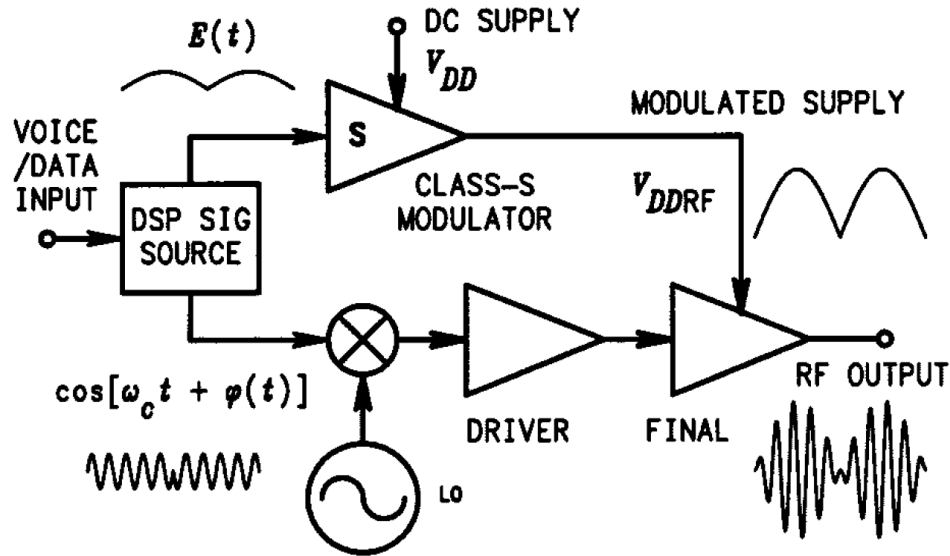


Figure 2.14: Topology of EER PA

signal is amplified with a high efficient digital to analog converter (DAC). The modulated RF amplitude signal is used as the supply of the non-linear PA and this combines the amplitude and phase signal to restore the original signal. Moving the carrier frequency to the mm-wave bands, the requirement on wide baseband signal makes high efficiency EER PAs more difficult to design because of the wide bandwidth of the envelope signal and the high accuracy alignment requirement on the amplitude and phase for signal restoration. Additionally, the efficiency of the amplitude amplifier or DAC drops with increased bandwidth. As a result the efficiency benefits are limited.

Based on the above discussion, several PA basic cells or topologies are not preferred at mm-wave band due to their use of switches (class-E, class-G, switches capacitor PA) and the EER PA becomes more challenge on wide bandwidth designs while also improving efficiency. Since the high efficiency comes from non-linearity which could change the DC power consumption, the usage of non-linearity based high PAE PAs is a better choice for the mm-wave bands. Based on this conclusion, the class-B, class-C, class-F PAs and topologies that combine non-linear PAs such as outphasing and Doherty PAs need to be

investigated to further improve the peak efficiency and average efficiency. In the next Chapter, peak efficiency improvement techniques are discussed.

Chapter 3

Peak Efficiency Improvement PA Design

Peak efficiency is a critical merit of the PA. As demonstrated in chapter 2, the complex PA such as outphasing PA and doherty PA are based on the combination of basic PA cells. The peak efficiency of the PA is the ceiling of the possible solution or combinations. In order to find the possible solution to improve the PAE, the factors that may affect the PAE should be carefully studied. PAE could be formulated as:

$$\begin{aligned} PAE &= \frac{P_{out} - P_{in}}{P_{DC}} \\ &= P_{out} \frac{1 - 1/Gain}{P_{DC}} \end{aligned} \tag{3.1}$$

The output power P_{out} is limited by the fundamental voltage swing and current swing for a certain device. The voltage swing is limited by the breakdown voltage and the current swing is limited by the size of the transistor. Gain is limited by the MAG and the parasitics of device. DC power consumption is limited by the output voltage and current waveform shape and overlapping condition. For a certain process, the breakdown

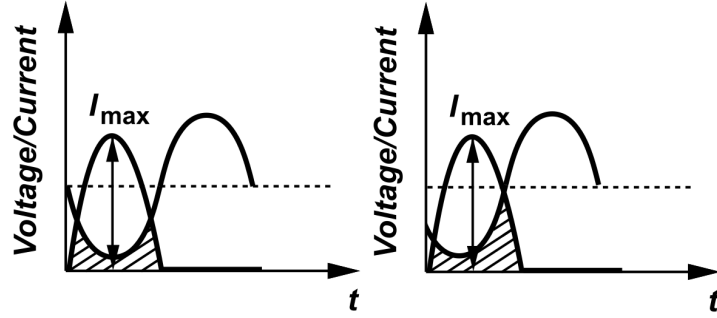


Figure 3.1: Voltage and current waveform relative shift due to the parasitics

voltage is fixed and based on the output power requirement and this breakdown voltage, the fundamental current swing could be calculated by:

$$I_p = \frac{2 * P_{sat}}{V_p} \quad (3.2)$$

The size of the device could be estimated from I_p . In order to improve the efficiency, either increasing *Gain* or decreasing DC power consumption P_{DC} techniques should be used. In theoretical class-B PA, P_{DC} depends on the output power level. However, in reality the transistor is hardly to cut off even biased below the V_{th} . Also because of the parasitics such as C_{gd} , C_{ds} and routing inductance and capacitance, the output voltage and current waveforms are not 180° out of phase. So the DC power consumption is higher comparing to theoretical result as shown in the Fig. 3.1.

Fig. 3.2 shows maximum available gain (MAG) of a $240\mu m$ NMOS with and without C_{gd} de-embedding. In the comparison, a negative equal amount capacitor with C_{gd} is added in between gate and drain. From the comparison, the MAG with neutralization is higher than MAG without neutralization in all band. Specifically, at 30 GHz, the MAG with neutralization is 21 dB, 7 dB higher than the MAG without neutralization. This not only improves gain, but also helps to reduce the DC power consumption and increasing the PAE.

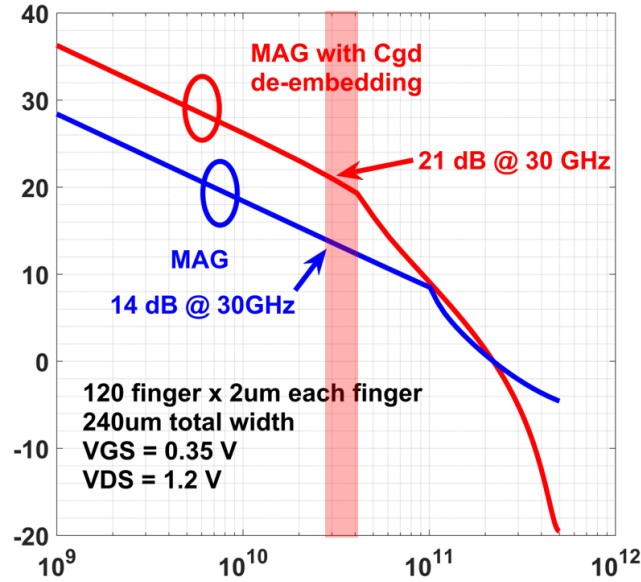


Figure 3.2: Comparison of 240 μm NMOS MAG under with neutralization and without neutralization conditions in GF 45nm SOI RF technology

Different methods of handling the parasitics are proposed in the past. In section 3.1, two state of art design are shown to demonstrate the parasitic handling strategy.

3.1 State of art on high efficiency power amplifier design

In [16], a drain to gate inductive coupling was presented as shown in the reprint Fig. 3.3. The coupling between drain load inductor and the gate input matching network inductor introduces a mutual current that injected into the drain node to compensate the current flow through the C_{gd} and injected into drain node. With correct coupling direction and the proper coupling coefficient, the mutual current could be adjusted to partially, fully or over compensate the C_{gd} and form a neutralization. In this work, a 15.8dB gain, 15.6dBm P_{sat} output power PA with 41% peak PAE was designed with 65nm CMOS.

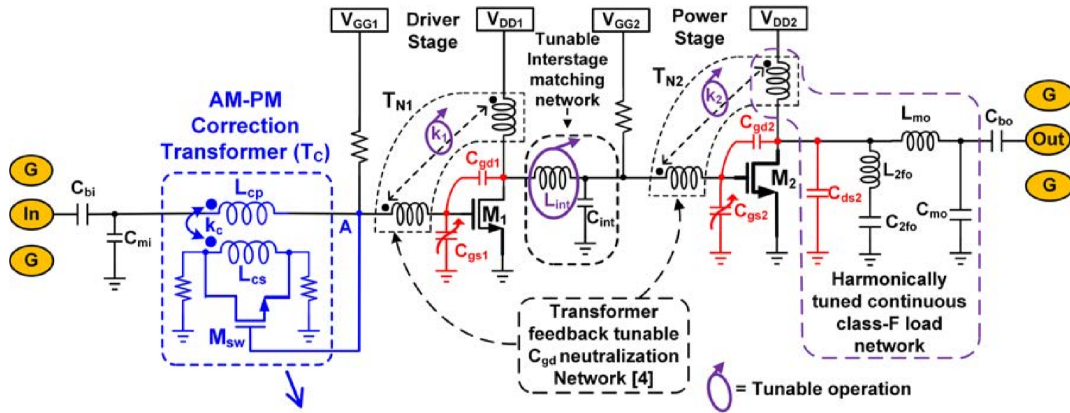


Figure 3.3: Schematic of the drain to gate inductive coupling neutralization power amplifier

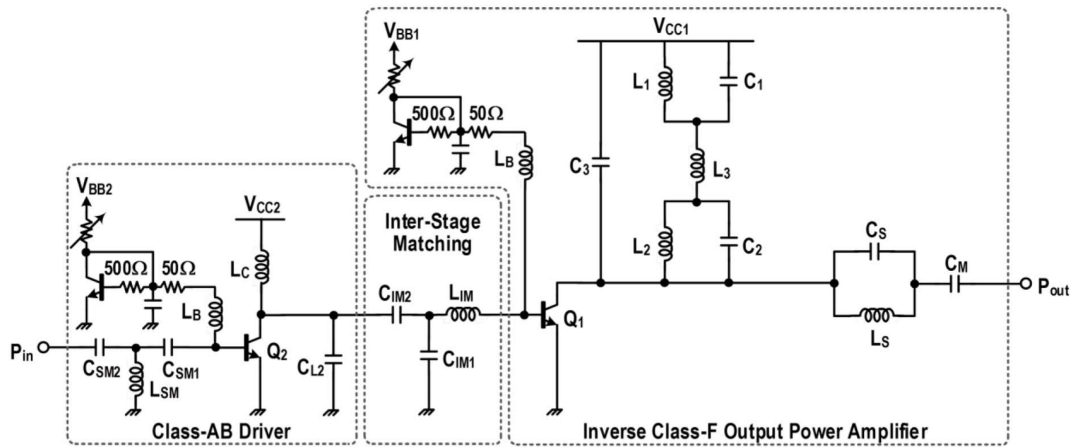


Figure 3.4: Schematic of the inverse class-F power amplifier

The high gain actually from two stage of the design. The neutralization contributes the peak efficiency improvement.

Another example of the high efficiency power amplifier design at mm-wave band is in [10]. The reprinted schematic is shown in Fig. 3.4. The design achieves 18dBm P_{sat} output power and 50% PAE at 24GHz and 16.5dBm P_{sat} output power and 38.5% PAE at 38GHz with $0.13\mu m$ SiGe process. In this design, a complex harmonic tuning network is designed in as the collector load. The harmonic tanks ensure that the impedance seeing into collector load is high at both fundamental and the second order harmonic but low

at the third order harmonic. Two disadvantages in the waveform shaping PA is that: to use inverse class-F or class-F is strongly dependent to the process so it's more difficult to migrate from technology to technology and the complex harmonic tanks make the topology more difficult to use at higher frequencies where the required inductor sizing in tank need to be much smaller and more difficult to implement.

Based on the above review, one take is that although class-F like waveform shaping PA is very attractive and could reach high efficiency at 38GHz, it's may not proper for the higher band high efficiency PA design. Also, the neutralization is very helpful for the gain and PAE improvement.

3.2 Conventional neutralization methods

Conventionally four neutralization methods are shown in the Fig. 3.5. The first method is shown in Fig. 3.5a, a cross coupled capacitor pair is attached to a differential pair for the neutralization. Assume the differential pair could provide a voltage gain as $-A$ and the input voltage amplitude is $\pm V_{in}$. So the output voltage amplitude could be calculated as $\mp V_{out} = -A * \pm V_{in}$. The current injected to the positive output drain node through C_{gd} is:

$$\begin{aligned}
 I_{gd} &= \frac{-V_{in} - V_{out}}{\frac{1}{sC_{gd}}} \\
 &= (-V_{in} - AV_{in})sC_{gd} \\
 &= -(1 + A)V_{in}sC_{gd}
 \end{aligned} \tag{3.3}$$

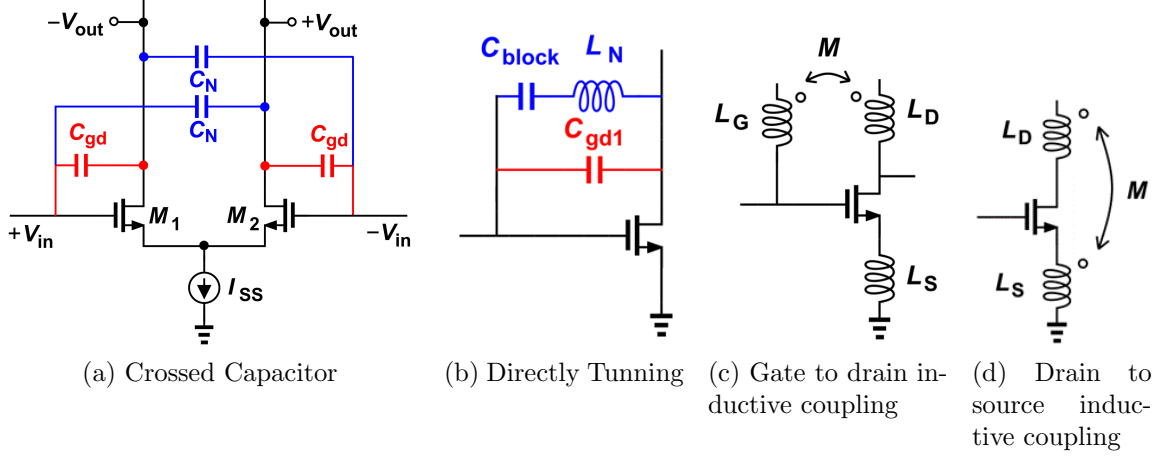


Figure 3.5: Conventional neutralization techniques

and the current injected to the positive output drain node through C_N is:

$$\begin{aligned}
 I_N &= \frac{V_{in} - V_{out}}{\frac{1}{sC_N}} \\
 &= (V_{in} - AV_{in})sC_N \\
 &= -(A - 1)V_{in}sC_N
 \end{aligned} \tag{3.4}$$

It is obvious that the I_{gd} is not equal to I_N . If A is large enough and C_N is chosen to be equal to C_{gd} , the compensation current I_N is very close to the current I_{gd} and the effective C_N closely compensates the C_{gd} . However, in the modern technology at mm-wave band, the voltage gain is usually 6-15dB. Even for 15dB gain, numerically it's less than 6. So the current ratio is: $I_N/I_{gd} = 5/7$. The C_{gd} is partially compensated. If the C_N is chosen to be larger than C_{gd} to effectively fully compensating the C_{gd} at fundamental frequency, then at smaller frequency where gain is higher, the C_{gd} is over compensated and it will cause instability. In other words, the good neutralization results from using the cross coupled capacitor pair based on the prerequisite condition of high gain from differential pair. Another disadvantage is the requirement of choosing the differential signals.

The second method is to use an inductor directly tune out the C_{gd} at the fundamental frequency as shown in Fig. 3.5b. The advantage of this method is that this is the best solution to fully compensate the C_{gd} at a certain frequency. However, there are two disadvantages in using inductor tuning:

1. At lower frequency, the inductor forms a low impedance feedback path which might lead to unstable.
2. For smaller device, the inductor sizing may be too large to design in the real implementation.

The third method is to use gate and drain inductive coupling to generate a mutual current for C_{gd} compensation as shown in Fig. 3.5c. The advantage of using this method is that the drain load inductor and gate matching network inductor are re-used in the compensation circuit, it helps to squeeze the size of layout. However, there are two disadvantages in using gate to drain inductive coupling:

1. For modern process, the coupling coefficient of the transformer is usually less than 0.5. This means the mutual current may be not strong enough to fully compensate the C_{gd} .
2. To form a feed back path with using this type of neutralization, single FET should be used in design. However, in deep sub-micron CMOS technology, if the size of NMOS is too large, then the load line impedance is too low comparing to 50Ω , a high impedance transformation ratio matching circuit is required. If the size of the NMOS not large enough, the output power is low because the breakdown voltage is as low as 1V. So the output power is constrained. In other words, the single FET topology constrains the output power.

The fourth method is to use a drain and source inductive coupling to generate a mutual current for C_{out} compensation. This method is similar to the third method. Besides, it has another disadvantage that source degeneration topology deducts the gain which

eventually hurts the PAE.

As a conclusion, the above methods have different disadvantage and trade-off must be made when design a certain specification PA.

3.3 Implementation of inductive coupled neutralization PA

To achieve high output power while maintain high efficiency, another idea is to use stack-FET PA design [17] combining with the neutralization. Fig. 3.6 shows a close look at the operation of the drain to source neutralization. At very low frequency, the affect from parasitics such as C_{gd} is negligible. So the output voltage waveform is 180° degree out of phase to the input voltage waveform. Since the phase of drain current I_d is same to the input voltage waveform, the I_d is also 180° degree out of phase with the output voltage waveform and the relation of the current and voltage at drain node could be written as:

$$V_d e^{j\theta} = I_d e^{j\theta + \pi} * R_L \quad (3.5)$$

At higher frequency, due to the voltage difference at the input and output, a current is injected to the output and the current and voltage could be written as:

$$V_d e^{j\Theta} = (I_d e^{j\theta + \pi} + I_{gd} e^{j\psi}) * R_L \quad (3.6)$$

From the equation 3.6, the output voltage V_d and drain current I_d are not 180° degree out of phase. This increases the overlapping between the output voltage and current waveforms and increasing the DC power consumption. The inductive coupling between the drain inductor and source inductor could bring a mutual current that in the reverse

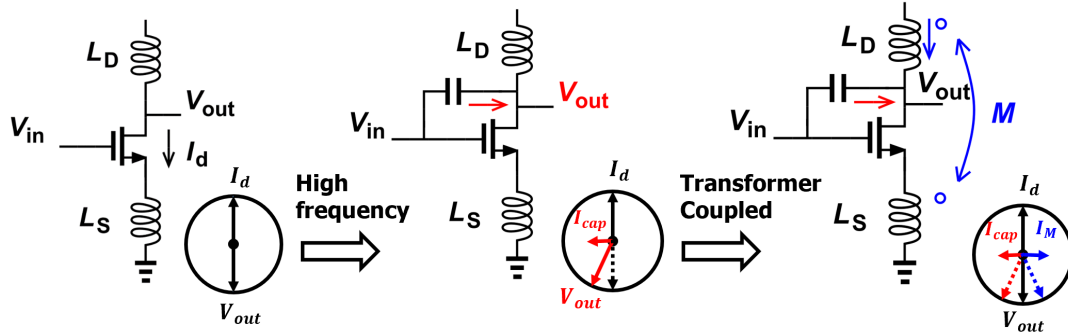


Figure 3.6: Operation of drain to source inductive coupling neutralization

direction of current $I_{gd}e^{j\psi}$. As shown in the Fig. 3.6, this mutual current helps to push the phase of the output voltage back to be 180° degree out of phase of the drain current if the C_{gd} is fully compensated.

The idea is clear for the inductive coupling neutralization that a mutual current is brought to the drain node to compensate the current flow through the C_{gd} . The Fig. 3.7 shows the ideal of combining inductive coupling with the stack FET PA. Instead of using the drain to source inductor coupling, here using the drain load inductor and the inter-stage matching inductor coupling. The operation is same to the drain to source inductive coupling. A mutual coupling current is injected to both drain node of the two FETs as 180° degree phase difference of the current I_{gd} to compensate the C_{gd} .

As discussed before, the inductive coupling generates a mutual current that injected into drain node to fully or partially compensated the C_{gd} . In this design, I swept the coupling coefficient to check the change of PAE and stability factor μ as shown in Fig. 3.8. From this sweep, the coupling coefficient is chosen to be 0.2 to keep high PAE while maintain stable. For the layout design feasibility, the coupled inductors are designed as coupled transmission lines in Fig. 3.9.

Fig. 3.10 shows the detailed schematic of this design. Since the $240\mu\text{m}$ NFET in GF 45nm RF SOI technology shows a load line impedance about 25Ω with $1.2VV_{ds}$ in class-

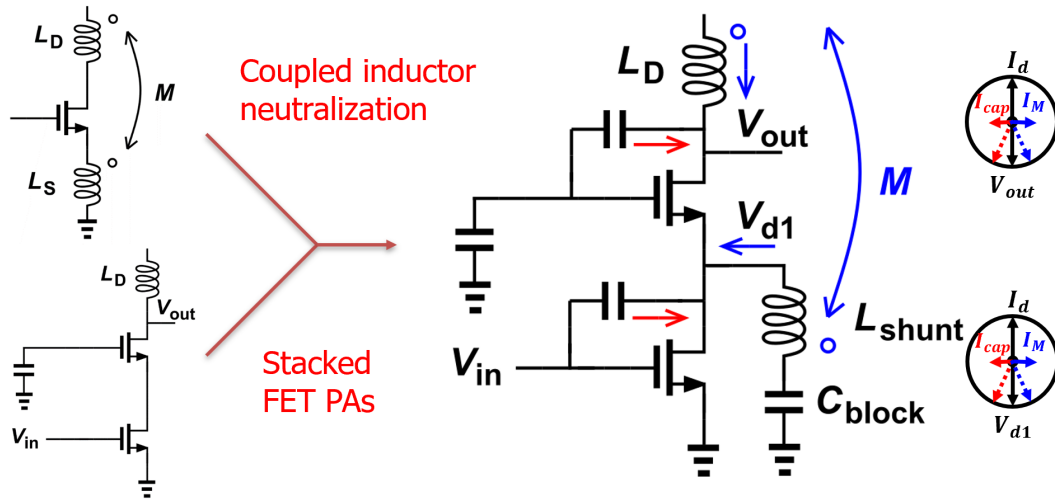


Figure 3.7: Novel neutralization topology combines inductive coupling with stack FET PA

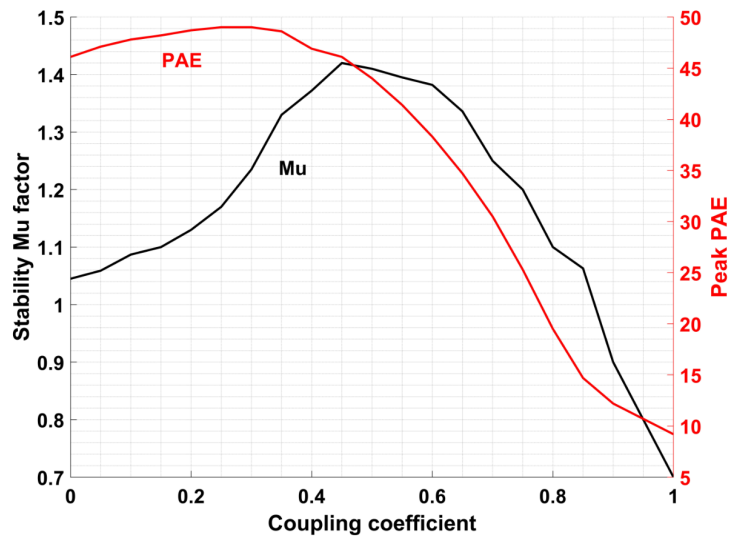


Figure 3.8: Coupling coefficient vs PAE and stability factor μ

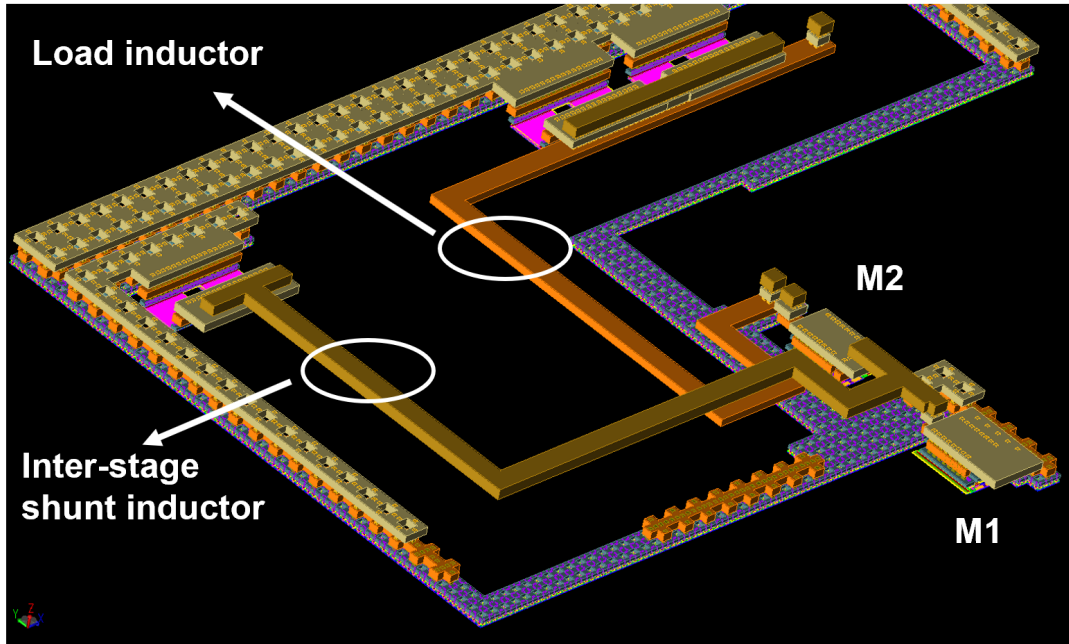


Figure 3.9: Implementation of the layout for coupled inductors

B bias condition, two stack-FET topology with $240\mu\text{m}$ NFET PA shows 50Ω load line impedance. This helps to remove the output matching network which used to be lossy at mm-wave band to minimize the power reduction. The gate capacitance of the top transistor is chosen to be 1pF and this make the PA looks more like a cascode while it does not exceed the breakdown voltage and the reliability voltage. The V_{gs} is set to be 0.3V for class-B operation.

Fig. 3.11 and Fig. 3.12 shows a comparison of the cases with and without neutralization voltage V_{ds} and current I_d waveforms for bottom NFET and top NFET. We can observe that in the Fig. 3.11a and Fig. 3.11b, the voltage and current waveforms are aligned in the case with neutralization and a phase mismatch between voltage and current waveforms exists in the case without neutralization. This shows the effect of the mutual current that helps to shift the voltage waveform back to be 180° degree out of phase with current waveform. The average DC power consumption for bottom NFET with neutralization is

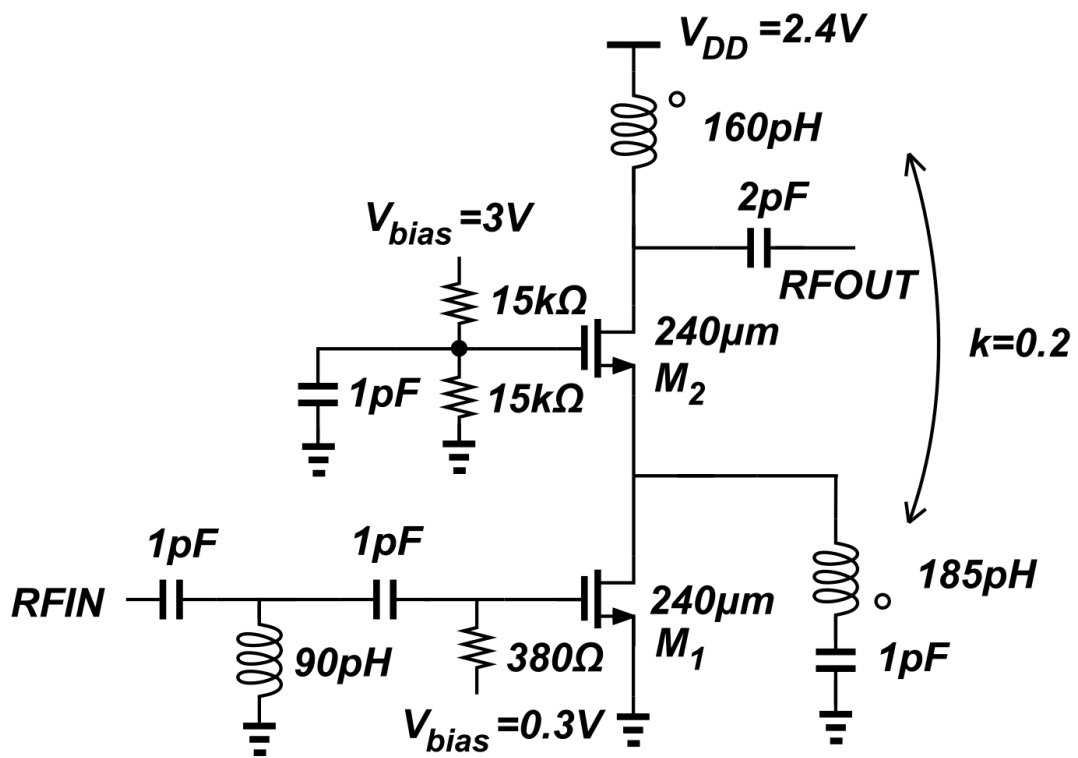


Figure 3.10: Schematic of the inductive coupling neutralization PA design

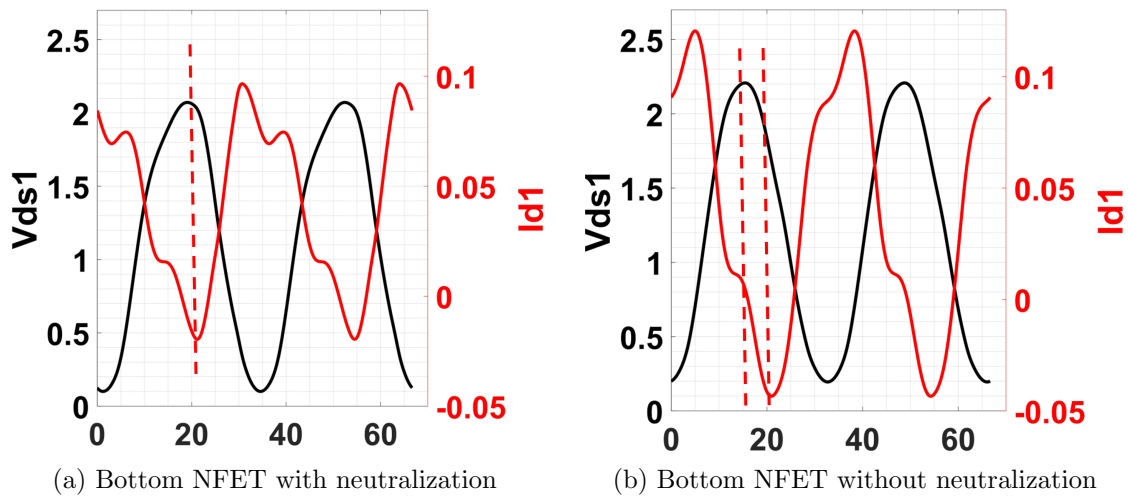


Figure 3.11: Comparison of with and without neutralization voltage and current waveforms on drain node for bottom NFET

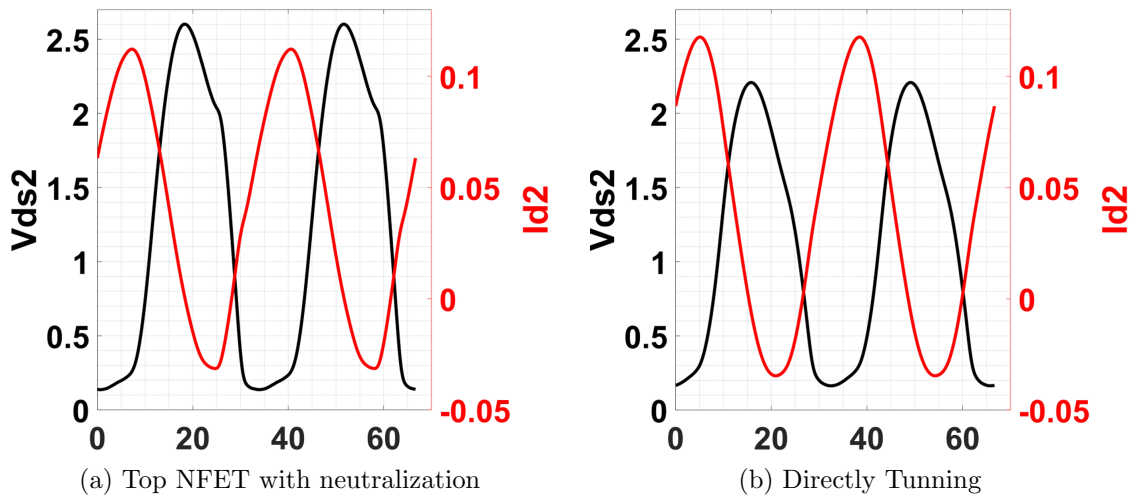


Figure 3.12: Comparison of with and without neutralization voltage and current waveforms on drain node for top NFET

42mW and for bottom NFET without neutralization is 48mW.

Fig. 3.12a and Fig. 3.12b show the voltage and current waveforms in two cases for the top NFET. From these two, we could tell both NFET present similar phase shift between the voltage and current waveforms and it's because of the parasitic capacitance C_{ds} as the feedback capacitance rather than C_{gd} . The top NFET has 49mW DC power consumption

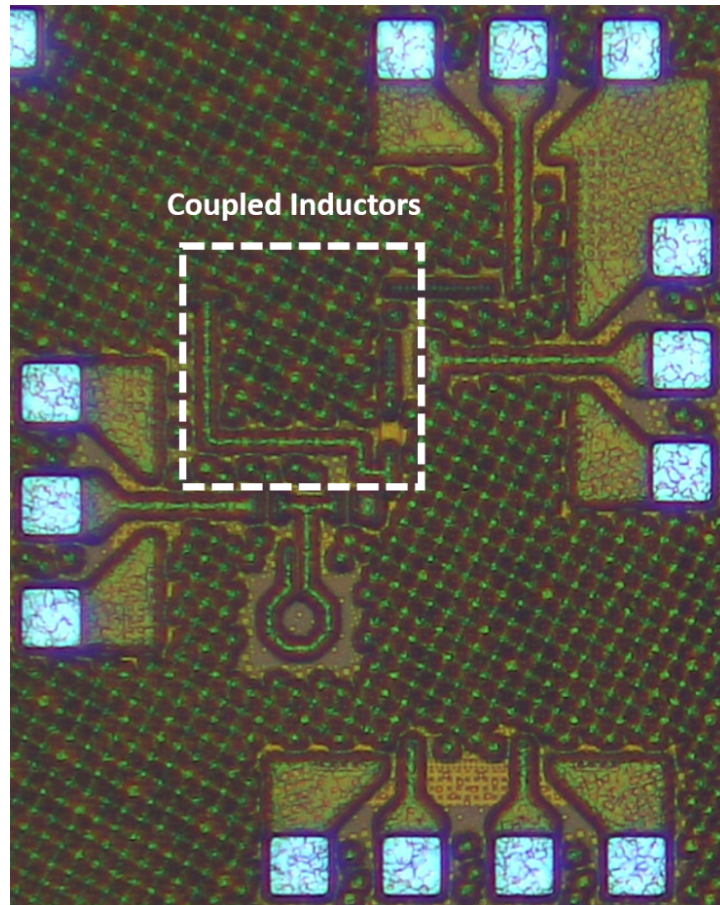


Figure 3.13: Chip micrograph

in the case with neutralization and 43mW in the case without neutralization. This is mainly because the in the simulation, the output power of the bottom NFET is larger with the neutralization.

Fig. 3.13 shows the micrograph of the implemented PA. Chip size is $520\mu m * 530\mu m$ including DC and RF pads. Fig. 3.14 shows comparison of simulation and measurement small signal S-parameter results. The peak S-parameter is 13.6dB at 30 GHz with a wide bandwidth from 25.5 GHz to 37.5 GHz. In band S11 and S22 are lower than -10dB. The measurement results matched the simulation results well. A frequency shift on the measured S11 comparing to simulation result could be contributed by the modeling in-

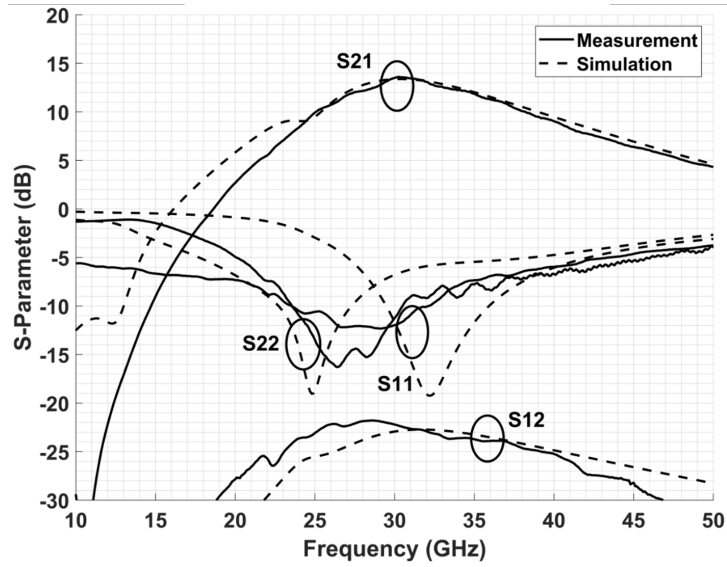


Figure 3.14: Comparison of simulated and measured s parameter

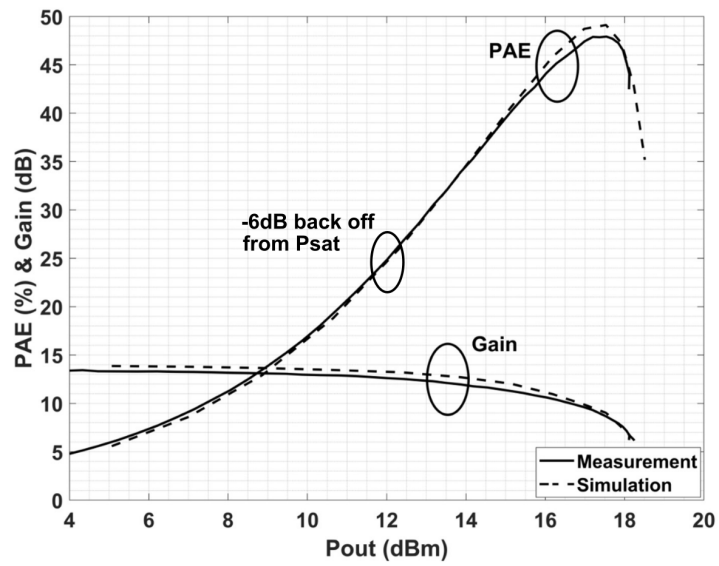


Figure 3.15: Measured PAE and gain at 30GHz

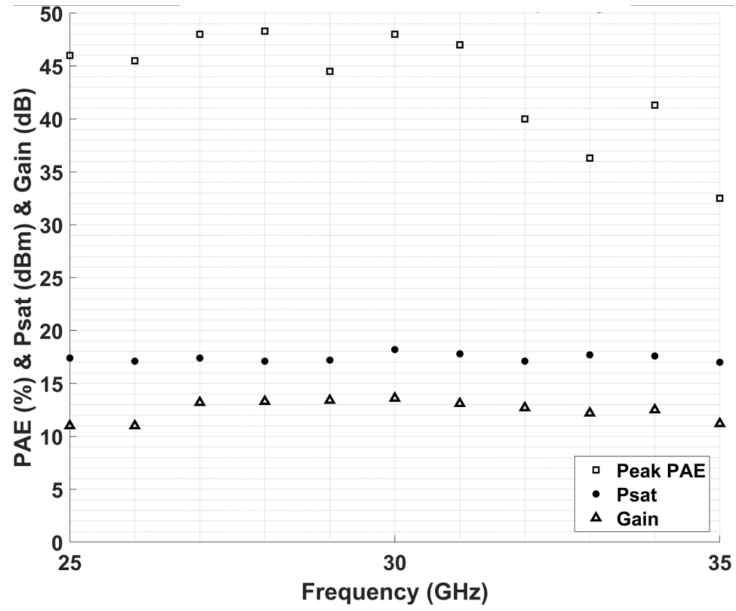


Figure 3.16: Gain, P_{sat} and PAE at P_{sat} over the band

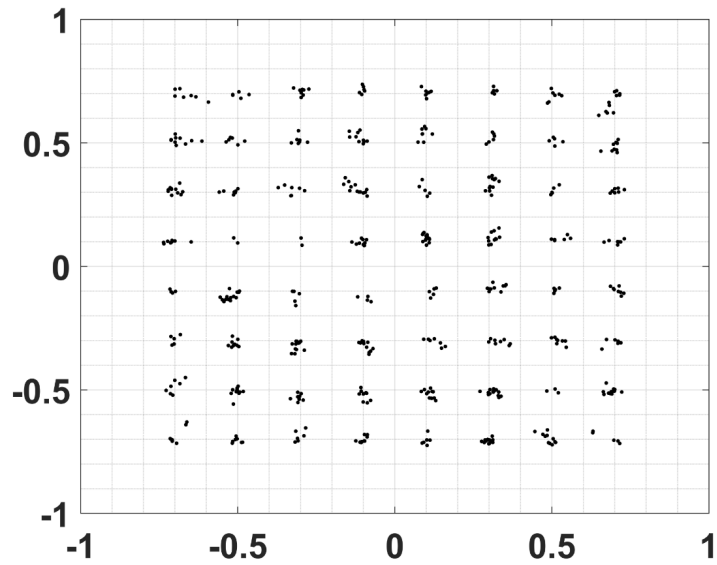


Figure 3.17: Measured constellation for QAM64 signal

Comparison of this work with state of art

Param.\Ref.	[10]	[18]	[16]	[19]	[20]	This work
Tech CMOS	130nm SiGe	65nm	65nm	40nm	28nm	45nm SOI
Supply (V)	2.3	1.1	1.1	1	1.1	2.4
Frequency (GHz)	22-28	26-34	24-32	26-29	24-30	25.5-37.5
FBW (%)	24	26.7	28.6	10.9	22.2	38
P_{sat} (dBm)	18	14.75	15.6	18.1	19.8	18
P_{1dB} (dBm)	16	13.2	14	16.8	18.6	16
PAE at 28GHz (%)	36	44	41	41.5	41.4	48.2
Gain (dB)	21	10	15.8	20.5	13.6	13.6
Chip Size (mm ²)	0.6	0.12	0.24	0.36	0.28	0.27
FOM1	264	251	256	263	258	258

$$FOM1(ITRS) = P_{sat} + Gain + 10\log(PAE_{peak}) + 20\log(Freq)$$

accuracy on RF pads.

Fig. 3.15 shows large signal measurement and simulation comparisons. The PAE and gain are measured at 30GHz. Peak PAE is 48.2% with 13.6dB small signal gain. The saturate output power P_{sat} is 18dBm with 16dBm P_{1dB} . From the PAE vs. P_{out} , efficiency drops to half every 6dB output power back-off, it's clear that it is a class-B PA. Fig. 3.16 shows measured gain, P_{sat} and PAE at P_{sat} over the 3dB bandwidth of small signal. From the measurement results, the peak PAE is over 40% from 25GHz to 33GHz. P_{sat} is above 17dBm in the small signal 3dB bandwidth.

The Fig. 3.17 shows the constellation measurement result for QAM64 signals with 100MS/s symbol rate in using raised cosine filter. The peak power of the modulated signal is 3dB back off from P_{sat} and the average power is 8.2dBm. From the measurement results, the ACPR is -30dBc and EVM is 4.2%.

The table shows a comparison of this work with the state of art. This PA achieves the highest PAE at this band.

Chapter 4

Outphasing PA Design

In modern wireless communication systems, M-QAM signals are used for transmitting high data rates in bandwidth-limited channels. Theoretically, the peak-to-average power ratio (PAPR) is 3.7dB for 64-QAM and 4.8dB for QAM signals with M approaching infinity. However, real implementations of a M-QAM communication link requires filtering due to the limited bandwidth. As shown in Chapter 1, the filtered signal has a PAPR about 5 to 6 dB. In fact, in the modern communication systems such as 4G mobile communication and digital television, orthogonal frequency-division multiplexing (OFDM) is used which has a PAPR close to 12dB. These transmission systems require high efficiency not only at the peak output power, but also at the back-off power range. This means that improving the average efficiency of the PA is critical for improving efficiency on the whole system. In the past, outphasing PA was proposed by Chireix to improve PA efficiency at power back-off. However, in mm-wave band, there has been limited research in outphasing PAs. Additionally, no constant envelope outphasing PA has been designed successfully to show efficiency improvements at power back-off when compared to a class-B PA.

In [21, 22], a 60 GHz outphasing PA was proposed using a transformer for power com-

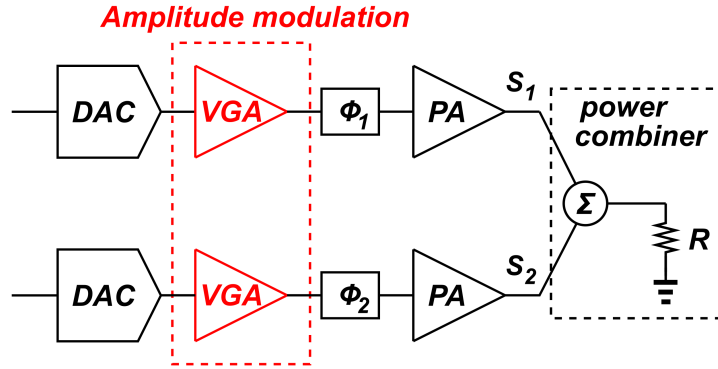


Figure 4.1: Architecture of others' work

binning. However, the PAE of this PA drops from 25% at peak output power 15.3dBm to 7% at 9.3dBm, the 6dB output power back-off point. In [23], a 28GHz, 23dBm P_{sat} outphasing PA with SiGe process has been proposed. In this work, the Chireix power combiner was designed using a sub-quarter wavelength balun. However, the loss of the sub-quarter wavelength balun strongly depends on the metal thickness, which leads to process-dependent performance. Also, in this design, the amplitude modulation are used with the outphasing control at the RF input. In [24], an outphasing PA is designed with the antenna. This PA achieves 53% drain efficiency with 17dBm output power. However, this design makes use of amplitude modulation with outphasing angle on the RF signals. As shown in the Fig. 4.1, the outphasing designs at mm-wave band use the architecture that includes amplitude modulation to assist the output power level control. However, in this work's proposed outphasing architecture, as shown in the Fig. 4.2, there is only outphasing phase control. In this work, we are trying to research on the issues that degrades the performance and propose circuit using constant envelope, phase-only control RF signals.

In this chapter, section 4.1 discusses the conventional outphasing PA theory. Section 4.2 discusses the basic theory of the hybrid outphasing PA. Section 4.3 discusses the parasitics handling in the outphasing PA design. Section 4.4 demonstrates the design

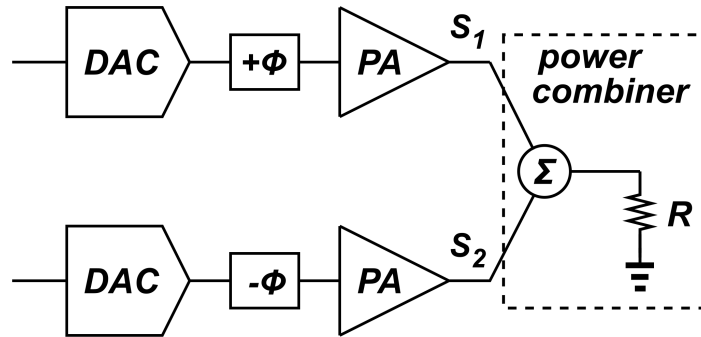


Figure 4.2: Proposed architecture of this work

methodology of outphasing power amplifier at 28GHz with constant envelope input signals in GlobalFoundries 45 nm SOI CMOS process. Section 4.5 shows the measurement results of the outphasing PA. Section 4.6 shows the limitations of outphasing PA topology and modern process.

4.1 Theory of Conventional Outphasing PA

In 1935, H. Chireix proposed a high-power outphasing modulation in [3] that improved the back-off efficiency in comparison to linear PAs such as class-A and class-B. In this section, a detailed derivation of the outphasing modulation is shown to develop a foundation for the following discussion.

Here we start with simple power combining as shown in Fig. 4.3. Two constant-envelope voltage sources represent two PAs. The two PAs are combined in parallel with two $\lambda/4$ transmission lines. This topology is a voltage-mode power amplifier with a voltage-mode power combiner. These two PAs have different phases which are represented with $\pm\theta$.

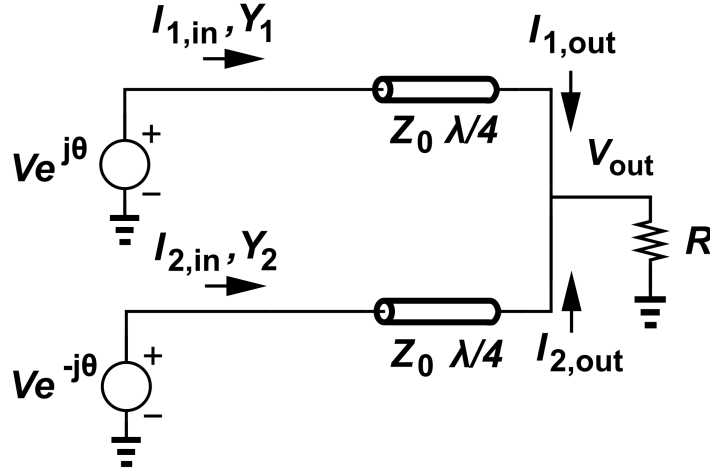


Figure 4.3: Voltage mode power amplifier with voltage mode power combining

The voltage and current at input and output can be written as:

$$\begin{bmatrix} Ve^{j\theta} \\ I_{1,in} \end{bmatrix} = \begin{bmatrix} \cos(\theta) & jZ_0 \sin(\theta) \\ j\frac{\sin(\theta)}{Z_0} & \cos(\theta) \end{bmatrix} \begin{bmatrix} V_{out} \\ -I_{1,out} \end{bmatrix} \quad (4.1)$$

$$\begin{bmatrix} Ve^{-j\theta} \\ I_{2,in} \end{bmatrix} = \begin{bmatrix} \cos(\theta) & jZ_0 \sin(\theta) \\ j\frac{\sin(\theta)}{Z_0} & \cos(\theta) \end{bmatrix} \begin{bmatrix} V_{out} \\ -I_{2,out} \end{bmatrix} \quad (4.2)$$

$$(I_{1,out} + I_{2,out})R_L = V_{out} \quad (4.3)$$

From these equation, we have the following result:

$$R'_L = \frac{Z_0^2}{R_L} \quad (4.4)$$

$$I_{1,in} = I_{2,in} = \frac{2V \cos(\theta)}{R'_L} \quad (4.5)$$

$$I_{1,out} = j \frac{V e^{j\theta}}{Z_0} \quad (4.6)$$

$$I_{2,out} = j \frac{V e^{-j\theta}}{Z_0} \quad (4.7)$$

$$V_{out} = 2jV \cos(\theta) \frac{R_L}{Z_0} \quad (4.8)$$

From above equations, it is clear that the output voltage amplitude is a cosine function of the input phase θ . Theoretically, this could reach any voltage amplitude level that does not exceed $2V \frac{R_L}{Z_0}$.

To calculate the efficiency, the following assumptions are made:

1. The PA is biased at class-B point.
2. The voltage at the input of the combiner has a constant amplitude as V regardless the change of outphasing angle θ .
3. The PA is working at the maximum output power point, or say, the voltage amplitude V is equal to V_{dd} of the PA.
4. The PA is able to provide any current as required by the load impedance.

The admittance could be calculated as:

$$\begin{aligned} Y_k &= \frac{I_k}{V_k} = \frac{2\cos^2(\theta)}{R'_L} \mp j \frac{\sin(2\theta)}{R'_L} \\ &= G_0 \mp jB_0 \end{aligned} \quad (4.9)$$

Where $k=1,2$ represent the different paths. From assumption 3, the power provided by each PA could be calculated as:

$$\begin{aligned} P_{RF,k} &= \frac{1}{2} \text{Re}\{V_k^* Y_k^* V_k\} \\ &= \frac{1}{2} |V_k|^2 G_0 \end{aligned} \quad (4.10)$$

Notice that in above equation, $V_k^* Y_k^*$ is the RF current provided by the PA at fundamental, from equation 2.8, the fundamental current has the following relation with the maximum instantaneous current in class-B PA:

$$I_{1st} = \frac{1}{2} I_{max} \quad (4.11)$$

And the average DC current I_{DC} has the relation with I_{max} in equation 2.11:

$$I_{DC} = \frac{I_{max}}{\pi} \quad (4.12)$$

The DC power consumption is then written as:

$$\begin{aligned} P_{DC} &= |I_{DC}| * V_{DC} \\ &= \left| \frac{I_{max}}{\pi} \right| * V_k \\ &= \left| \frac{2I_{1st}}{\pi} \right| * V_k \\ &= \left| \frac{2V_k^* Y_k^*}{\pi} \right| * V_k \\ &= \frac{2}{\pi} V_k^2 |Y_k^*| \end{aligned} \quad (4.13)$$

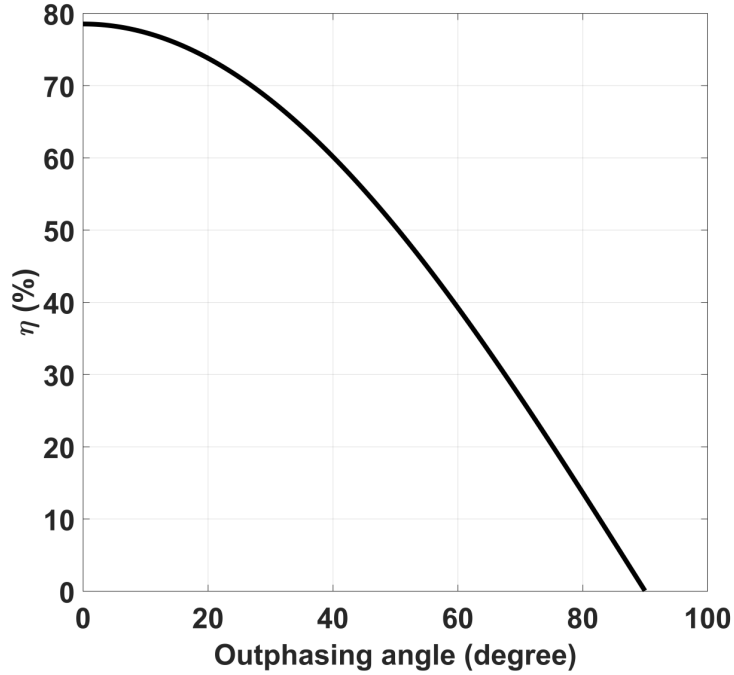


Figure 4.4: Theoretical η with outphasing angle

Since $|Y_1| = |Y_2|$, the RF power provided by two PAs are the same, the DC power consumption is as well. The drain/collector efficiency is given by:

$$\begin{aligned}
 \eta &= \frac{P_{RF}}{P_{DC}} \\
 &= \frac{\frac{1}{2}|V_k|^2 G_0}{\frac{2}{\pi} V_k^2 |Y_k|} \\
 &= \frac{\pi}{4} \frac{G_0}{\sqrt{G_0^2 + B_0^2}}
 \end{aligned} \tag{4.14}$$

Fig. 4.4 and Fig. 4.5 shows a drain efficiency with the outphasing angle and drain efficiency relative to output power respectively. In Fig. 4.5, it is obvious that in terms of back-off efficiency improvement, the outphasing PA has exactly same performance comparing to class-B PA. The numerator in equation 4.14 represents for the output power term and the denominator represents for the DC power consumption term. To improve

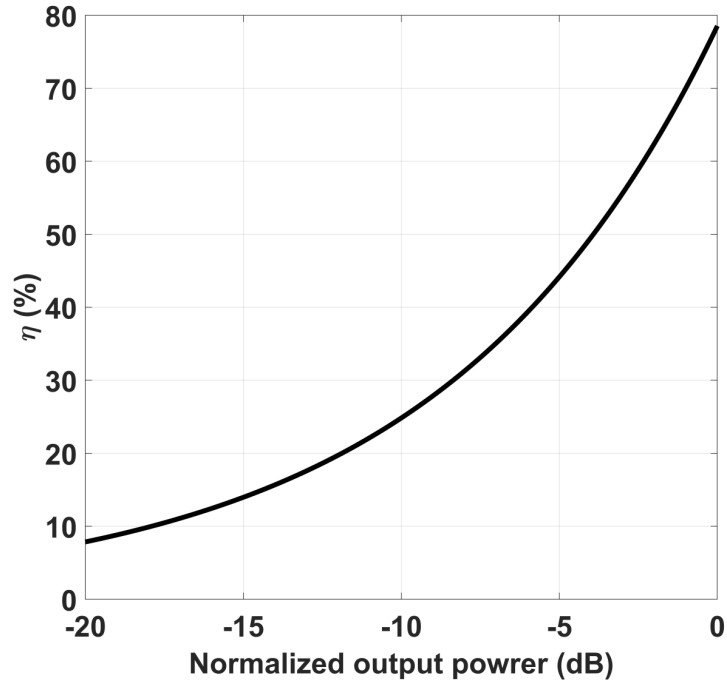


Figure 4.5: Theoretical η with normalized output power in dB

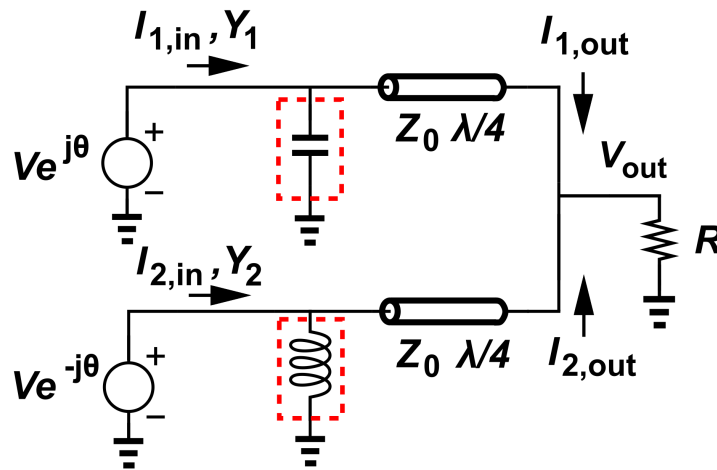


Figure 4.6: Schematic of the Chireix's outphasing PA

the efficiency, H. Chireix introduced compensation shunt component as shown in Fig. 4.6. Since $Y_1 = \frac{2\cos^2(\theta)}{R'_L} - j\frac{\sin(2\theta)}{R'_L}$ on the top path, a positive susceptance B_c , a capacitor is added to compensate with B_0 in order to decrease the denominator of equation 4.14. The added susceptance does not change the input voltage, it could be treated as additional current is provided by the PA to flow through the susceptance. In the Chireix outphasing PA topology, the admittance could be directly written as:

$$Y_k = G_0 \mp jB_0 \pm jB_c \quad (4.15)$$

The RF power is $\frac{1}{2}|V_k|^2G_0$, same as the RF power without compensation component, and the DC power consumption is calculated as: $= \frac{2}{\pi}V_k^2|Y_k^*|$. The η is then written as:

$$\eta_{Chireix} = \frac{G_0}{\sqrt{G_0^2 + (B_0 - B_C)^2}} \quad (4.16)$$

In changing phase operation, G_0 and B_0 varies with the outphasing angle θ . But the compensation component B_C is constant. We could choose a coefficient γ that $B_C = \gamma B_{0,max}$ to fully or partially compensating the susceptance.

Fig. 4.7 shows the η versus outphasing angle. Comparing to Fig. 4.4, we can see that at the power back off, the efficiency η is higher in topology with the compensation.

Fig. 4.8 shows η versus the output power with chosen $\gamma = 0.4$ and $\gamma = 1$. It's clear that γ less than 1 - which means the susceptance is partially compensated - provides larger efficiency improvement range on output power back-off with a efficiency drop before it reaches peak again at back off. Choosing γ actually relates to the specific modulation scheme with a particular PAPR.

In Fig. 4.8, the DC power consumption with adding Chireix's compensation components are compared to the topology without using compensation. It's clear that in the out-

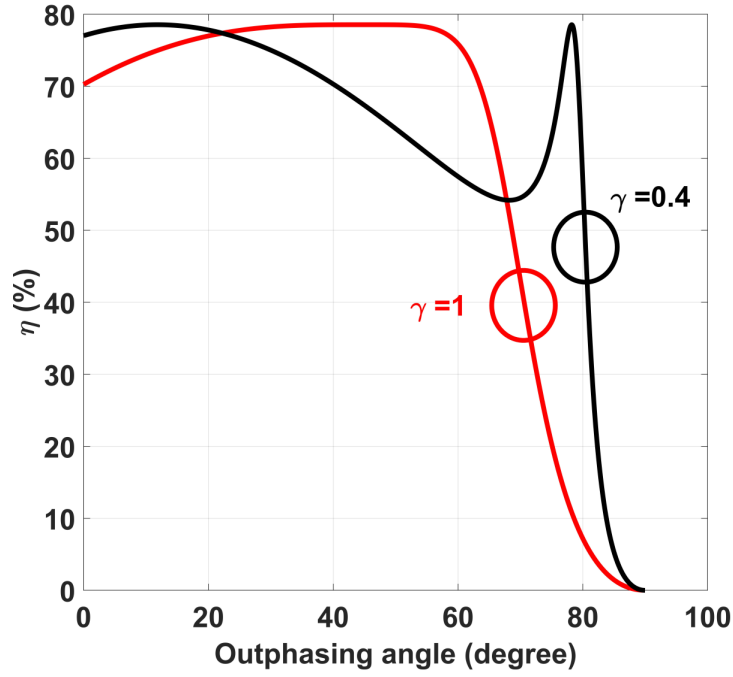


Figure 4.7: Theoretical η with outphasing angle in Chireix's outphasing PA (voltage-mode PA with voltage-mode power combiner)

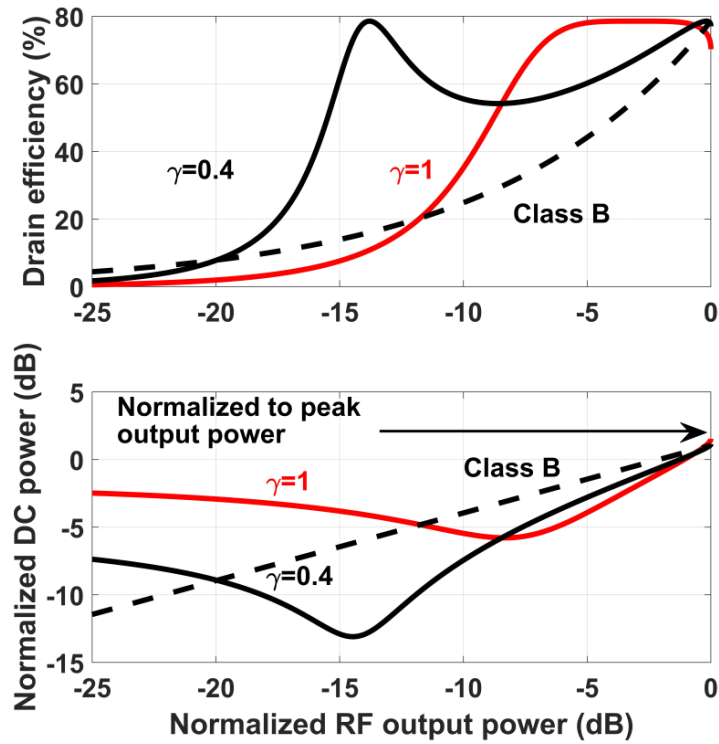


Figure 4.8: Theoretical η with normalized output power in dB in Chireix's outphasing PA

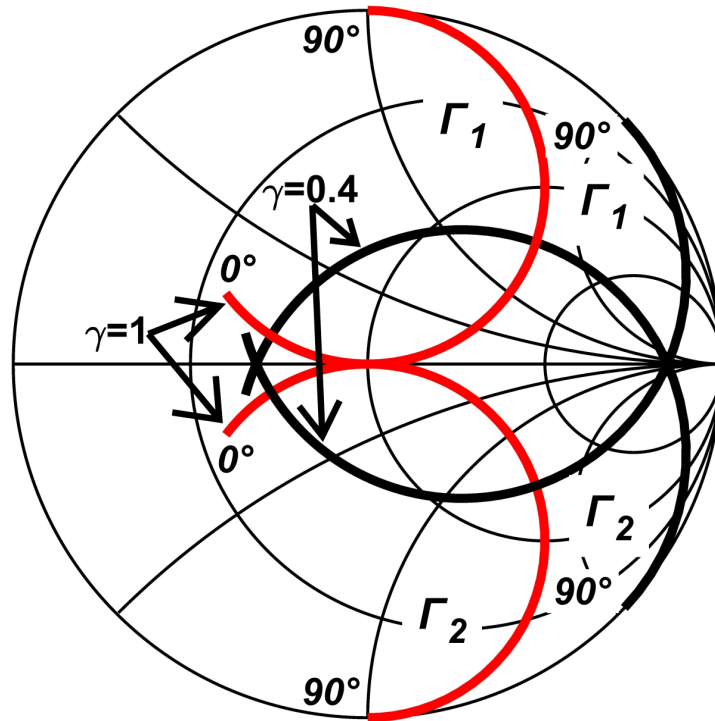


Figure 4.9: Smith chart with showing reflection from two path of the combiner

phasing PA, the DC power consumption reduction at the power back off is the factor for efficiency improvement. In the $\gamma = 0.4$, the DC power consumption below normal class-B has a larger output power back off range comparing to the $\gamma = 1$ curve, so does η curve.

Checking the reflection coefficient of two path is another way to understand the efficiency improvement procedure. This is plotted in Fig. 4.9 with the outphasing angle swept from 0° to 90° degree in both $\gamma = 0.4$ and $\gamma = 1$ cases. In this plot, the impedance seeing into the two paths are symmetrical to the real impedance axis. Comparing Fig. 4.9 and Fig. 4.7, in Fig. 4.7 the peak output power occurs in 0° to 10° range and the back-off η peaks at 60° to 80° range. In Fig. 4.9, both 0° to 10° range and 60° to 80° range are close to the real impedance axis. In real designs, this helps to determine the load line impedance since it should not too far away from the peak back-off efficiency improve-

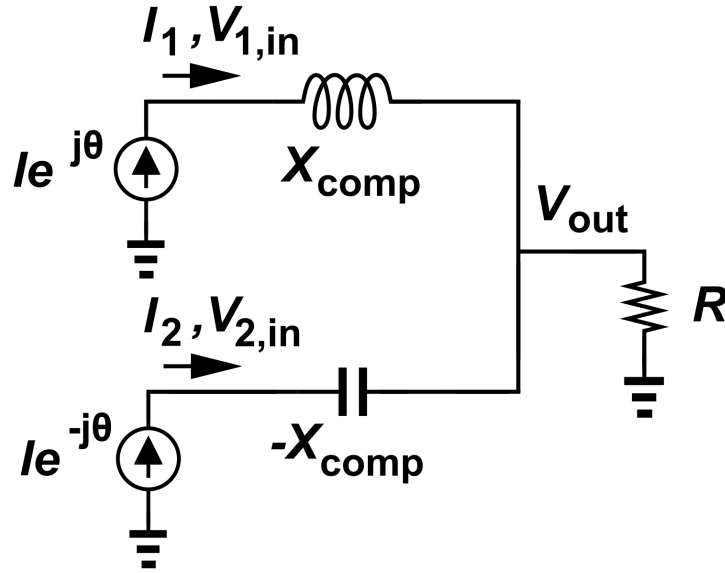


Figure 4.10: Schematic of current-mode power amplifier with current mode power combiner

ment impedance. And it is obvious that using $\gamma = 0.4$ to get wide power back-off η improvement range, the impedance could be as high as 500Ω . This is not prohibitive for the modern PA design in CMOS technology. Due to the low break down voltage, the MOSFET often sized to be large enough for certain amount of output power that the load line impedance is usually lower than 100Ω .

The above theory is the Chireix outphasing power amplifier. It requires constant envelope voltage sources for the power combining. In past, the outphasing power amplifier with using constant envelope current source has also been proposed in [25–28]. Fig. 4.10 shows the schematic of current source PA with current-mode power combining. For this schematic, we could write the current and voltage at input and output as:

$$V_{1,in} - V_{out} = I e^{j\theta} * sL \quad (4.17)$$

$$V_{2,in} - V_{out} = I e^{-j\theta} * \frac{1}{sC} \quad (4.18)$$

$$V_{out} = (Ie^{j\theta} + Ie^{-j\theta}) * R_L \quad (4.19)$$

Solve above equations, we have:

$$V_{out} = 2I\cos(\theta)R_L \quad (4.20)$$

$$V_{1,in} = V_{out} + Ie^{j\theta} * sL \quad (4.21)$$

$$V_{2,in} = V_{out} + Ie^{-j\theta} * \frac{1}{sC} \quad (4.22)$$

So the impedance seeing into two paths are:

$$\begin{aligned} Z_{1,in} &= \frac{V_{1,in}}{I_{1,in}} \\ &= 2R_L\cos(\theta)(\cos(\theta) - j\sin(\theta)) + j\omega L \\ &= 2R_L\cos^2(\theta) - jR_L\sin(2\theta) + j\omega L \\ &= R_0 - jX_0 + jX_C \end{aligned} \quad (4.23)$$

$$\begin{aligned} Z_{2,in} &= \frac{V_{2,in}}{I_{2,in}} \\ &= 2R_L\cos(\theta)(\cos(\theta) + j\sin(\theta)) - j\frac{1}{\omega C} \\ &= 2R_L\cos^2(\theta) + jR_L\sin(2\theta) - j\frac{1}{\omega C} \\ &= R_0 + jX_0 - jX_C \end{aligned} \quad (4.24)$$

Similar to the voltage mode, the RF power, DC power consumption and drain/collector efficiency η in the current mode could be written as:

$$\begin{aligned} P_{RF,k} &= \frac{1}{2} \text{Re}\{I_k^* Z_k^* I_k\} \\ &= \frac{1}{2} |I_k^*|^2 R_0 \end{aligned} \quad (4.25)$$

$$\begin{aligned} P_{DC} &= |I_{DC} * V_{DC}| \\ &= |I_{DC} * \frac{V_{max}}{\pi}| \\ &= \frac{2}{\pi} I^2 |Z_k^*| \end{aligned} \quad (4.26)$$

$$\begin{aligned} \eta &= \frac{P_{RF}}{P_{DC}} \\ &= \frac{\frac{1}{2} |I_k^*|^2 R_0}{\frac{2}{\pi} I^2 |Z_k^*|} \\ &= \frac{\pi}{4} \frac{R_0}{\sqrt{R_0^2 + X_0^2}} \end{aligned} \quad (4.27)$$

These results are similar to the Chireix outphasing PA. However, as shown in the Fig. 4.11, the reflection coefficient seeing into two paths of the current-mode power combiner is very different from the voltage-mode power combiner. In the voltage-mode case, the high efficiency range is from 25Ω to 500Ω , but in the current-mode approach, the high efficiency range is actually from the 10Ω to 100Ω . This low impedance range is preferred in CMOS design due to the low breakdown voltage.

The above equations are similar to the PA with the voltage-mode power combiner. However, in above derivation, an assumption was made:

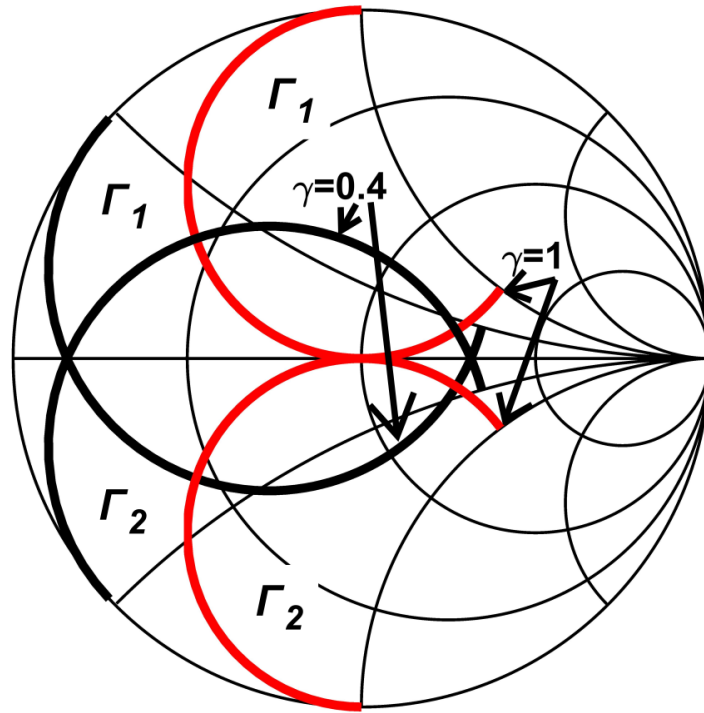


Figure 4.11: Smith chart of showing reflection coefficient in current mode PA with current mode power combiner

It's an 'inverse class-B' PA.

The derivation actually assumes that in the current-mode outphasing PA, the voltage waveform should look like the current waveforms in the voltage-mode outphasing PA. However, in MOSFET operation, the output voltage waveform is determined by the current waveform on the drain node and the impedance seen at the drain node. And the drain current waveform is determined by the input signal and the threshold voltage. So the theoretical half-wave waveform of the drain current comes from the period that the NMOS is off from the class-B bias. That means the voltage waveform at drain current waveform can't be changed to design as an inverse class-B easily.

So, in using the real class-B waveform for the current-mode outphasing PA, the theoretical derivation should be:

$$\begin{aligned}
P_{DC} &= |I_{DC} * V_{DC}| \\
&= \left| \frac{I_{max}}{\pi} * V_{DC} \right| \\
&= \left| \frac{2I_{fund}}{\pi} * V_{DC} \right|
\end{aligned} \tag{4.28}$$

$$\begin{aligned}
\eta &= P_{RF,k} / P_{DC} \\
&= \frac{\frac{1}{2} |I_k^*|^2 R_0}{\left| \frac{2I_{fund}}{\pi} * V_{DC} \right|} \\
&= \frac{\pi I_k^* R_0}{4 V_{DC}}
\end{aligned} \tag{4.29}$$

Here, the class-B PA could not provide the current-mode operation that has DC power reduction at the power back off.

Based on the above derivation, a prerequisite condition for the conventional Chireix outphasing PA design is that the power amplifier should support a large range and very high load impedance even to 500Ω while maintaining a constant output voltage amplitude. Another disadvantage is the use of $\lambda/4$ transmission lines. These transmission lines at the fundamental frequency in modern process usually very lossy. This not only decreases the output power, but also drops the PAE and the current-mode outphasing PA actually requires an inverse class-B PA which is not feasible with the real MOSFET.

4.2 Theory of Hybrid outphasing PA

In section 4.1, we discussed the conventional Chireix voltage-mode PA with voltage-mode power combiner, and also showed the current-mode PA with the current-mode

combiner. The advantage of low impedance range in current-mode power combiner, allows for a voltage-mode PA with the current-mode power combiner to comprise a hybrid voltage- and current-mode outphasing PA. The topology of hybrid outphasing PA is shown in Fig. 4.12.

Similar to the Chireix outphasing power combiner where compensation components exhibit symmetrical characteristics, in the hybrid outphasing PA, the compensation reactance should be in the same absolute value with different sign as shown in the schematic. The voltage and current at the input and output is then written as:

$$V e^{j\theta} - V_{out} = I_{1,in} * jX_C \quad (4.30)$$

$$V e^{-j\theta} - V_{out} = I_{2,in} * (-jX_C) \quad (4.31)$$

$$I_{1,in} + I_{2,in} = V_{out}/R_L \quad (4.32)$$

From these, we have:

$$I_k = \frac{V \sin(\theta)}{X_C} \mp j \left(\frac{V \cos(\theta)}{X_C} - \frac{2V R_L \sin(\theta)}{X_C^2} \right) \quad (4.33)$$

$$V_{out} = \frac{2V R_L \sin(\theta)}{X_C} \quad (4.34)$$

The admittance could be written as:

$$Y_k = \frac{V \sin(\theta)}{X_C} \mp j \left(\frac{V \cos(\theta)}{X_C} - \frac{2V R_L \sin(\theta)}{X_C^2} \right) \quad (4.35)$$

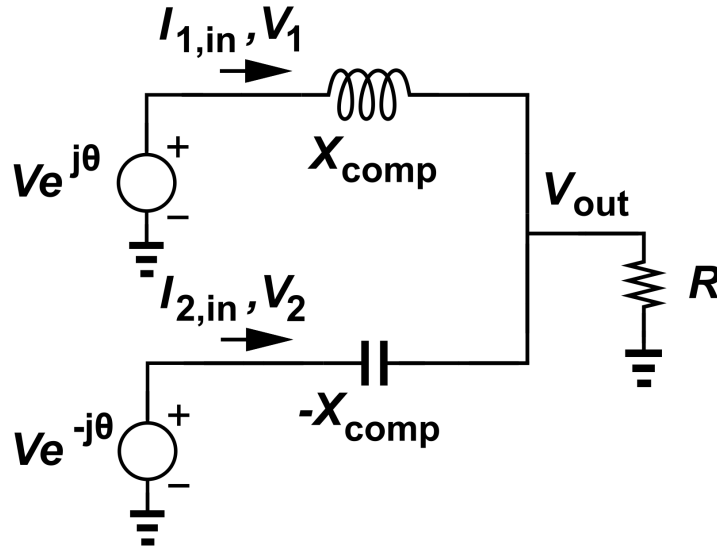


Figure 4.12: Schematic of hybrid outphasing power amplifier

Similar to other two modes outphasing PA, the fundamental RF output power and the DC power consumption could be calculated as:

$$\begin{aligned}
 P_{RF,k} &= \frac{1}{2} V_k \text{Re}\{Y_k^*\} \\
 &= |V^2| \sin^2(\theta) \frac{R_L}{X_C^2}
 \end{aligned} \tag{4.36}$$

$$\begin{aligned}
 P_{DC} &= \frac{2}{\pi} V^2 |Y_k^*| \\
 &= \frac{2}{\pi} V^2 \frac{R_L}{X_C^2} \sqrt{(2\sin^2(\theta))^2 + \left(\frac{X_C}{R_L} - \sin^2(2\theta)\right)^2}
 \end{aligned} \tag{4.37}$$

So the efficiency in hybrid mode outphasing is:

$$\eta = \frac{\pi}{2} \frac{\sin^2(\theta)}{\sqrt{4\sin^4(\theta) + \left(\sin(2\theta) - \frac{X_C}{R_L}\right)^2}} \tag{4.38}$$

In above equation, we can define a new gamma that $\gamma = \frac{X_C}{R_L}$. And we could choose the

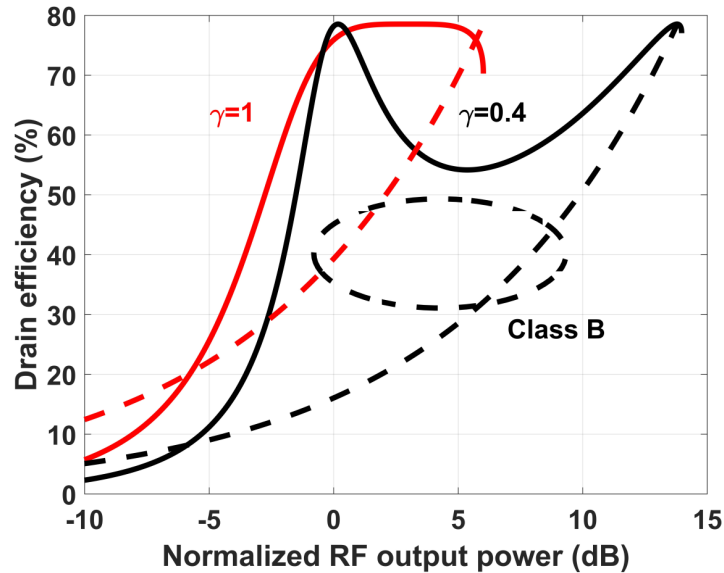


Figure 4.13: Efficiency at back off with different compensation component in hybrid mode outphasing PA

$\gamma = 0.4$ and $\gamma = 1$ cases to plot the efficiency with the output power as shown in the Fig. 4.13. Characteristics of the hybrid mode outphasing PA η plot:

1. Different size of compensation component brings different efficiency improvement range at power back-off.
2. In the hybrid mode PA theoretical calculation result, the different compensation has a different peak power level. This is a theoretical calculation mathematical result. To demonstrate this, we could simply take it as larger X_C resists more current to be transferred to the load. So with larger compensation component, less output power could be reached.
3. From the above conclusion, it is worth to check the impedance seen into two paths of the current-mode combiner in hybrid mode operation.

Fig. 4.14 shows the reflection coefficient looking into two paths of the PA. In the $\gamma = 0.4$ curves, it is showing that the impedance range for peak output power and back-off peak efficiency is from 10Ω to 100Ω , same as the current mode outphasing PA. This is one

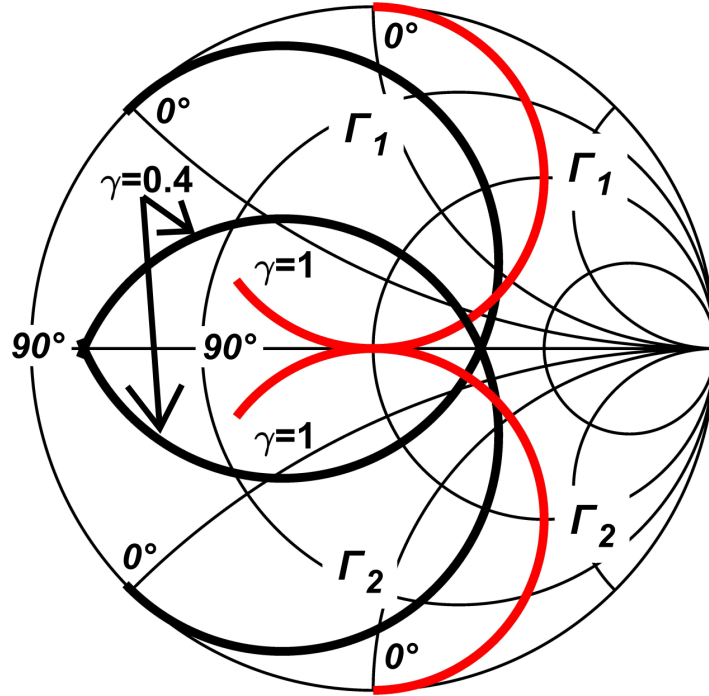


Figure 4.14: Reflection from the two paths of the current mode combiner in hybrid mode operation

advantage of hybrid mode outphasing PA for modern CMOS process that it requires low load line impedance for the whole outphasing angle operation range. Also, it omits the requirement for using the lossy $\lambda/4$ transmission lines.

4.3 Critical Parasitics Handling

Another issue needs to be handled well is the critical parasitics in the outphasing PA. As shown in the Fig. 4.15, the main parasitics in a NMOS are C_{gs} , C_{gd} and C_{ds} . Since in the outphasing PA operation, the amplitude of the output voltage from a single PA is constant. This means that the input voltage amplitude should not change with different outphasing angle. In this case, the C_{gs} will not hurt the outphasing PA efficiency improvement at the back off.

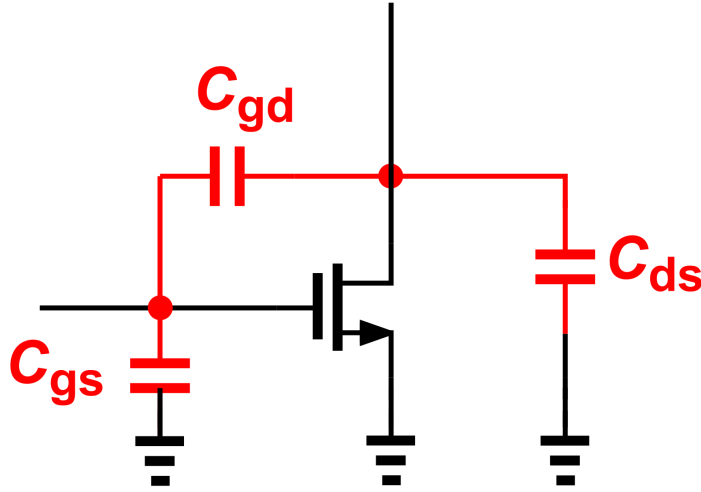


Figure 4.15: Main parasitics in a NMOS

Fig. 4.16 demonstrates a schematic of Chireix's outphasing PA with considering the appearance of C_{ds} in the PA. Comparing equation (4.9) with equation (4.15) for the admittance, equation (4.14) with equation (4.16) in section 4.1, the compensation components only change the DC power consumption, so in the admittance and efficiency calculation, these terms could be directly added to the imaginary part of the admittance and the denominator of the efficiency. So if we set another coefficient α that $\alpha B_c = \omega C_{ds}$, the admittance looking into the two paths of the Chireix power combiner is:

$$Y_k = G_0 \mp jB_0 \pm jB_c + j\alpha B_c \quad (4.39)$$

So the efficiency is:

$$\eta = \frac{\pi}{2} \frac{1}{\sqrt{1 + \frac{B_0^2}{G_0^2}(1 - \gamma - \gamma\alpha)^2} + \sqrt{1 + \frac{B_0^2}{G_0^2}(1 - \gamma + \gamma\alpha)^2}} \quad (4.40)$$

To evaluate the impact from the C_{ds} , Z_0 is chosen to 50Ω and the compensation com-

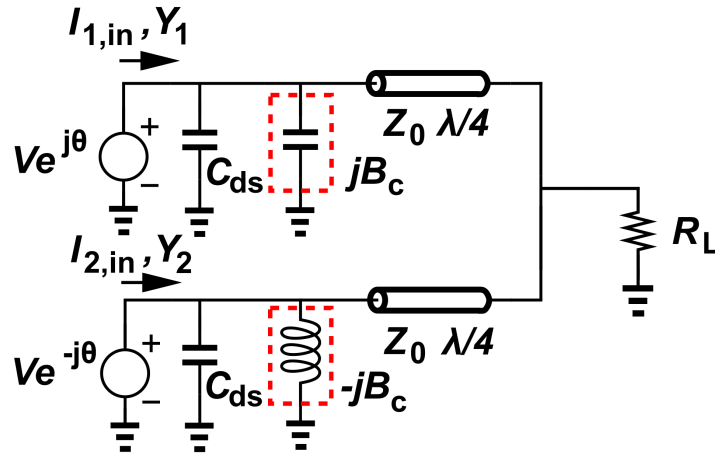


Figure 4.16: Schematic of Chireix’s outphasing PA with parasitic C_{ds}

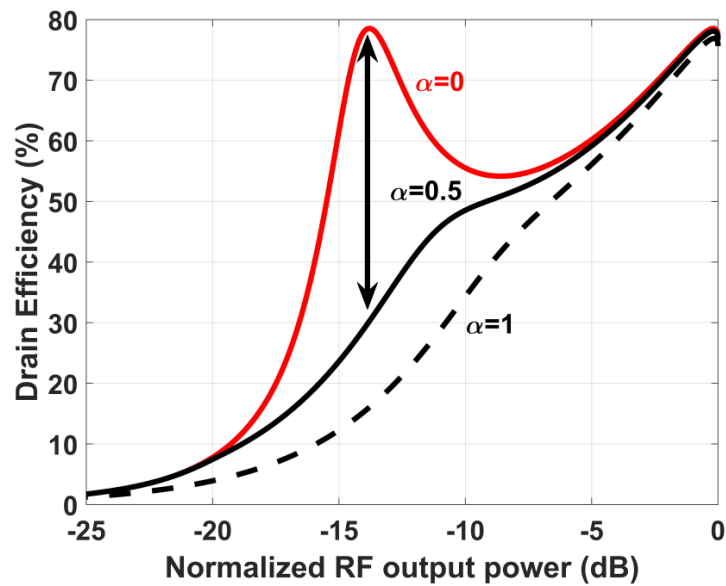


Figure 4.17: η with output power under the different C_{ds} conditions

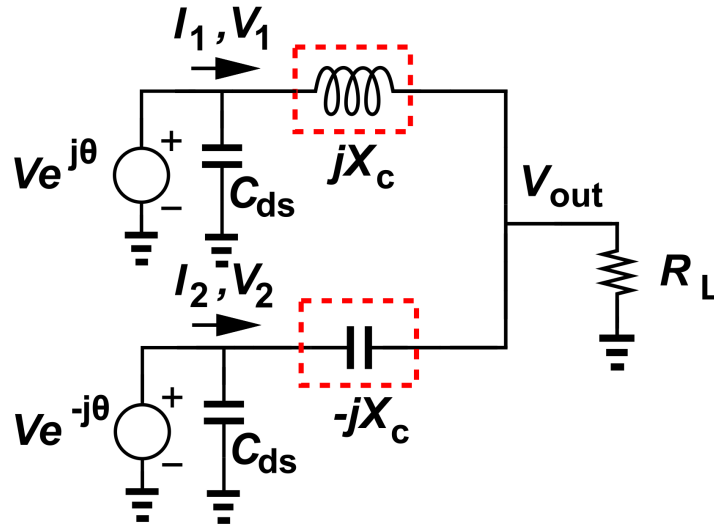


Figure 4.18: Schematic of hybrid mode outphasing PA with C_{ds}

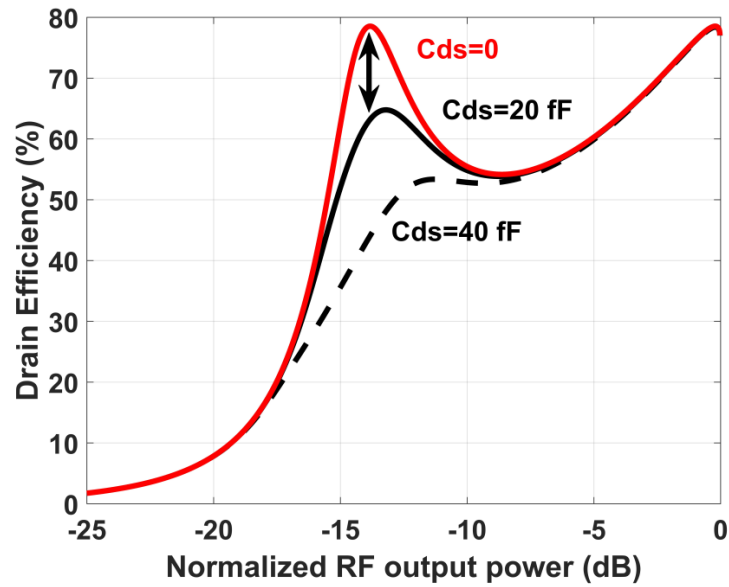


Figure 4.19: η of hybrid outphasing PA with C_{ds} impact

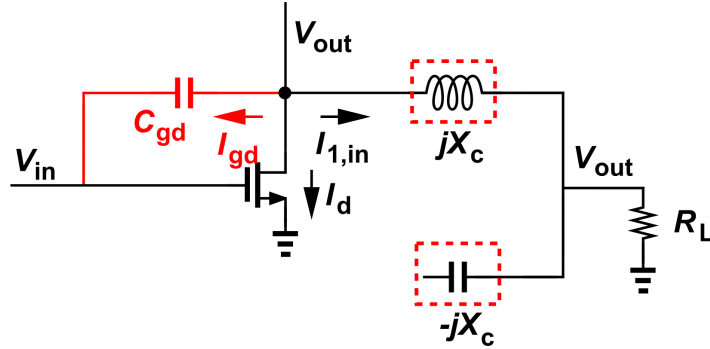


Figure 4.20: Cgd impact for constant envelope operation

ponent is chose to $\gamma = 0.4$. At 30GHz, this compensation capacitor is $42fF$. In 45nm RF SOI technology $240\mu m$ NMOS, the C_{ds} is $50fF$. In Fig. 4.17, η with P_{out} curves are plotted with the $0fF$ ($\alpha = 0$), $20fF$ ($\alpha = 0.5$) and $40fF$ ($\alpha = 1$) conditions. It's clear that even if only $20fF$ C_{ds} shows up, the η drops from 78% to 30% for where the η should peak at power back-off.

As a comparison, Fig. 4.18 shows the schematic of the hybrid outphasing PA with the C_{ds} parasitics. To have a fair comparison result, the extra C_{ds} also chosen to be $0fF$, $20fF$ and $40fF$ for the efficiency calculation. The result is shown in Fig. 4.19 and it's clear with $20fF$ C_{ds} , the η drops from 78% to 65%. From this result, the hybrid outphasing PA provides higher C_{ds} tolerance comparing with the conventional Chireix outphasing PA. This C_{ds} parasitic could be fully tuned out by the load inductor at the fundamental frequency.

For now, the hybrid outphasing PA is still based on several assumptions of the PA operation. One is that the output voltage is a constant amplitude regardless the impedance seen at the drain node. As shown in Fig. 4.20, in above calculation were based on the assumption of PA operation: $I_d = I_{in}$. However, in real operation, the constant envelope of V_{out} is a result of I_{gd} , I_{in} and Y_{in} for PA. Only if I_{gd} is negligible comparing to I_d , the above discussion could be applied for the reality. If C_{gd} exists, that means in

the operation of changing outphasing angle, the impedance seeing into two paths varies from 10Ω to 100Ω and that would change the percentage of the I_{gd} from I_d since the impedance seeing into feedback path does not change. This will result in a changing V_{out} with different outphasing angle θ . Besides, the outphasing angle θ at power back off high efficiency is about 20° which locates to the high impedance range. That means most current flow back from the feedback C_{gd} path rather than flow into the output. This tremendously decrease the efficiency at power back off. To fully handle this issue, as discussed in Chapter 3, the only fully compensation method is to use an inductor to tune out the C_{gd} at the fundamental frequency.

4.4 Implementation of mm-wave Outphasing PA

To design hybrid outphasing PA, the PA should be sized properly first. Two questions need to be answered for the PA operation:

1. How to keep output voltage to be constant regardless the impedance?
2. How to size the NMOS?

Because in the outphasing PA, the input power of the NMOS PA is constant and it pushes the transistor into compression region already, so the load line theory is a specifically good model to address the design. As shown in the Fig. 4.21 and Fig. 4.22, assume the transistor has a load line Z_{opt} for the maximum output power. If $R_L = Z_{opt}$, then the Z_{opt} line is the load line of the PA operation. As shown in Fig. 4.21 that $R_{L2} > R_{L1} > Z_{opt}$, if $R_L > Z_{opt}$, then the NMOS is working at a voltage limited range, which means the fundamental output voltage does not change. As shown in the Fig. 4.22 that $R_{L4} < R_{L3} < Z_{opt}$, if $R_L < Z_{opt}$, then the transistor is working at a current limited range, which means the fundamental output current does not change. However, as demonstrated in the previous section, the voltage limited region is needed in the hybrid outphasing PA.

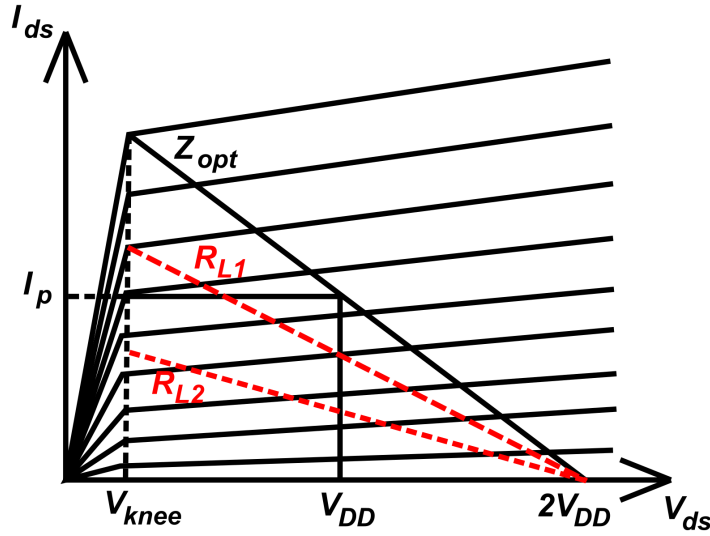


Figure 4.21: Loadline operation for the cases $R_L > Z_{opt}$

As shown in the Fig. 4.23, the back off efficiency improvement occurs at 20° outphasing angle $\gamma = 0.4$ and the peak output power occurs at 90° . Put these two points into Fig. 4.14, it's clear that the at the peak output power, the impedance seeing into two paths of the hybrid outphasing PA is around 10Ω and the impedance at back off peak efficiency is around 100Ω . To match the low load line impedance for peak output power, the transistor should be sized to a low load line impedance. This is also a especially good feature for modern CMOS technology. Because of the low break down voltage, so the low load line impedance means that the current is high which is contributed by the large device. This ensures high output power transmitted out.

As discussed in chapter 3, the $240\mu\text{m}$ NMOS provides a Z_{opt} around 25Ω with class-B bias under $1.2VV_{dd}$. So in here the $240\mu\text{m}$ NMOS is chosen for the PA cell design.

Fig. 4.24 shows a load-pull simulation result for a $240\mu\text{m}$ NMOS with input matching network with C_{ds} neutralization and without C_{gd} unilateralization. From the plot, the peak output power is 15.5 dBm and with a η between 33% to 38% while the peak efficiency is 48%. And at 6dB power back-off, the efficiency drops to 28% which is really

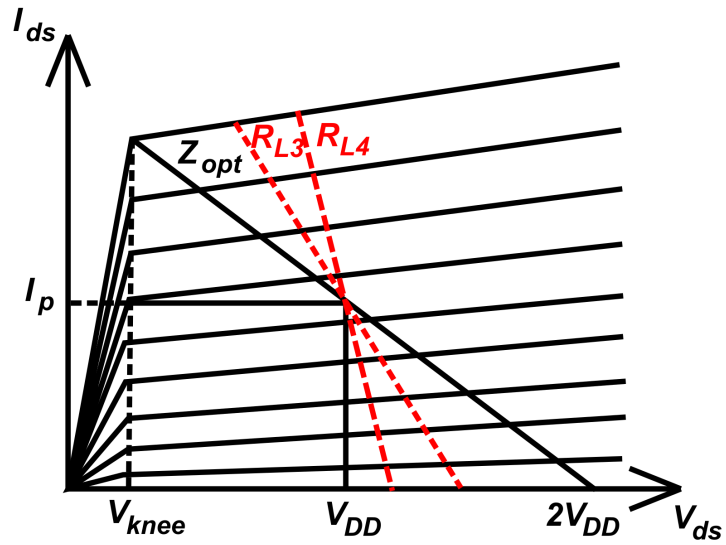


Figure 4.22: Loadline operation for the cases $R_L < Z_{opt}$

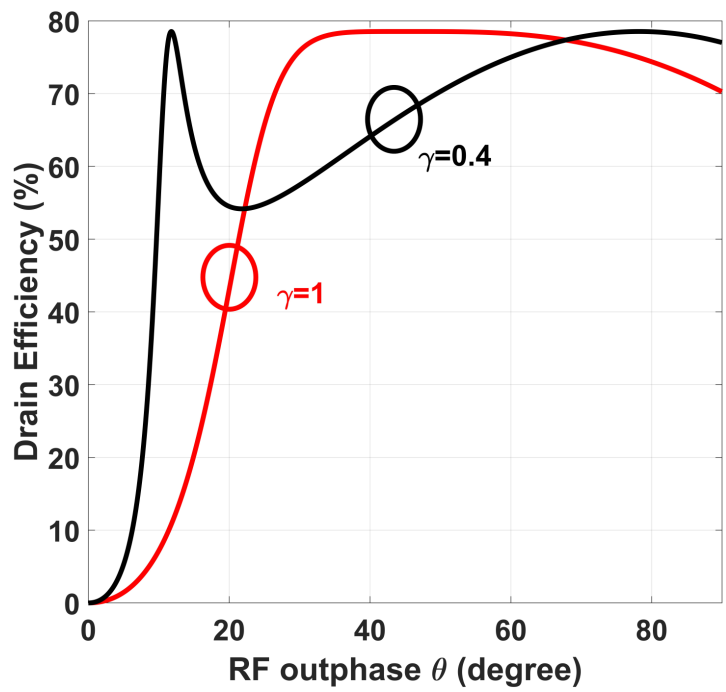


Figure 4.23: η with outphasing angle in hybrid outphasing PA

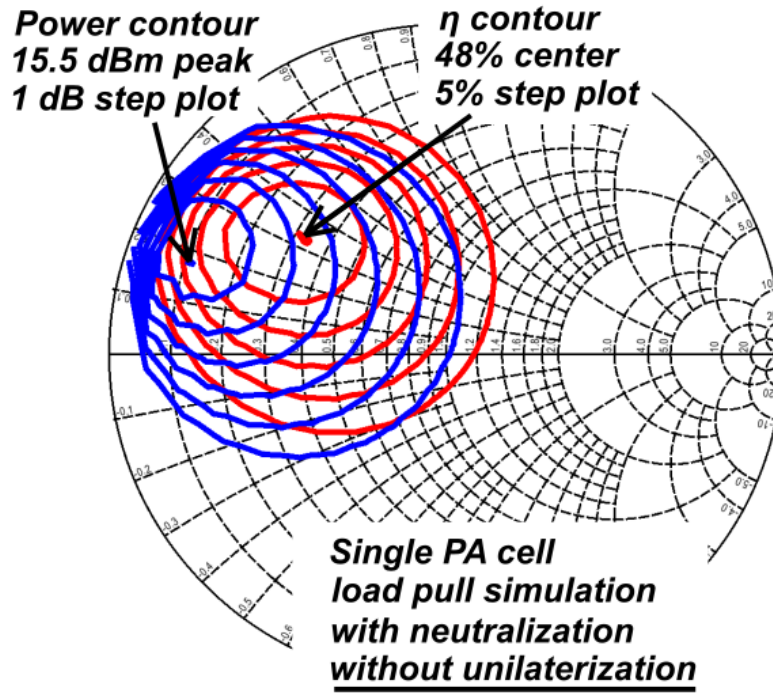


Figure 4.24: Load pull simulation for $240\mu\text{m}$ NMOS with C_{ds} neutralization but without C_{gd} unilaterization

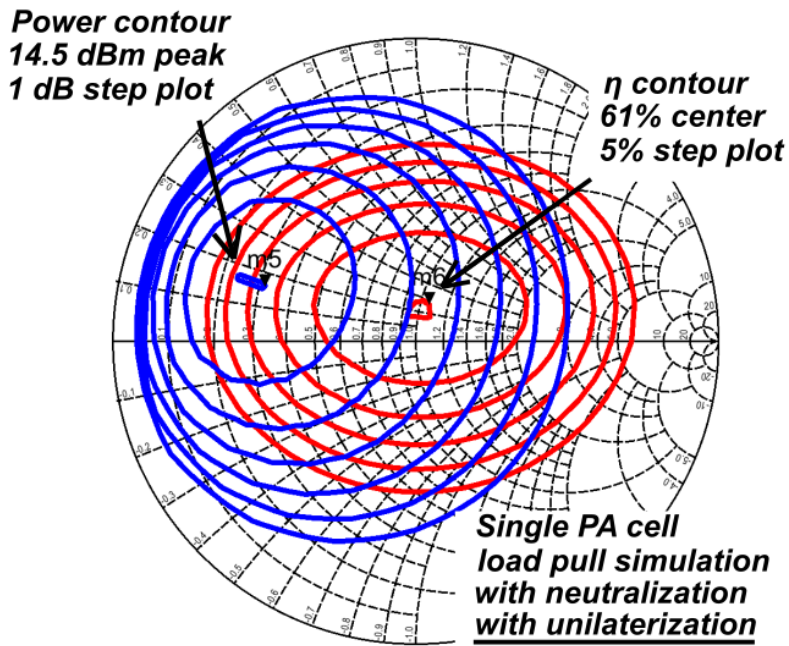


Figure 4.25: Load pull simulation for $240\mu\text{m}$ NMOS with C_{ds} neutralization and with C_{gd} unilaterization

close to the class-B performance. Fig. 4.25 shows the load-pull simulation result with C_{ds} neutralization and with C_{gd} unilateralization. From this plot, the peak output power is 1dB lower with a efficiency as 45% and the 6dB back off has a η as 55%. These two plots show that the 240 μ m NMOS has a peak output power with a load line around 15 Ω in the simulation, while at 100 Ω load point, the efficiency is still as high as 56%.

Now, the question of why the 10 Ω NMOS is not chosen could be answered for the following reasons:

1. The larger device requires more routing for the combination, this naturally brings more loss and reduce the performance.
2. With the lower peak output power impedance Z_{opt} , the efficiency contour would also move to lower impedance which will reduce the η at 100 Ω . In other words, this will hurt the η at power back-off.

Fig. 4.26 shows a full schematic of the hybrid outphasing PA. The unilateralization network is designed using a 1pF DC blocking capacitor in series with a 380pH inductor to accurately compensate the C_{gd} at fundamental frequency 30GHz. A 200pH inductor load is used to compensate the NMOS parasitic C_{ds} and the layout parasitic capacitance from the unilateralization inductor, the capacitance from the combiner and the parasitic capacitance from itself. A shunt 120pH inductor is used for the input matching. In this design, since the unilateralization network comprise a low impedance feedback at 6GHz and make the stability factor μ lower than 1, a 600pH shunt inductor with a DC blocking capacitor is added at the gate of NMOS to short this reflected current. However, as shown in the Fig. 4.27, even with this shunt path, μ factor is still lower than 1 around 24GHz. So a high pass stabilization circuit is added in series with gate as shown in the schematic to reduce the gain at 24GHz but have less reduction at 30GHz.

From choosing $\gamma = 0.4$ for 30GHz design, the calculated compensation series inductor is 215pH and the capacitor is 130fF. The inductor is designed by a slot transmission

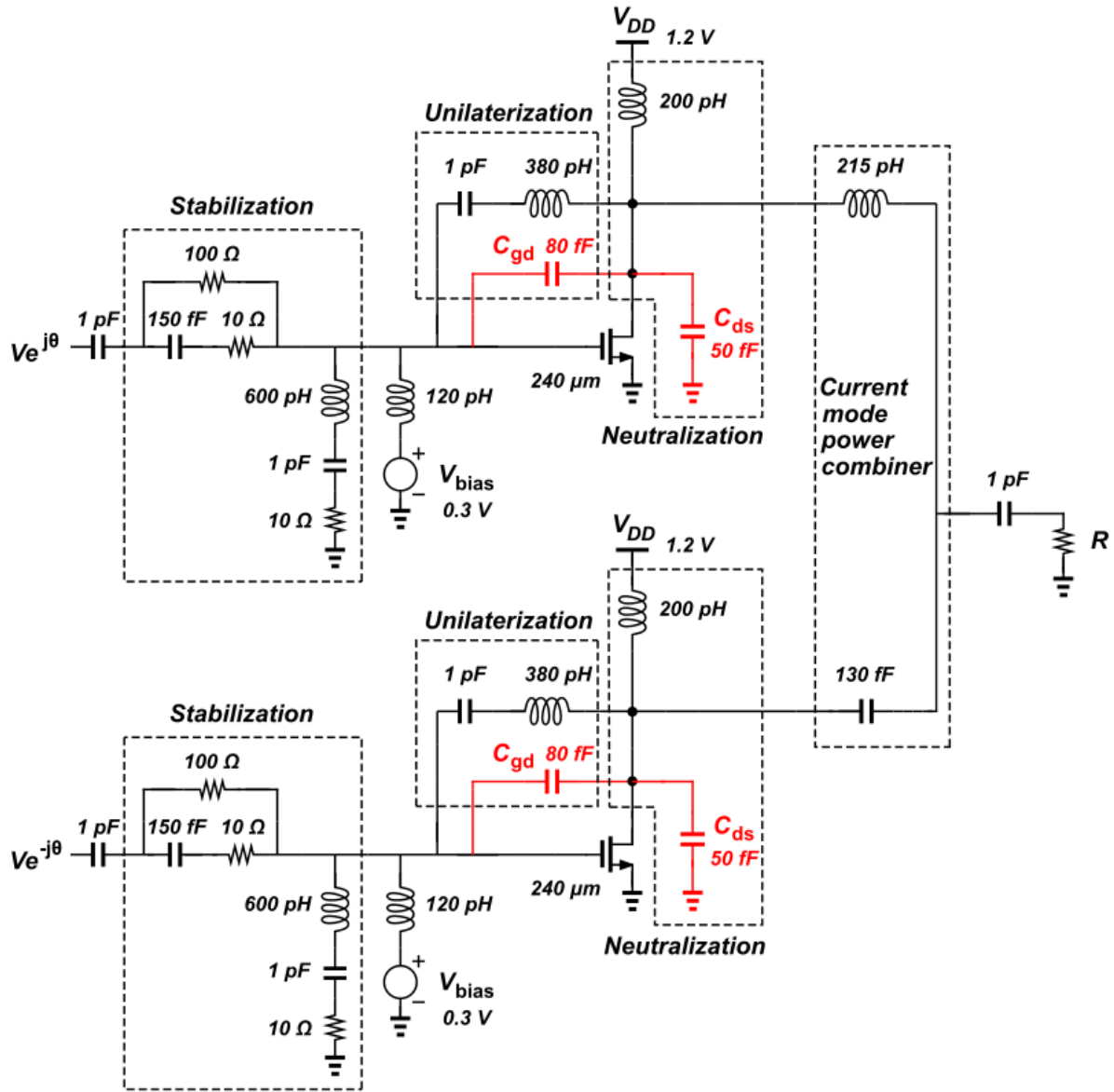


Figure 4.26: Schematic of the hybrid outphasing PA

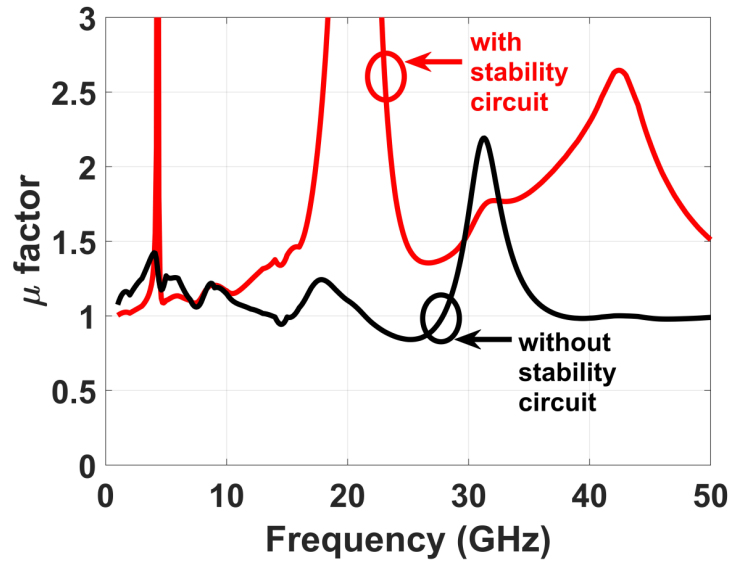


Figure 4.27: Stability of the single PA with and without stabilization circuit

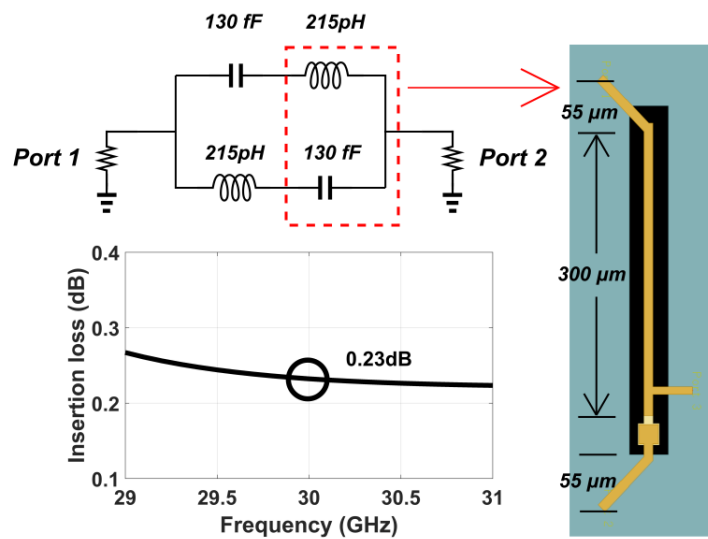


Figure 4.28: A back to back simulation for the current mode power combiner

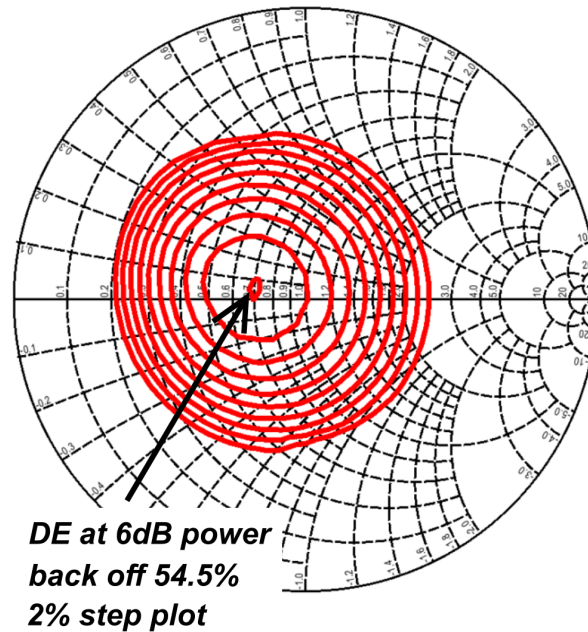


Figure 4.29: Load pull simulation for 6-dB power back off

line with a $10\mu\text{m}$ wide $4\mu\text{m}$ thick metal. The capacitor is chosen for high Q MIM from the process to reduce the loss. As shown in the Fig. 4.28, a back to back configuration is used with two current mode combiners. From the EM simulation result with using EMX, the loss of the combiner is 0.23dB, it's much less comparing to the Chireix's combiner that close to 1dB loss of the $\lambda/4$ transmission line. The layout of the combiner is also shown in the figure.

The Fig. 4.29 shows the simulated load pull result at 6dB power back off which is set by the outphasing angle to be 20° . This simulation demonstrates the back off η variation at different impedance due to the VSWR from antenna. The result shows at 50Ω impedance, the η is 52.5% while at 35Ω , the η is at its peak 54.5%. At 70Ω , for another $VSWR = 1.4$ impedance, the η is 48.5%. This shows high VSWR tolerance of this hybrid mode outphasing PA.

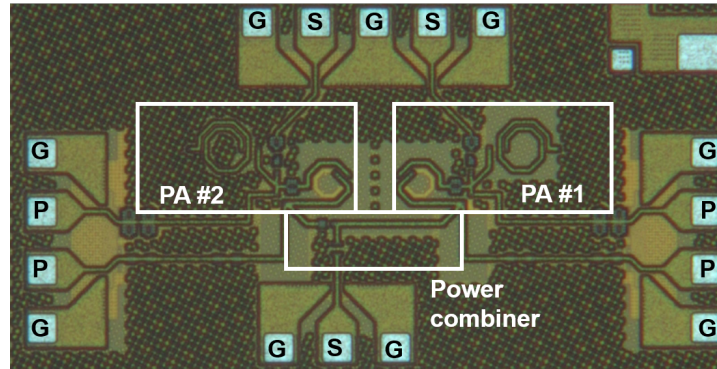


Figure 4.30: micrograph of the implemented hybrid outphasing PA

4.5 Measurement of Outphasing PA

The Fig. 4.30 shows a micrograph of the implemented GlobalFoundries 45nm CMOS SOI hybrid outphasing PA. Chip size is $920\mu m * 1790\mu m$. The chip is biased under $1.2V V_{DD}$ and $0.3V V_{gs}$ as the class-B PA. Fig. 4.31 shows a comparison of the measured and simulated S parameters. Since this is a three-port network, the PA was measured one by one. One PA is turned on with $0.3V V_{gs}$ class-B bias under $1.2V V_{DD}$ and the other PA is off with $0V V_{gs}$ and $0V V_{DD}$. From this comparison, each PA has 9dB small signal gain S_{21} and the simulation matches the measurement results well. In fact, the imbalance of the S_{21} in simulation result is worse than the measurement result. S_{11} and S_{22} is -15dB that the circuit matches well. The S_{33} is not sufficient because in the design, two paths should be both turned on.

Fig. 4.32 shows the large signal and power measurement setup. Outphasing signals are generating from the Matlab and sent to the Keysight M8195A arbitrary waveform generator with 8GHz IF carrier. Two Marki MM1-1044HS mixers up-convert the 8GHz IF to 30GHz RF. The outphasing signals are amplified with two Spacek Labs SG2612-30-24 amplifies. Two Marki FB-3270 band pass filter are used to filter the out band signals. After device under test (DUT), the output signal of the hybrid outphasing PA is down

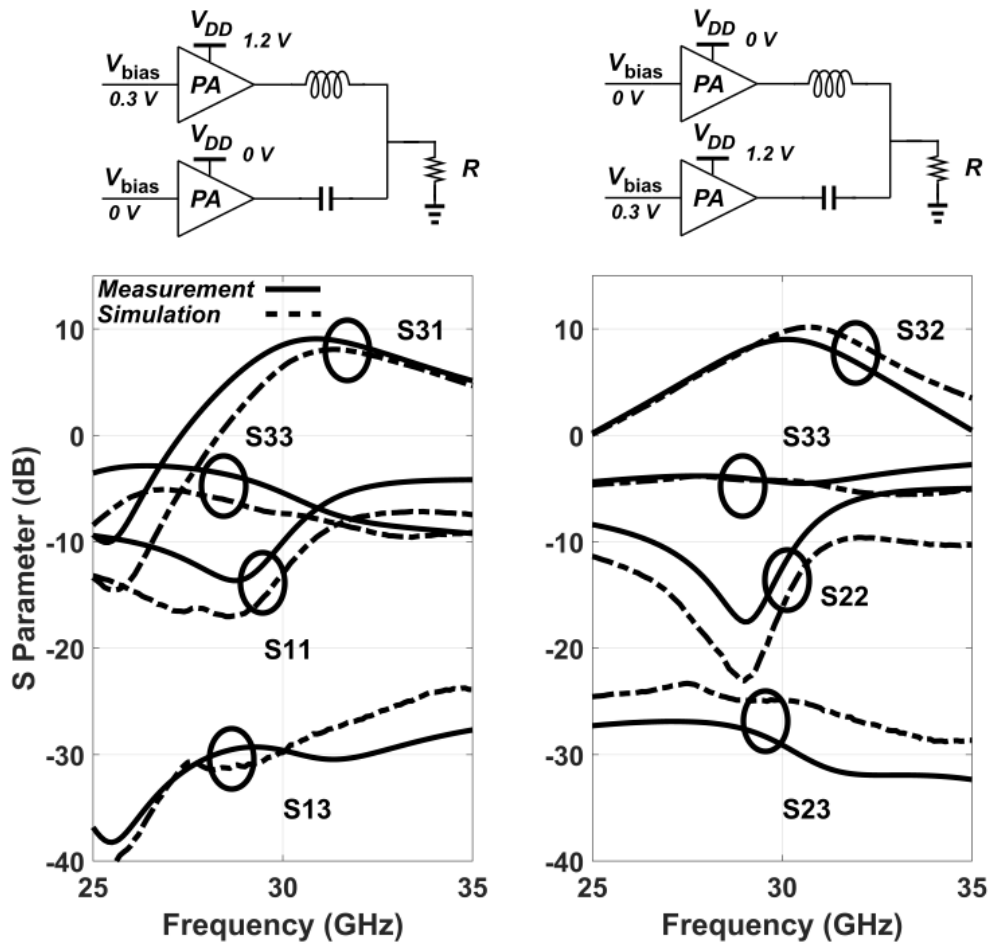


Figure 4.31: Comparison of measurement and simulation result of small signal S parameter

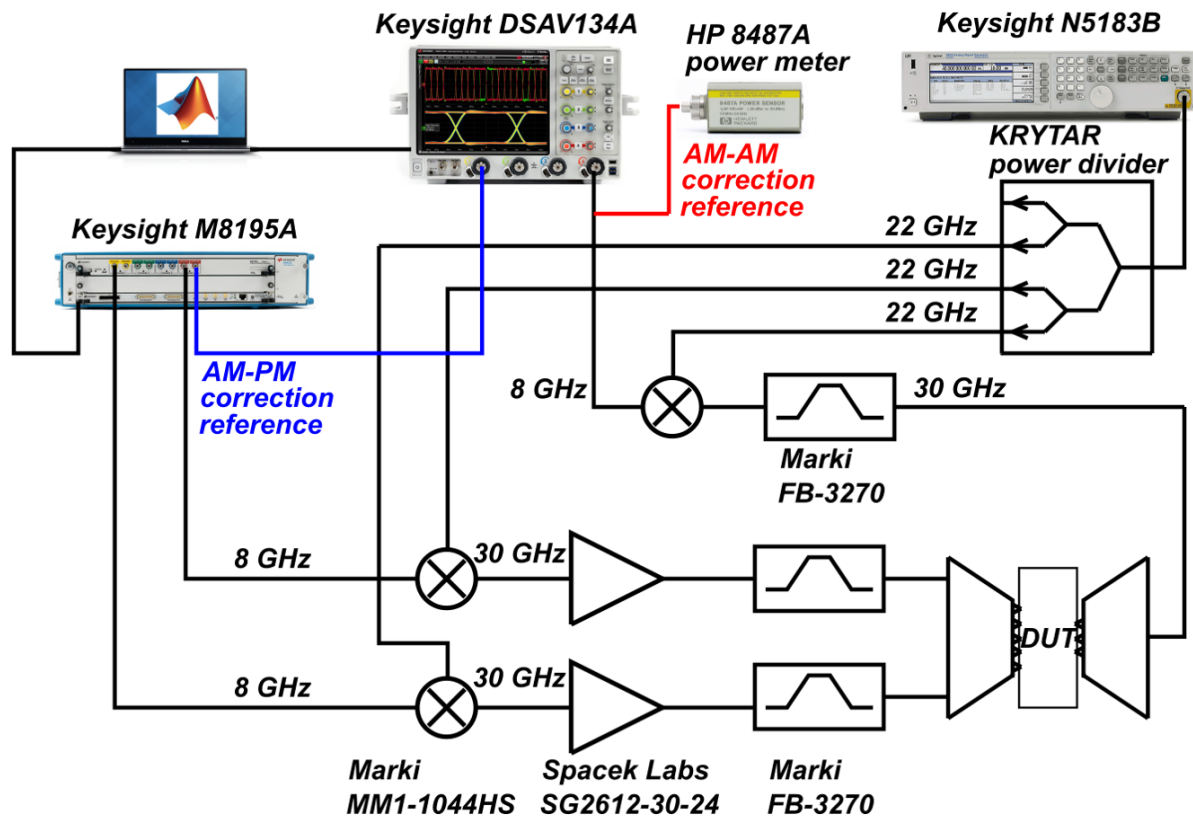


Figure 4.32: power performance measurement and EVM measurement setup

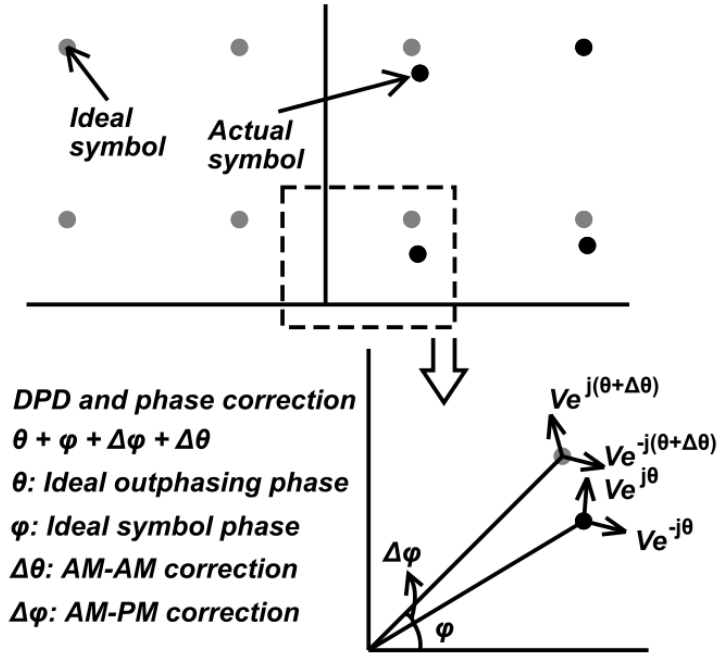


Figure 4.33: Theory of phase only DPD

converted by the Marki MM1-1044HS mixer to 8GHz IF carrier and is demodulated by the Keysight DSAV134A oscilloscope.

Fig. 4.33 shows the theory of phase only DPD. For symbols’ amplitude information, it could be achieved by choosing the proper outphasing angle θ . For symbols’ phase information, it could be achieved by the common phase angle ψ . This means for a symbol, the theoretical outphasing input should be:

$$S1 = A\cos(\omega t + \theta + \psi) \tag{4.41}$$

$$S2 = A\cos(\omega t - \theta + \psi) \tag{4.42}$$

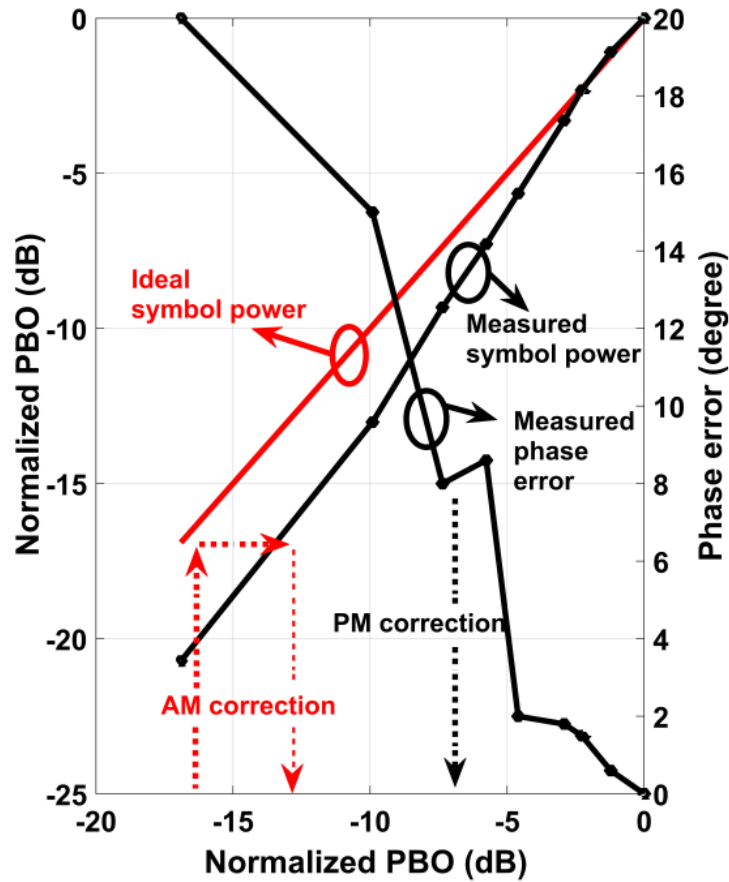


Figure 4.34: AM and PM LUT for correction

However, due to the loss mismatch on the current combiner that the capacitor and inductor have different quality factor (Q) and the non-identical PA cell in real world because of the processing variation, even with the proper outphasing angle, it still result in amplitude mismatch. A correction outphasing angle $\Delta\theta$ could be added to help the correction. Also, the common phase could exist mismatch between the sent and received signals. A correction common angle $\Delta\psi$ could be added.

As shown in the Fig. 4.34, the output power amplitude and phase are measured relative to outphasing angle, the figure shows the AM and PM errors that is used as a LUT. Based on this LUT, the outphasing angle correction $\Delta\theta$ for amplitude and the common

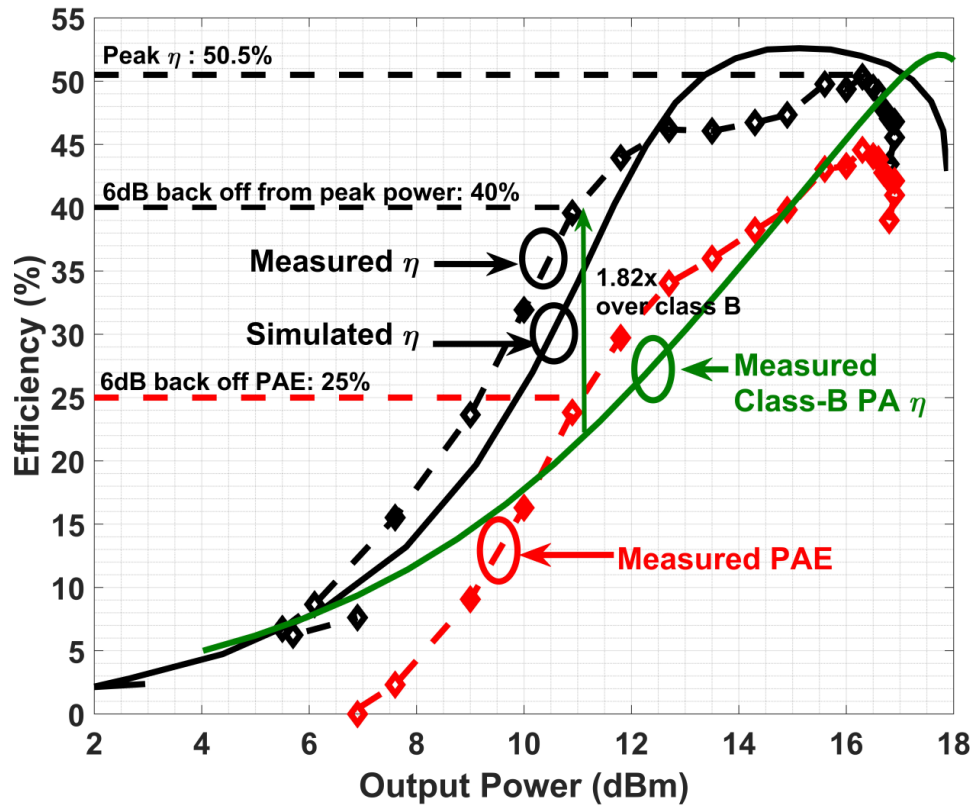


Figure 4.35: Measured drain efficiency comparing to the simulation result and the inductive-coupling neutralization class-B PA

phase angle $\Delta\psi$ are calculated and compensated with the Matlab code. With this simple LUT correction, the drain efficiency and the PAE are measured.

The measurement result is compared to the simulation result and shown in the Fig. 4.35, the P_{sat} is 17dBm with 50.5% drain efficiency (DE). At 6dB power back off, the DE is 40% while the PAE is 25%. Comparing the measurement result with the simulation result, P_{sat} is lower than the expected number and it is contributed by the under estimation of the loss of RF pads. However, the efficiency is close to the simulation. This measurement also compares to the inductive-coupled neutralization PA described in Chapter 3. These two PAs have similar DE at peak P_{sat} , however, at 6dB output power back off, the hybrid outphasing PA shows 1.82 times higher DE than the class-B PA.

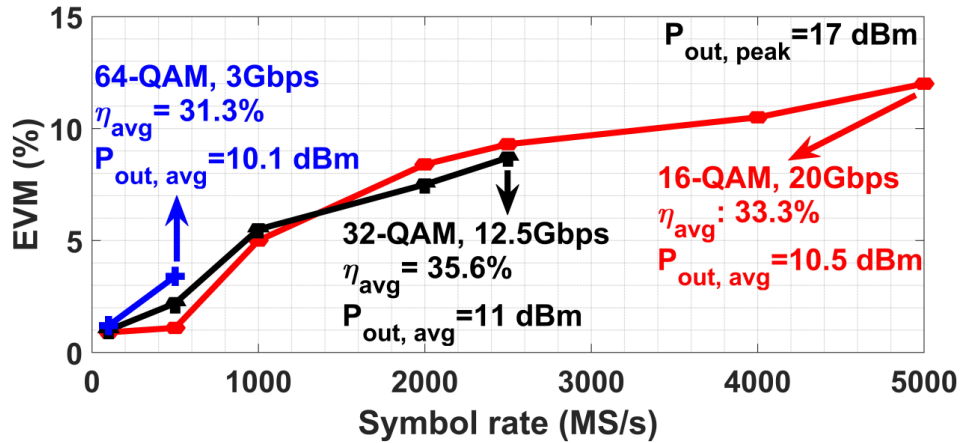


Figure 4.36: EVM results for different QAM signals with different symbol rate

Fig. 4.36 shows the measurement result of the EVM with QAM16, QAM32 and QAM64 at different data speed. All the measurement are done with setting the peak symbol power level to be the P_{sat} . For different modulation scheme, the PAPR is different, but around 6dB. The measurement shows that the average efficiency for different conditions are all above 30%. At low data speed such as 500MSymbol/s for QAM16, the EVM is less than 2%. As shown in the figure, this hybrid outphasing PA achieves a record 20Gbps speed with QAM16.

Fig. 4.37 and Fig. 4.38 show the ACPR for 100MSymbol/s and 500MSymbol/s data speed. Without using the LUT, the ACPR is -22dBc and -21.3dBc respectively. The ACPR is improved by nearly 6dB with using the LUT.

The following table shows a comparison of the hybrid outphasing PA with the state of art. This is the first true envelope outphasing PA at mm-wave band.

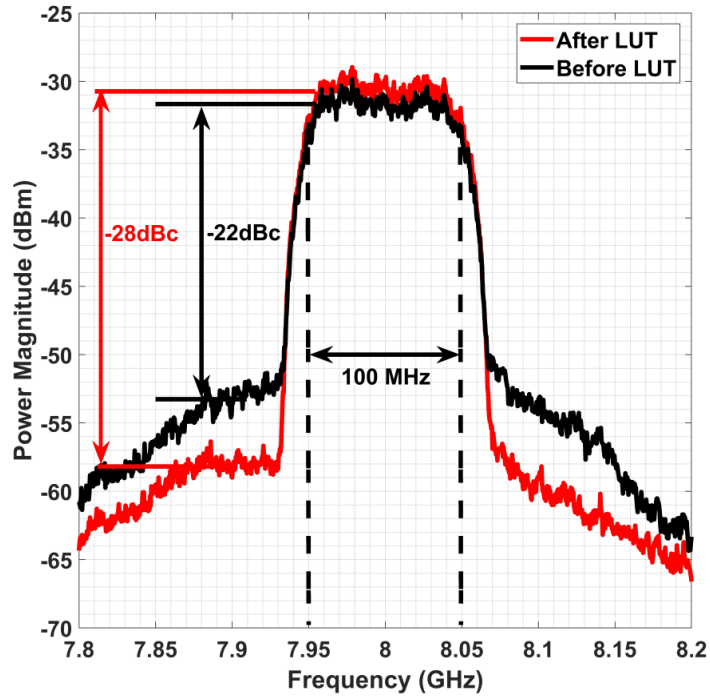


Figure 4.37: ACPR results with and without using LUT at 100 MSymbol/s data speed

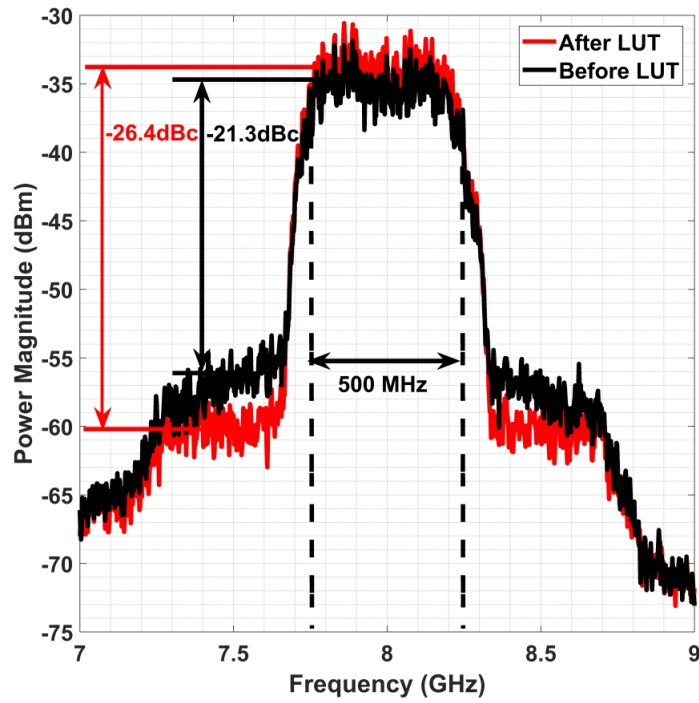


Figure 4.38: ACPR results with and without using LUT at 500 MSymbol/s data speed

	[22]	[23]	[29]	[30]	This Work
Technology	40nm CMOS	130nm SiGe	45nm SOI	130nm SiGe	45nm SOI
Architecture	Outphasing	Outphasing	Outphasing	Doherty	Outphasing
Supply (V)	1	4	1	1.5	1.2
Frequency (GHz)	59.5-67	28	25.5-30	23.3-39.7	30
Gain (dB)	26	14	-	18.2	7
P_{sat} (dBm)	15.6	23	17.1	16.8	17
Peak η (%)	25*	43	56	29.4	50.5
η @6dB PBO	9*	35	38	25.4	40
Modulation	QPSK	64QAM OFDM	64QAM	64QAM	16QAM
Data Rate (Gb/s)	3.52	0.48	6	3	0.4
EVM (dB)	-34	-30.5	-29.7	-27	-41
P_{avg} (dBm)	10.8	14.3	10.7	9.2	-36
η @ P_{avg} (%)	-	25.3	36	18.5	-38
Area (mm^2)	0.96	0.56	34	14.4	-28.4
* for PAE instead of η			-	1.76	11
					35.6
					31.2
					1.65

4.6 Limitation of Outphasing PA

In the previous sections, the designed hybrid outphasing PA is demonstrated in detail and the average efficiency improvements are shown. However, the outphasing PA has several limitations at the mm-wave band when a higher specification is required. For example, in the designed outphasing PA, the P_{sat} is 17dBm. In the normal PA design, choosing twice the PA size or choosing stacking topology could help improve the maximum available current or voltage swing to improve the output power. For twice the device size, the Z_{opt} of the NMOS turns to be 12.5Ω , half of the 25Ω load line impedance. This will shift the load pull contours to lower impedance center. As demonstrated in the section 4.5, the γ was chosen to be 0.4 to cover 10Ω to 100Ω range. If the load pull contour shifts to lower impedance center, the average efficiency drops.

Another solution is to use a stack-FET topology. As shown in the Fig. 4.39, instead of using single NMOS PA cell, the PA cells are replaced by the stack FET PA. For the top transistor, the impedance looking into two paths are still same as shown in the Fig. 4.14, however, for the bottom transistor, the impedance Z_3 and Z_4 is always $\frac{1}{G_m}$. Based on the theoretical derivation, the back off η improvement comes from the impedance change with phase change. This impedance change reduces the DC power consumption. For the bottom transistor, the impedance is close to a constant value. Thus, the efficiency improvement at back-off is only shown on the top transistor. The total PA cell effectively does not have back-off efficiency improvement.

The two drawbacks above could be attributed to modern CMOS technology. However, the outphasing PA topology naturally has a disadvantage. The PA cell has to be pushed into the compression region for the highest PAE from the PA cell. However, the PA in compression region has less gain than small signal. Moreover, with changing the outphasing angle, the smaller output power is comprised by the two paths of PA cells without

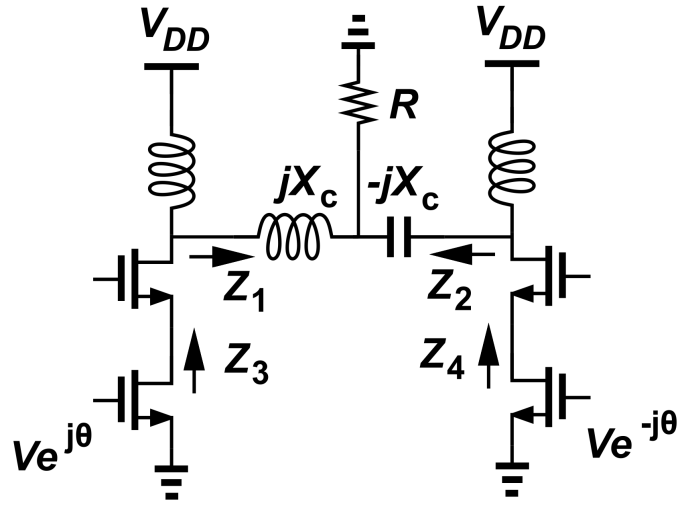


Figure 4.39: Hybrid outphasing PA with using stack FET PA cell

changing the input power, it means in the power back-off region, the gain drops with the power, e.g. 6dB power back off brings 6dB gain drop. So it is difficult to keep the PAE to high in the outphasing PA design if the PA cells could not provide enough high gain. Unfortunately, the modern single stage PA at mm-wave band could provide very limited gain as shown the MAG in chapter 3. The MAG is usually around 15dB. If loss and stability are considered into the design, the gain is usually reduced to around 10dB.//

Chapter 5

mm-wave Doherty PA Design

In chapter 4, the mm-wave outphasing PA has been designed, the improvement of the drain efficiency (η) at power back-off is significant. However, due to the power combining topology that utilizes constant envelope signals in the outphasing PA topology, the gain drops with the power back-off. This hurts the effective PAE performance. The Doherty PA combines two PAs with different power to achieve high gain and high efficiency at both peak output power and power back-off. This topology naturally avoids the challenges in outphasing PA. In this chapter, a mm-wave Doherty PA design methodology is demonstrated in detail.

5.1 Conventional Doherty PA Design Theory

To understand the constraints of the Doherty PA Design in modern process for mm-wave frequency range, the conventional Doherty PA design theory is reviewed in this section.

In 1936, W. H. Doherty proposed a combining PA topology to improve the efficiency of the PA [4]. The efficiency calculation at back-off, the power level, and transistor sizing are

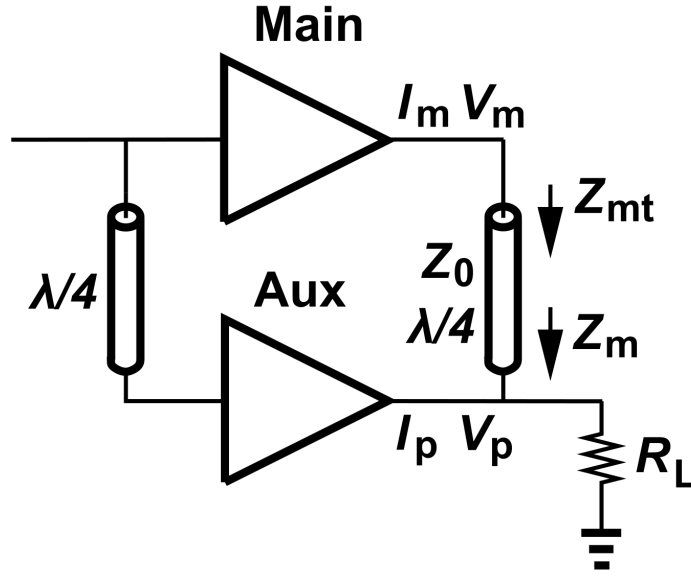


Figure 5.1: Conventional doherty PA topology

derived in [5,31]. Fig. 5.1 shows the topology of the conventional Doherty PA structure. Based on this topology, we have the following expressions:

$$Z_m Z_{mt} = Z_0^2 \quad (5.1)$$

$$I_m V_m = I_{m,out} V_{out} \quad (5.2)$$

$$Z_{mt} = \frac{V_m}{I_m} \quad (5.3)$$

$$Z_m = \frac{V_{out}}{I_{m,out}} \quad (5.4)$$

From above equations, we have:

$$I_m = V_{out}/R_L \quad (5.5)$$

From this equation, it is clear that the current provided by the main PA increases with increasing of the output voltage, same as output power. So from:

$$I_m V_m = I_{m,out} V_{out} \quad (5.6)$$

we have:

$$\begin{aligned} V_m &= V_{out} \frac{I_{m,out}}{I_m} \\ &= I_{m,out} * R_L \end{aligned} \quad (5.7)$$

When the auxiliary PA gradually turns on, the output voltage V_{out} increases with increasing the current I_p and from equation (5.5), the output current from main PA I_m increases with the output voltage V_{out} . However, the voltage amplitude of the main PA V_m remains the same. Thus, the output power at the main PA end increases due to the increase of the output current I_m and the output power at the load end increases due to the increase of the output voltage V_{out} .

Fig. 5.2 shows the load-line impedance change looking from the main PA at the back-off peak efficiency point to the peak output power point. As shown in the figure, the impedance changes from $Z_{backoff}$ to Z_{peak} . Now, the efficiency at these two points can be calculated. For the RF power:

$$\begin{aligned} P_{backoff,RF} &= \frac{1}{2} Re\{V_{backoff} * I_{backoff,fund}^*\} \\ &= \frac{1}{2} * (V_{dd} - V_{knee}) * \frac{1}{2} I_{backoff} \\ &= \frac{1}{4} * (V_{dd} - V_{knee}) * I_{backoff} \end{aligned} \quad (5.8)$$

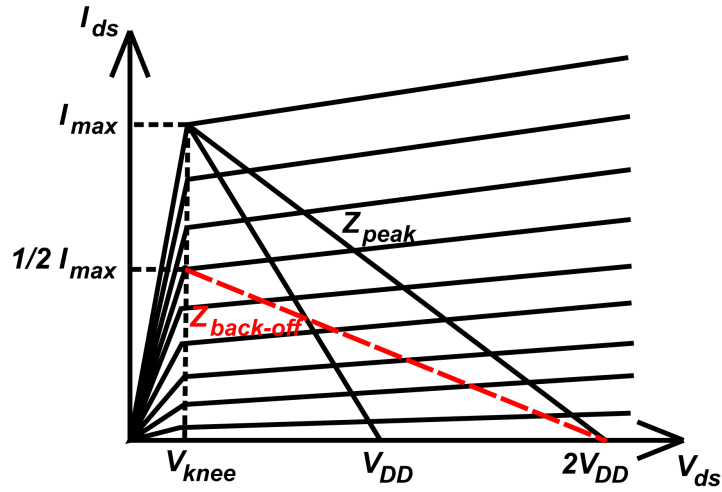


Figure 5.2: Conventional Doherty Load Line

The DC power consumption is:

$$\begin{aligned}
 P_{backoff,DC} &= V_{dd} * \frac{1}{\pi} I_{backoff} \\
 &= \frac{1}{\pi} V_{dd} I_{backoff}
 \end{aligned} \tag{5.9}$$

The efficiency is:

$$\begin{aligned}
 \eta &= \frac{P_{backoff,RF}}{P_{backoff,DC}} \\
 &= \frac{\pi}{4} \frac{V_{dd} - V_{knee}}{V_{dd}}
 \end{aligned} \tag{5.10}$$

The theoretical efficiency is then 78% if V_{knee} could be neglected. And from this calculation, it is observed that when the load impedance R_L higher than the load line impedance Z_{opt} , the theoretical peak efficiency is always 78%.

For this reason, when the peaking PA gradually turns on, the main PA remains in compression region and the impedance seeing by the main PA gradually decreases. So the main PA keeps the efficiency as 78%.

Similarly for the auxiliary PA, the impedance seeing from the auxiliary PA is infinite when

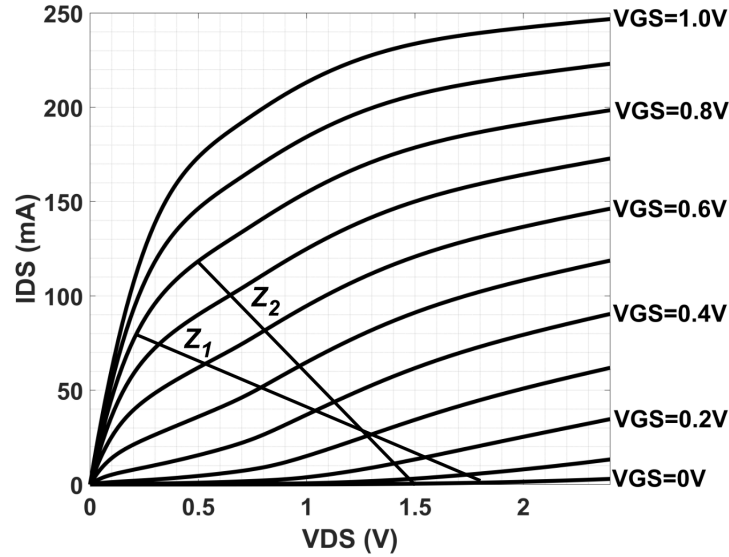


Figure 5.3: IV curve of a $240\mu\text{m}$ NMOS

the auxiliary PA is off. The impedance gradually decrease from the high impedance to low impedance when the auxiliary PA is gradually turned on. Thus, the auxiliary PA always in the high efficiency range.

Because of this load modulation, two PAs operate together at high efficiency from total peak output power to the power back-off at which point the auxiliary PA turns on.

However, the above calculations are based on the ideal transistor model. In other words, in the efficiency calculation, we see that the peak efficiency remains high in different load impedance if $R_L > Z_{opt}$ is based on the IV curve as shown in Fig. 5.2. As a comparison, Fig. 5.3 shows an IV plot for a $240\mu\text{m}$ NMOS in GlobalFoundries 45nm SOI technology. In this figure, following differences are observed comparing to the ideal NMOS model:

1. No clear knee voltage V_{knee} in I-V curves at low input power region.
2. At current saturation region, the current keeps increasing with the V_{DS} instead of remaining constant.

3. Even with $V_{GS} > 0.7V$, I_{DS} could change in a range of 1.5 times in compression region.

As a comparison of this realistic device IV curve to the conventional theoretical IV curve,

the modern device shows several characteristics that need to be considered in designing the Doherty PA:

1. In the conventional Doherty PA, the maximum power is associated with maximum voltage swing and maximum current swing at the same time. In other words, the maximum power is associated with a fixed load impedance Z_{opt} . In the modern devices, the peak output power is associated with a range of the load impedance. For example, with a particular V_{GS} taken as the input power, a smaller V_{DS} voltage swing could be chosen with a relative higher current swing or a larger V_{DS} voltage swing could be chosen with a relative smaller current swing as shown in Fig. 5.3.
2. The peak PAE at back-off for main PA in conventional Doherty PA is based on the assumption that $V_{DS} - V_{knee}$ is close to V_{DD} , or that V_{knee} is not a dominant factor in the efficiency calculation. That is, the conventional theoretical η instead of PAE. If we calculate PAE, then we need to include the consideration of the input power. As a first-order estimation, we could look at the power back-off region, e.g. low VGS I-V curves. Although high load impedance could help to push the voltage swing to be close to $2*(V_{dd} - V_{knee})$, but the current is very low. In other words, although the drain efficiency could be high, the PAE is low due to the low output power relative to the input power. A smaller load impedance would reduce the voltage swing but increase the current swing.
3. The quarter wavelength transmission line is used to convert the impedance so that from the power back-off to peak output power, the impedance looking from the main PA increases. However, in this figure, we could see that changing the impedance from high to low results in the voltage swing changing from high to low, so the power remains nearly the same.

5.2 Combiner-less Doherty PA Implementation in 45-nm SOI

From the discussion of section 5.1, it's clear that the load modulation required by the main PA comes from the conventional theoretical IV curve that provides high efficiency and higher output power from high impedance to Z_{opt} . And this constrains the impedance change from high to low. Because of this requirement, the quarter wavelength transmission line is used to transfer the impedance change trend. However, from Fig. 5.3, changing the impedance from high to low could not provide higher output power. This phenomenon illustrates that using the conventional Doherty PA topology could not provide the extra 3dB more output power when the auxiliary PA turns on. This also demonstrates that the impedance changing trend for the main PA could from low to high. This low to high impedance trend is suitable for a modern device, so the quarter wavelength transmission line could be omitted. In this section, a combiner-less Doherty PA design in 45nm SOI CMOS is demonstrated. The proposed new Doherty PA topology is shown in Fig. 5.4.

As illustrated in chapter 4 that the 45nm SOI CMOS could provide limited gain due to the C_{gd} , in this Doherty PA design, the inductive compensation method for unilateralization is still used to improve gain and PAE. Here is the design methodology:

1. Considering that at the power back-off range, the auxiliary PA turns off and only main PA turns on. So the impedance seeing by the main PA is the load impedance, 50Ω . This means that in the load pull simulation at the compression region, we should see the high output power contour include the 50Ω as low load impedance. Fig. 5.5 shows the schematic, PAE and P_{out} contour of the load pull simulation with choosing $120\mu m$ NMOS. In this simulation, the input matching has done because with using 4-stack topology, the output to input feedback is very low especially with the inductive unilateralization. The

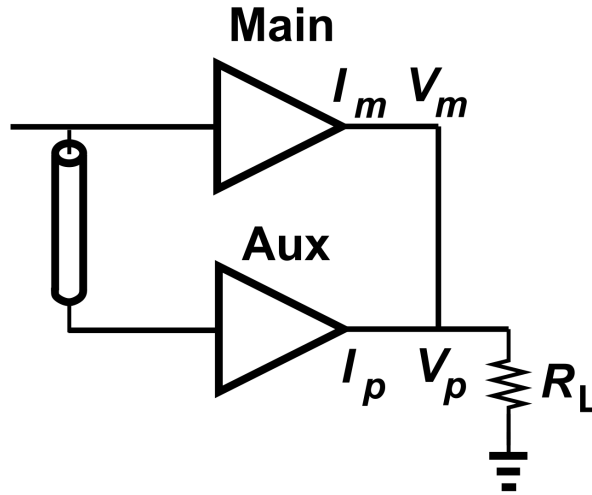


Figure 5.4: Proposed combiner-less Doherty PA topology.

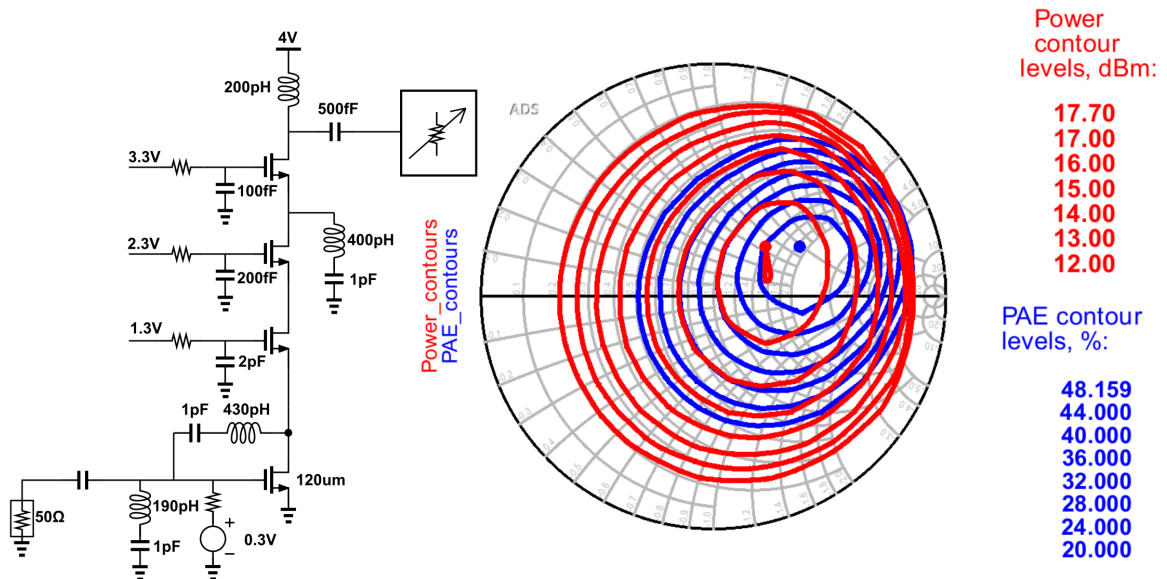


Figure 5.5: Load pull simulation schematic, PAE and P_{out} contour for 4-stack, $120\mu m$ NMOS PA cell including input matching network and unilateralization network

PA is set to class-B bias. From the simulation result, in the 50Ω to 100Ω load impedance range, the output power keeps the same to 17dBm.

2. Without the combiner, the voltage swing on the main PA and the auxiliary PA should be same. Because the main PA utilize the 4-stack topology for high output power, the auxiliary PA should also be 4-stack. To reduce the DC power consumption at the power back off, the auxiliary PA has to be biased in deep class-C mode. However, class-C bias reduces gain. To compensate gain, the unilateralization is also applied to the auxiliary PA. The unilateralization is designed with the class-B bias condition because the auxiliary PA working at the large signal that could turn it on. This could be adjusted for the AM-PM performance. Because the auxiliary PA has to provide more power that combining with the main PA to achieve high output power, the auxiliary PA should be sized larger than the main PA. Here is the trade off: if the NMOS in auxiliary PA have small size, the output power is low and the back off high efficiency range is small; if the NMOS in auxiliary PA have too large size, the DC power consumption could be high even with deep class-C bias condition and this will reduce the back off efficiency for the total PA performance. In this design, 2 times sizing of the NMOS comparing to main PA is chosen for the auxiliary PA design.

3. Due to the AM-PM performance being different in the main PA and auxiliary PA, a phase compensation is required at the input of the PA so that the output current of each PA are in phase. In this design, a Wilkinson power splitter is used at the input and additional transmission line is added in one path for phase compensation as shown in Fig. 5.6. A small capacitor $60fF$ is in series connected at the output of the main PA to compensate the load inductance of the auxiliary PA.

Fig. 5.7 shows the simulation of small signal S parameter of this Doherty PA. The center frequency is designed to 39GHz. S11 matched very well. The small signal gain is 14dB at the center frequency. This PA is narrow band because the phase matching between two

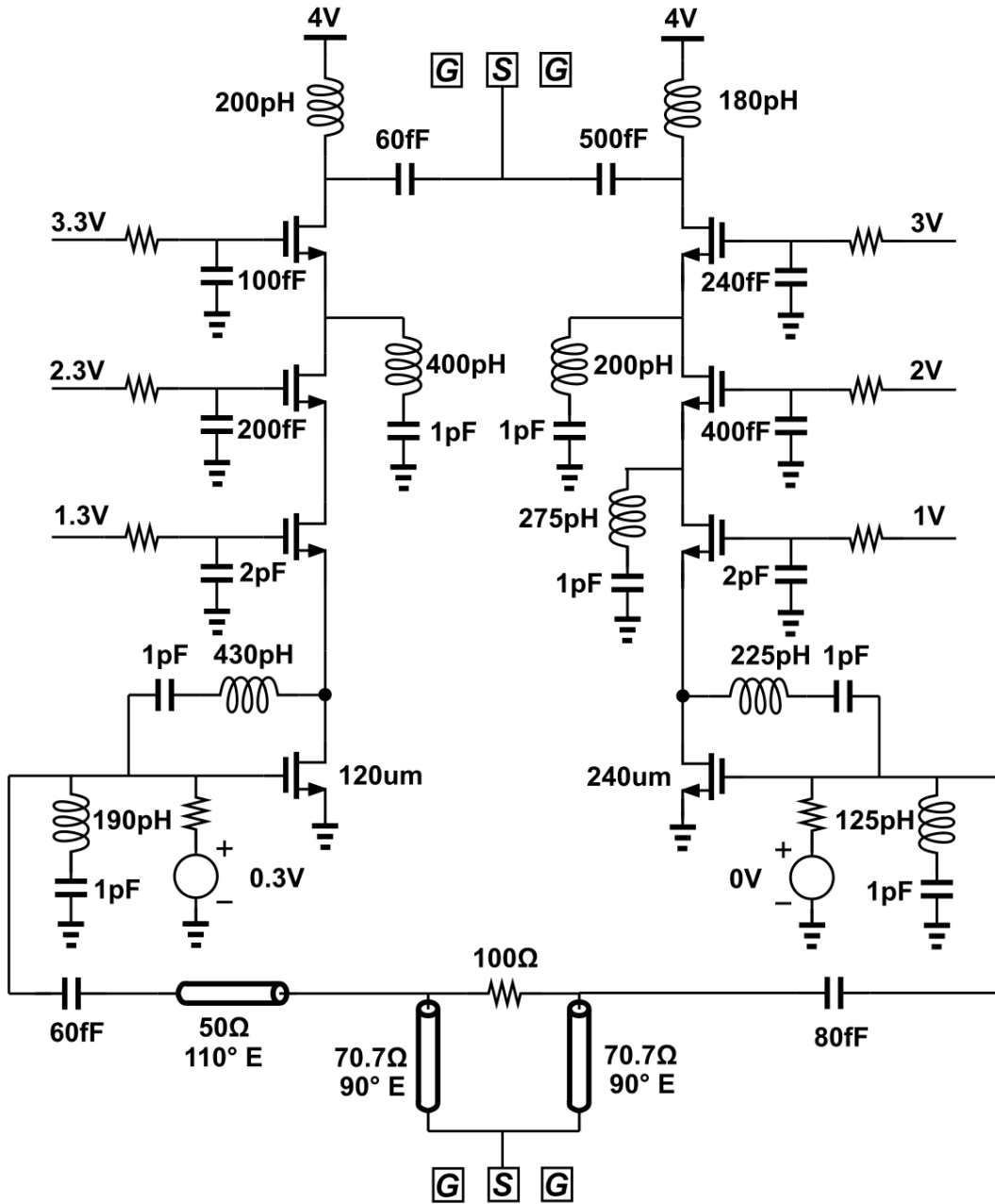


Figure 5.6: Schematic of the proposed Doherty PA

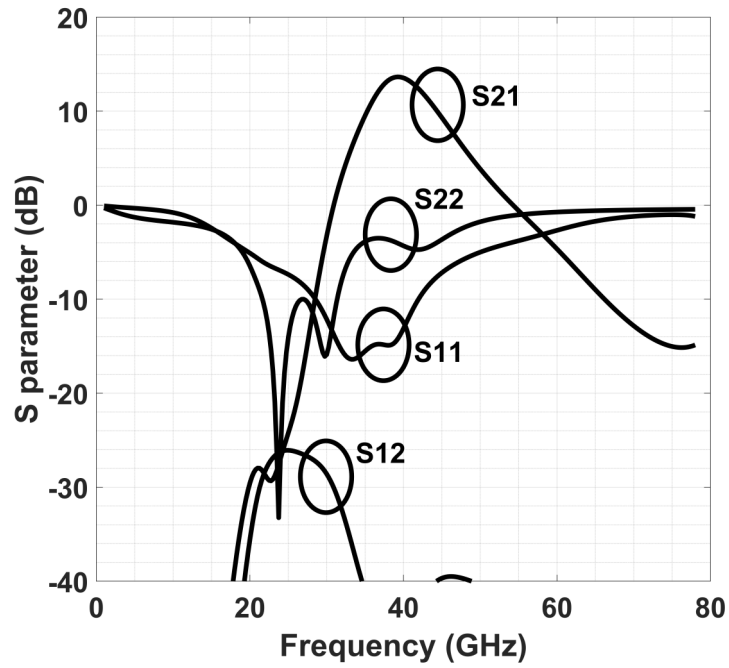


Figure 5.7: Simulated S parameter of the Doherty PA

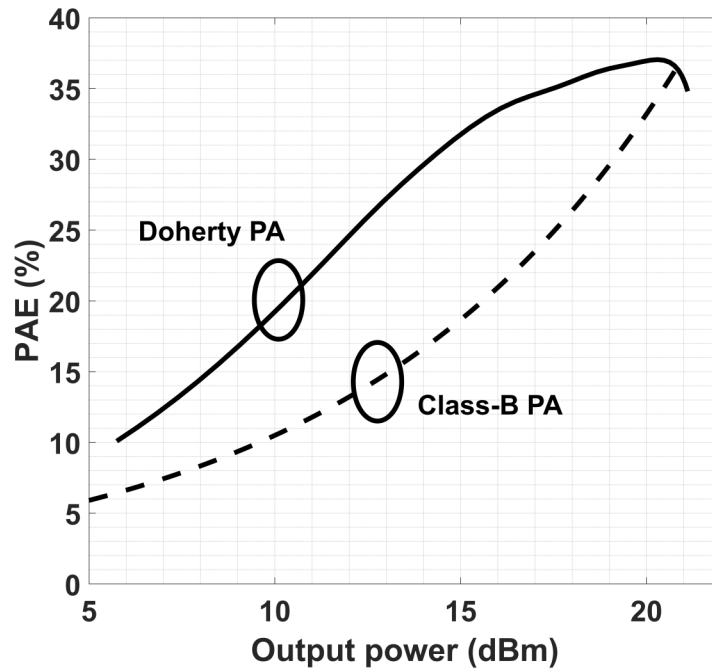


Figure 5.8: Comparison the PAE between Doherty PA and theoretical class-B PA

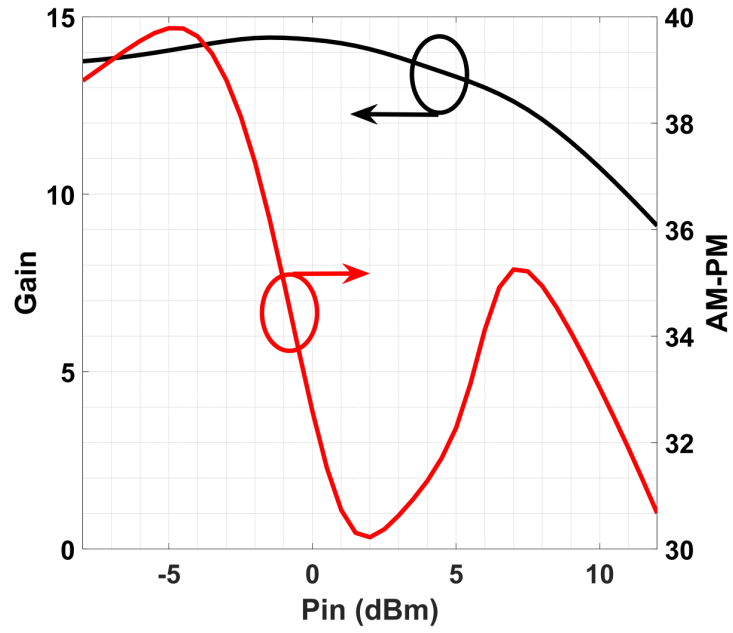


Figure 5.9: AM-AM and AM-PM for the Doherty PA

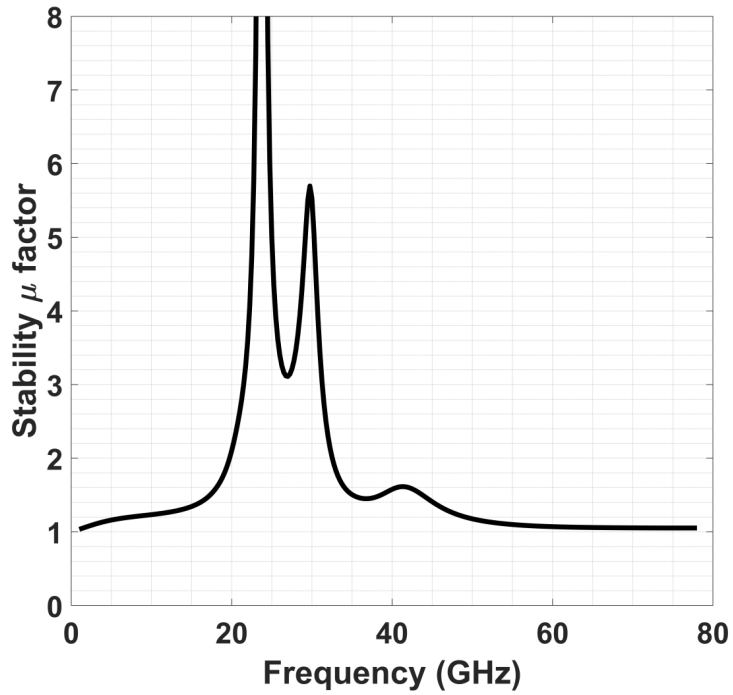


Figure 5.10: Stability μ factor of the Doherty PA

PAs are critical for the power adding. Fig. 5.8 shows the PAE simulation result comparing the theoretical class-B PA based on the assumption that the class-B PA reach the same peak output power and peak PAE. From this comparison, the PAE of Doherty PA at 6dB back-off is 32% while the PAE of class-B PA is 17%. At 10dB back off, the proposed Doherty PA provides 22% PAE while the class-B PA providing 12% PAE. Fig. 5.9 shows the gain variation with the input power (AM-AM) and the phase of the output voltage signal variation with input power (AM-PM). From this result, we could see that the P_{sat} is 21dBm and P_{1dB} is 19dBm. The phase variation is limited from 30° to 40° . Thanks to the unilateralization network, the small signal gain is 14dB. Fig. 5.10 shows the stability factor μ of the Doherty PA, the PA is unconditional stable over the all frequencies.

Chapter 6

Above 100GHz PA Design

Based on the exploring of the 5G band high efficiency PA design, some of the techniques could be expanded to the higher frequency range such as above 100GHz. Once the carrier frequency above 100GHz, the signal has abundant bandwidth for signal transferring. However, only few modern technologies support the IC operation beyond 100GHz. In this chapter, a few technology are compared to show the state of art of PA design above 100GHz. In section 6.2, a high efficiency InP PA is demonstrated with using sub quarter wavelength balun. In section 6.3, a 120GHz doherty InP PA design is illustrated.

6.1 Comparison of Modern Technology

With the improving of f_t and f_{max} in modern technology, PA above 100GHz becomes possible. The GlobalFoundary 45nm SOI CMOS provides NMOS with larger than 250 GHz f_t and larger than 300GHz f_{max} . However, working the PA at $\frac{1}{3}f_{max}$ or $\frac{1}{2}f_{max}$ requires enough gain to give room for the loss metal connection. The simplest way to improve the efficiency of PA is to design the PA working at class-B mode. But class-B biasing also decreases the gain while eventually hurts the efficiency.

Some III-V compound HBT technology could provide close to THz f_t and f_{max} . In these technologies, the MAG could be larger than 10dB at 120-140GHz band. These are very promising candidates for the high efficiency PA design above 100GHz. In the PA survey [32], several technologies are compared as shown in Fig. 6.1, Fig. 6.2, Fig. 6.3 and Fig. 6.4 for P_{out} of SiGe PA, GaN PA, GaAs PA and InP PA at different frequencies respectively. In these plots, only a few researches have been done above 100GHz. From the survey, only SiGe and InP technology have been used to successfully demonstrate the PA above 100GHz with higher than 20dBm peak output power. One take from these plot is that all the PAs above 100GHz reported from this survey have PAE less than 10%. Low efficiency could be the largest constrain on the whole system for commercial using. Due to the limitation of the technologies, the f_t and f_{max} are not beyond THz, so the MAG provided by the devices are low. To fully utilize the HBT to get gain close to MAG, very compact footprint need to be designed [33]. Also, in the circuit design, reducing the loss is the critical factor.

In the Teledyne 250nm InP HBT process, the f_t is 350GHz and the f_{max} is above 600GHz. This is potentially a good process for the applications above 100GHz. In the recent work [34], a 110-150GHz PA has been demonstrated with 24dBm P_{sat} , 20dBm P_{1dB} and less than 10% PAE. In the next session, the work targets for high PAE is demonstrated with this process.

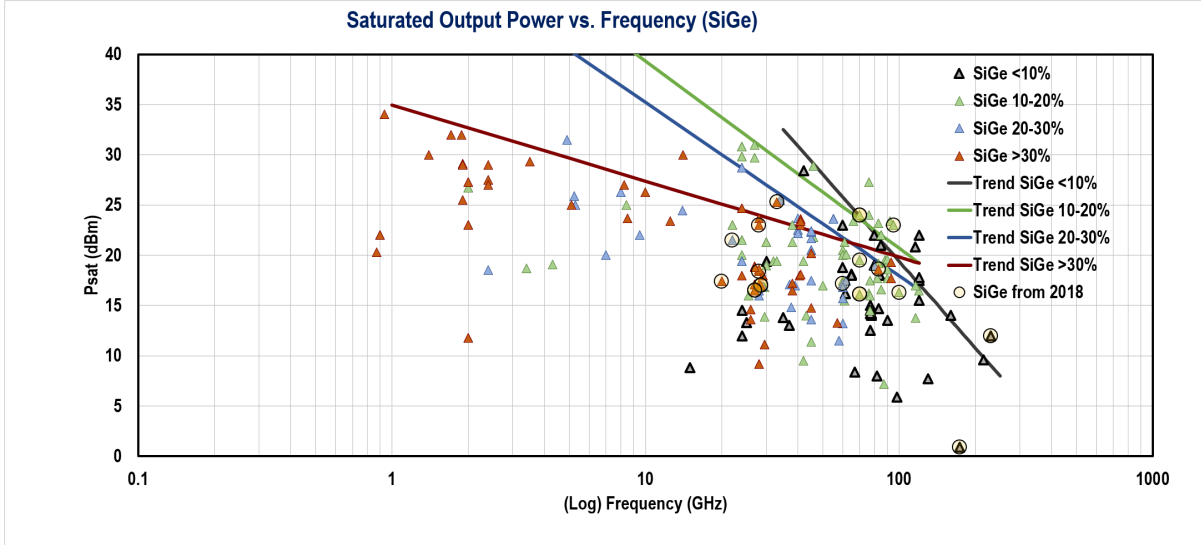


Figure 6.1: PA performance of SiGe process

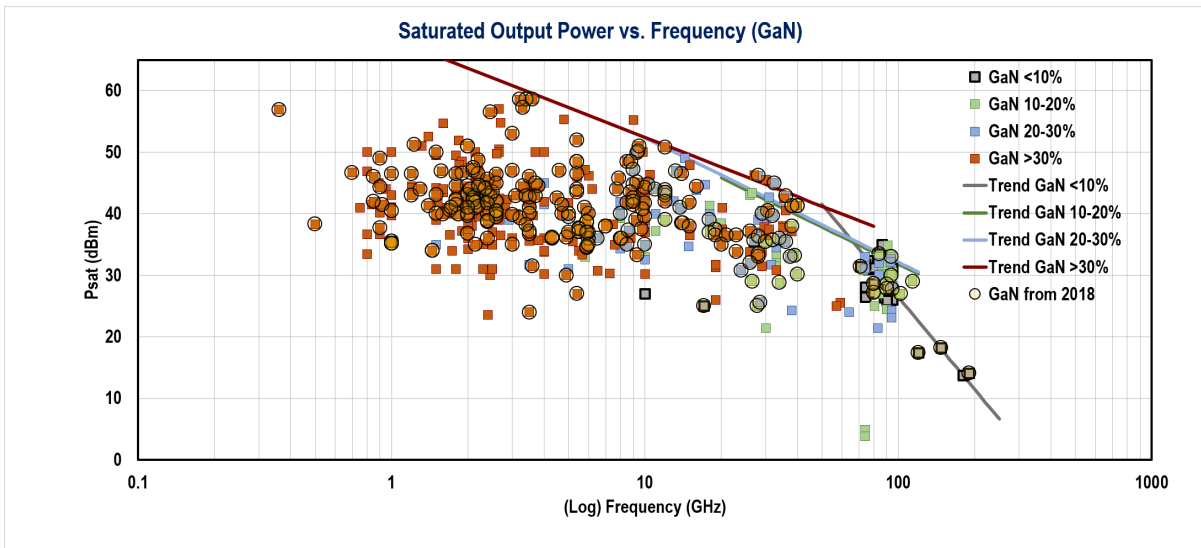


Figure 6.2: PA performance of GaN process

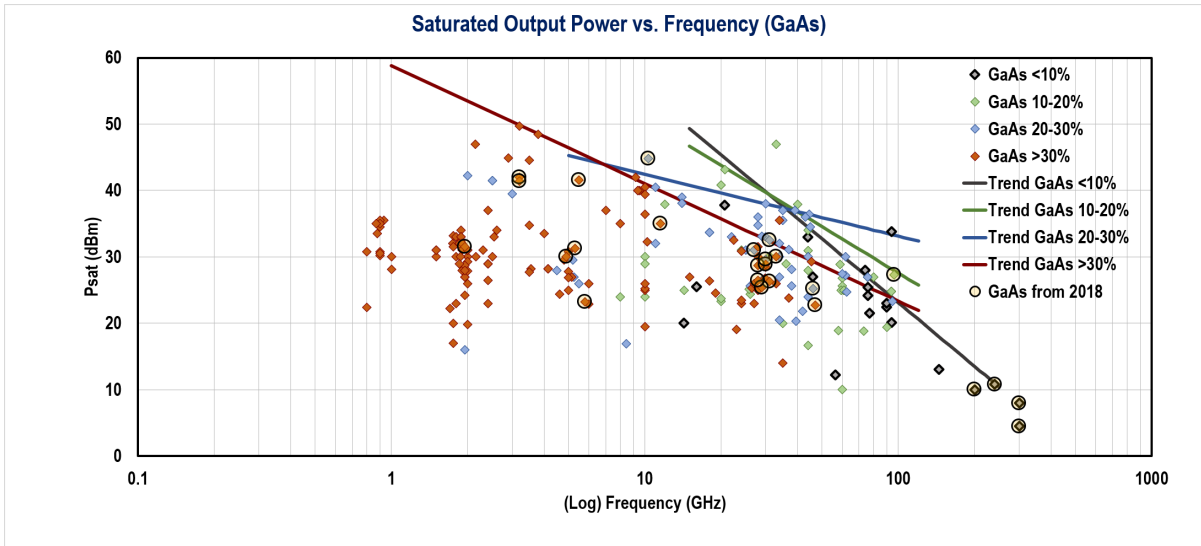


Figure 6.3: PA performance of GaAs process

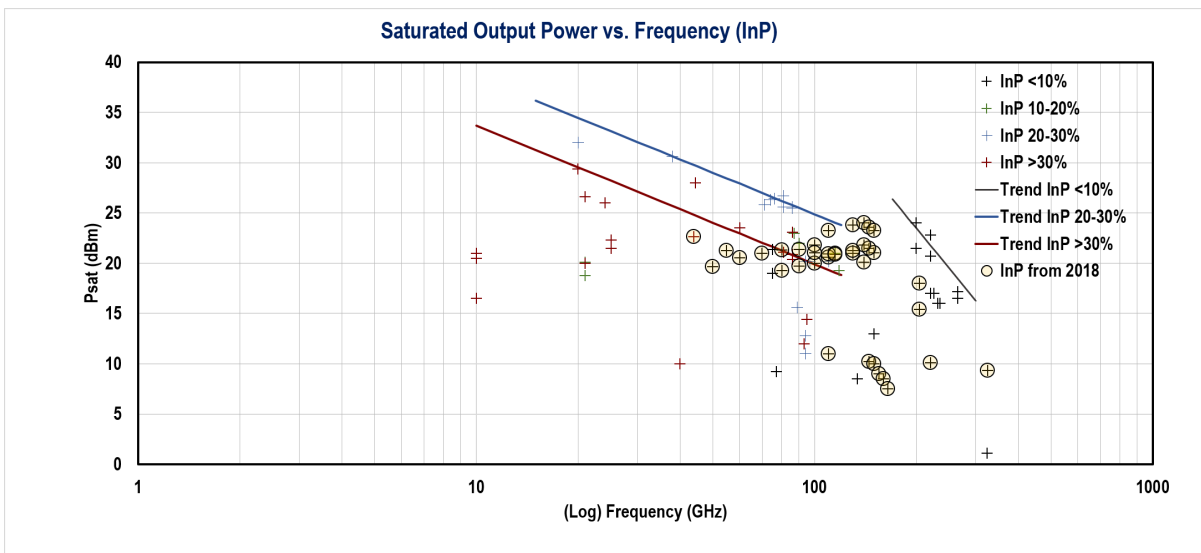


Figure 6.4: PA performance of InP process

6.2 Implementation of 120-140 GHz Common Base PA

As demonstrated in the section 6.1, most of the state of art PAs above 100GHz have PAE less than 10%. To improve the PAE, a critical factor is gain. The MAG of Teledyne 250nm InP PA is shown in the Fig. 6.5 with showing the bias condition. Here the transistors are biased at class-B point to improve the efficiency while maintain the linearity of the PA. From the Fig. 6.5, the MAG at 120GHz is 18dB in the common base (CB) topology and it's 12dB in the common emitter (CE) topology. This makes the CB topology superior than CE topology above 100GHz. Moreover, from the PDK model, the C_{CB} is much larger than C_{CE} due to the vertical device structure. This means the feedback capacitance in CE topology is much larger than the feedback capacitance in the CB topology. This is another advantage of the CB topology that smaller feedback capacitance helps to reduce the complexity of the stabilization circuitry or even could omit the stabilization circuit. It's especially an advantage in the band above 100GHz that helps to reduce passive components which bring loss in the signal path.

The common base schematic is shown in the Fig. 6.5. Base is directly connected to the ground to shorten the inductance and resistance at base. This also emit the need of bypass capacitance for the AC ground comparing to the conventional CB topology. Due to this connection, the emitter has to be biased at negative voltage. The Fig. 6.6 shows the footprint layout of $4 * 4\mu m$ HBT combination. With this footprint, the 4 HBTs are combined closely to minimize the phase shift between two HBTs.

To reduce the combining loss, the sub-quarter wavelength balun is chosen as the power combiner as proposed in [35, 36]. The topology of the sub-quarter wavelength balun is shown in Fig. 6.7. The impedance seeing into the two PAs which in figure are represented

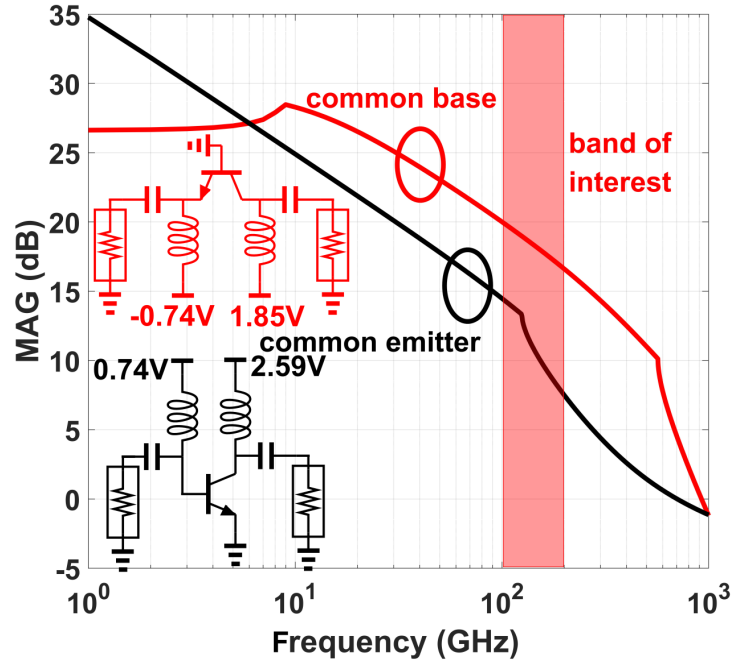


Figure 6.5: Architecture of others' work

by the pseudo differential voltage source is $\frac{Z_2}{2}(Z_1 * \cos(\theta))$. The reactive part could be tuned out with the parasitic capacitances or extra explicit shunt capacitors. Since this is a voltage combined PA, by choosing the characteristic impedance between M2 and M3 to be same as the load, the resistance seeing into two paths of the balun is $\frac{R_L}{2}$.

In the implementation, three specification need to be addressed for designing the length of sub-quarter wavelength balun:

1. Loss of the balun on each path.
2. The imbalance between two path due to the asymmetrical structure.
3. The characteristic impedance between M1 and M2 could be chosen to compensate the parasitic capacitance.

In this design, to get enough inductance $Z_1 * \cos(\theta)$, the M1 layer is slotted to increase the characteristic impedance. As shown in the Fig. 6.8 and Fig. ??, theoretically, longer balun has higher loss so the balun should be chosen small. However, the loss different in

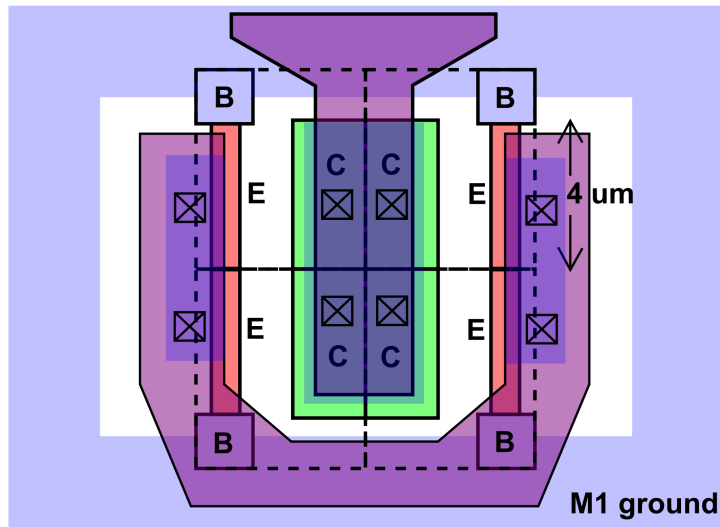


Figure 6.6: Footprint of the $4 * 4\mu m$ HBT combination

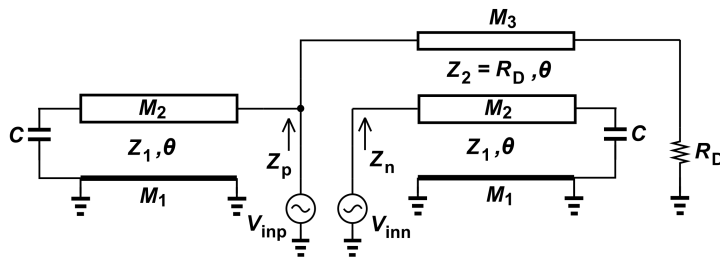


Figure 6.7: Schematic of the sub-quarter wavelength balun

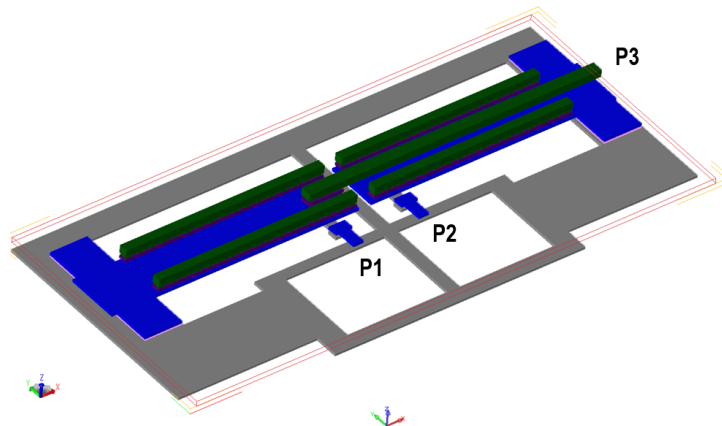


Figure 6.8: Layout of the sub-quarter wavelength balun

between two paths could be larger in the shorter balun. In other words, the shorter balun has the disadvantages:

1. Larger imbalance could attribute to the thermal runaway in between the differential pair.
2. The average loss of the balun is actually higher as shown in the comparison of $\lambda/8$ and $\lambda/12$.

Based on this trade off, the length is chosen as $\lambda/8$.

One thing worth to be noted is that in a common base topology PA, the collector current I_C is very close to the emitter current I_E , so the power gain is roughly equal to the power gain. So:

$$\begin{aligned}
 Gain &= \frac{P_{out}}{P_{in}} \\
 &= \frac{\frac{1}{2} Re\{V_{out} * I_C^*\}}{\frac{1}{2} Re\{V_{in} * I_E^*\}} \\
 &= \frac{V_{out} * I_C^*}{I_C^{*2}} \\
 &= \frac{V_{out} * I_C^*}{V_{in} * I_E^*} \\
 &= \frac{V_{out}}{I_C^*} \\
 &= \frac{V_{out}}{V_{in}} \\
 &= \frac{I_E^*}{I_C^*} \\
 &= \frac{R_{out}}{R_{in}}
 \end{aligned} \tag{6.1}$$

From this derivation, it's clear that the output impedance should be higher than the input impedance, specifically, the ratio of the output impedance and input impedance approximately equals to power gain. In other words, in CB topology, the input and output matching should be designed to match to different impedance. As shown in the Fig. 6.9,

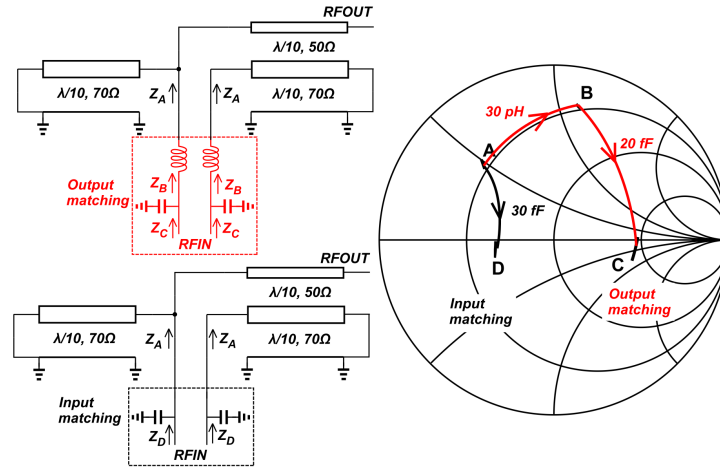


Figure 6.9: Matching network at input and output with sub-quarter wavelength balun

the impedance seeing into the balun is drawn on Smith chart point A. At the input, shunt capacitors are added to compensate the inductance from balun. So the impedance turns to 25Ω , point D. At the output, series inductors and shunt capacitors are added to turn the impedance to about 100Ω , point C. The parasitic capacitance C_{BE} and C_{BC} could be used as the shunt capacitor at the input and output respectively. However, due to the different capacitance requirement for the impedance matching, explicit capacitor could be added at the input.

The Fig. 6.10 shows a schematic of this design and Fig. 6.11 shows a micrograph of this PA. This PA is designed with Teledyne $250\mu m$ InP technology. Chip size is $0.4mm * 0.5mm$ with pads. Because the base is directly connected to the ground, $0V$. So the V_{EE} is set to $-0.74V$ and the V_{CC} is set to $1.85V$.

This chip is measured using Keysight N5247A PNA with a D-band (110-170 GHz) VDI frequency extender. Due to the output power of this frequency extender is constant to 10.7 dBm , counting on the 2.15dB loss from probe, the input power of the PA is 8.65dBm . The actual measurement is large signal S-parameter (LSSP) rather than small signal S-parameter. The measurement and the comparison result is shown in the Fig. 6.12. The

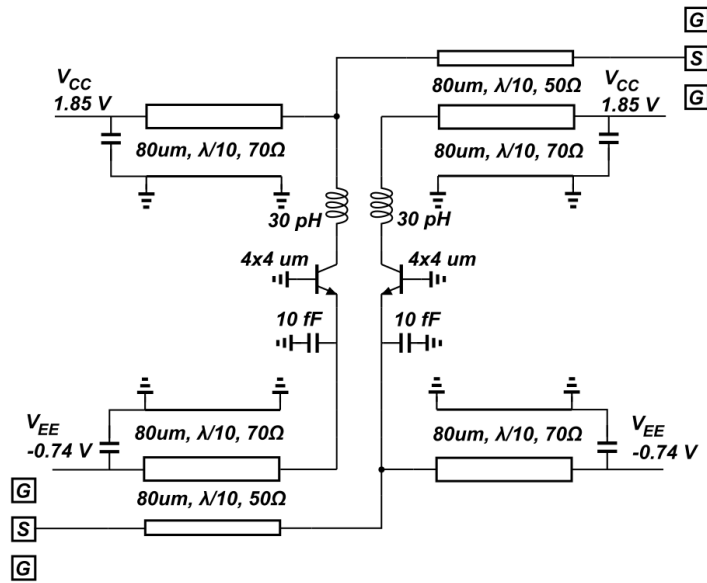


Figure 6.10: Schematic of the designed one stage InP HBT PA

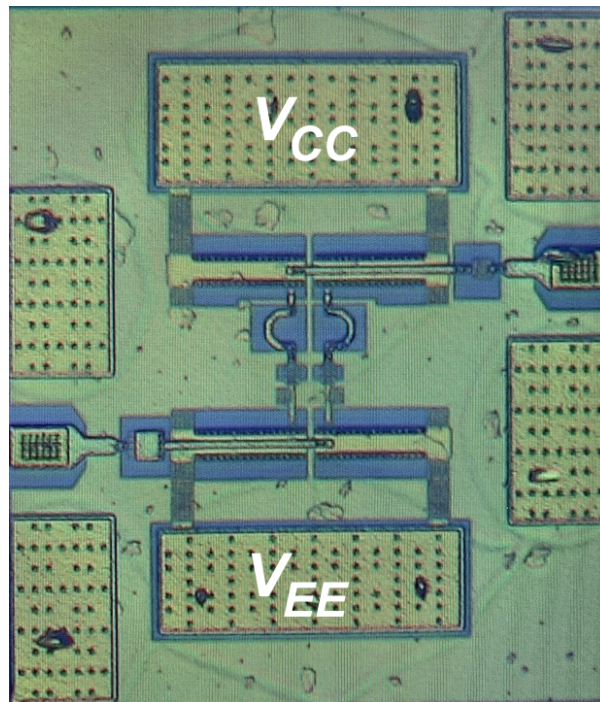


Figure 6.11: Micrograph of the InP HBT PA

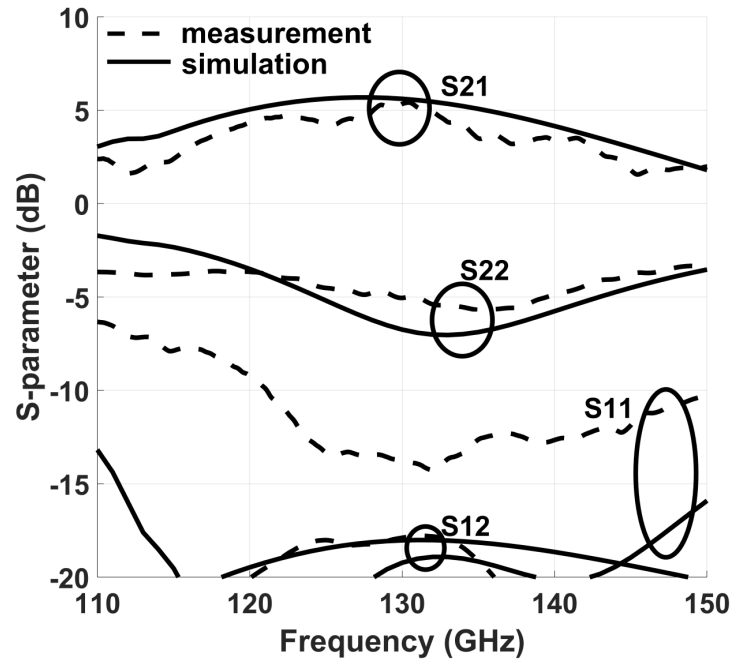


Figure 6.12: Comparison of the measured and simulated large signal S-parameter

peak gain is 7dB at 130 GHz. From the comparison, the measurement result match to the simulation result well.

In the power measurement, a D-band mechanically adjustable attenuator is added between the probe and frequency extender. By using the on wafer through transmission line, a look up table (LUT) is recorded for the power calculation. The Fig. 6.13 shows the PAE measurement result comparing to the simulation result. The peak PAE is 32% with 15.3 dBm peak P_{out} . The measured gain is 7dB at peak.

Fig. 6.14 shows the measurement result of PAE and P_{out} over the frequency band with the similar input power condition. As demonstrated before, the output power of the frequency extender is about 10.7dBm over the band and the loss of the probe varies with band in a small range as 0.5dB. So the input power of the InP PA is about 8.5dBm but varies due to the probe loss. From this measurement, the 3dB power bandwidth is from 118GHz to 148GHz. The measured PAE fits the simulation well above 130GHz, however,

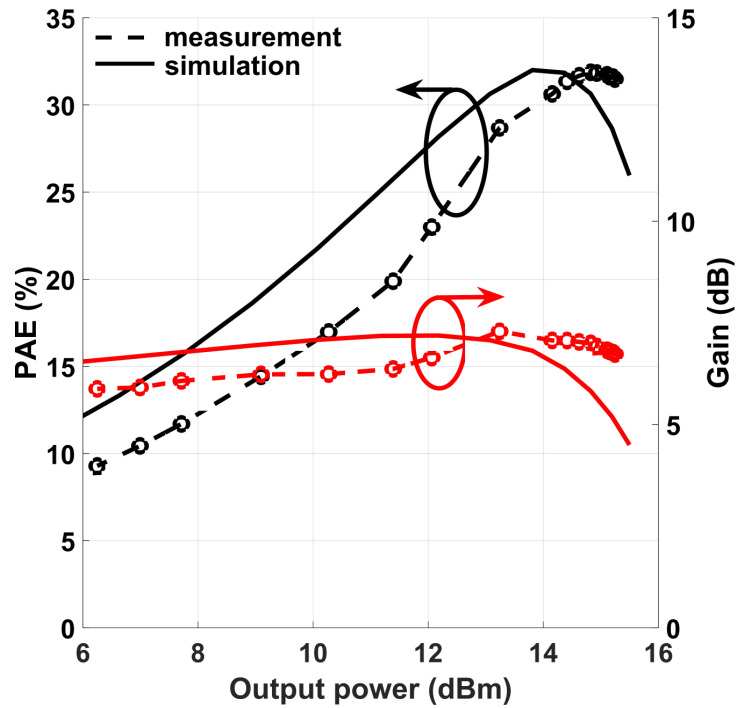


Figure 6.13: PAE and AM-AM measurement result comparing with the simulation result

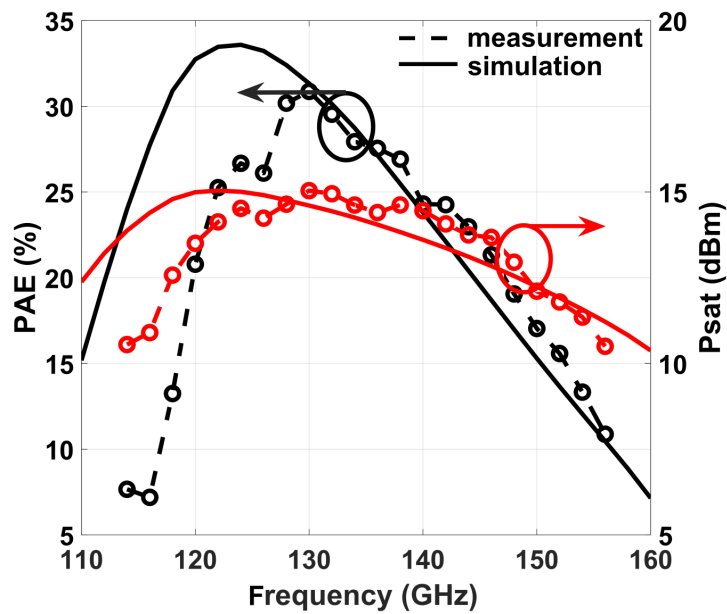


Figure 6.14: PAE and P_{out} over the frequency band

Comparison with state of art D-band PAs

Ref.	Technology	Frequency (GHz)	Gain (dB)	P_{sat} (dBm)	P_{1dB} (dBm)	PAE (%)	Chip Size (mm ²)
[34]	250nm InP HBT	110-150	14-16	24	20	8.87	1.88
[37]	130nm SiGe HBT	131-180	27	14	13.2	5.7	0.48
[38]	0.14 μ m GaN DHFET	98-122	22	27	-	7	6.98
[39]	0.1 μ m InP HEMT	65-140	6-8	14	-	2-4	1.68
[33]	90nm SiGe BiCMOS	110-140	7.7	22	-	3.6	0.62
This work	250nm InP HBT	118-148	7	15.3	14.4	32	0.2

it more likes a frequency shift from 124GHz to 130GHz. This may due to the HBT model inaccuracy.

The table shows a comparison of this PA with the state of the art. As in the comparison, this work achieves highest PAE with moderate output power and power gain. Also the chip size is the smallest comparing to others' work. The advantage of this topology is that it could be move to another frequency easily by changing the size of the balun and the matching network without consideration of stability due to the low parasitic capacitance C_{CE} .

6.3 120GHz Doherty PA Design

Based on the 120GHz differential common base InP HBT PA design demonstrated in section 6.2, we could use different size of HBTs to form a Doherty PA at 120GHz which could provide back-off efficiency improvement.

At the beginning, different size of HBTs need to be explored with the load pull simula-

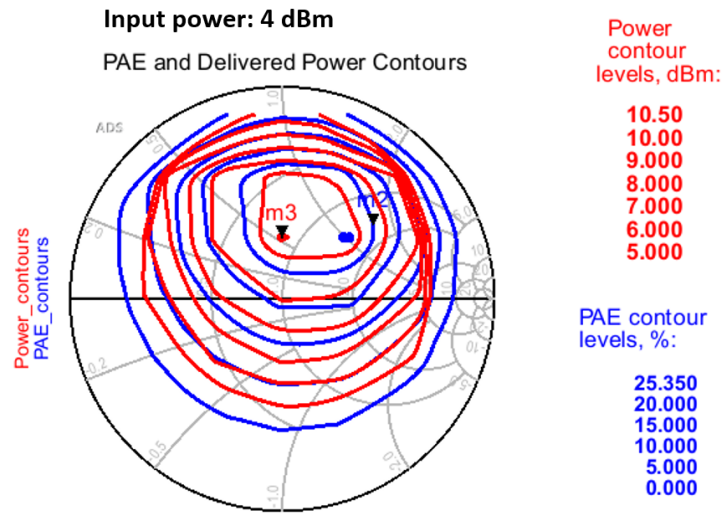


Figure 6.15: Load Pull simulation for $4 * 4\mu m$ differential CB PA with class-C bias at 4dBm input power

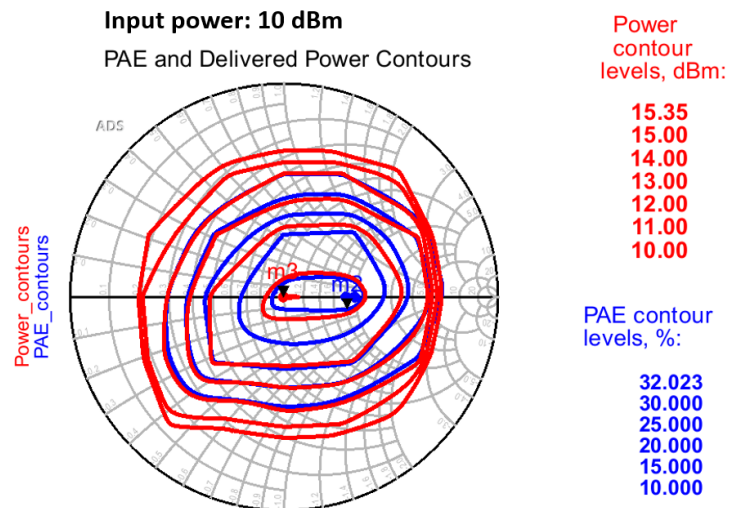


Figure 6.16: Load Pull simulation for $4 * 4\mu m$ differential CB PA with class-C bias at 10dBm input power

tion. Fig. 6.15 and Fig. 6.16 show the load pull simulation of a CB differential $4 * 4\mu m$ HBT PA cell including the balun in class-C bias condition with different input power. This means that the $V_{CC} = 1.8V$, $V_{BB} = 0V$ and $V_{EE} = -0.71V$ as class-C bias. Different power level simulation is for the understanding of expected load impedance at peak output power and the back off. To use this PA as an auxiliary PA for the Doherty PA, the power combiner at the output should:

1. Provide inductive impedance at power back off.
2. A large range of impedance fits the high efficiency, so just try to keep it in the center loop. Which could be inductive or capacitive.

Similarly, Fig. 6.17 and Fig. 6.18 shows the load pull simulation of a CB differential $2 * 4\mu m$ HBT PA cell including the balun in class-B bias condition with different input power. This means that the $V_{CC} = 1.8V$, $V_{BB} = 0V$ and $V_{EE} = -0.74V$ as class-B bias. To use this PA as a main PA for the Doherty PA, the power combiner at the output should:

1. Provide capacitive impedance at both peak and compression region
2. Keep high impedance to keep high PAE and Pout

Based on the above impedance requirement by the auxiliary PA and main PA at peak output power and at the power back off, it's clear that a series inductor could be added at the output of the main PA to keep the impedance to be inductive for the auxiliary PA at the power back off meanwhile to be resistive for the main PA. However, due to the different sizing and different bias of the two PAs, these two PA shows different AM-PM performance, that means to match the voltage and current waveform of two PAs, a phase shift needs to be added in between two PAs. From the simulation, 210° should be added in between two PAs. This could be done by adding another balun which provides 180° phase shift and other lumped component for another 30° phase shift. As shown in the Fig. 6.19 dashed circle box, different size of the impedance matching are used to achieve

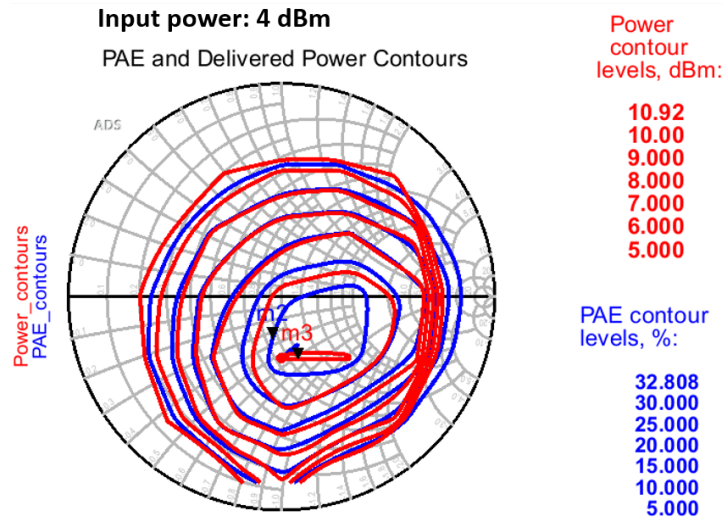


Figure 6.17: Load Pull simulation for $2 * 4\mu\text{m}$ differential CB PA with class-B bias at 4dBm input power

additional phase shift. In consideration of the loss balance problem, the PA cells are changed to have a crossed connection as shown in the Fig. 6.20. In this way, the imbalance between the two paths of the balun reversely occurring at both input and output. So the loss in two paths are equal. This should help with reducing the possibility of thermal runaway issue.

Fig. 6.21 shows the simulated S parameter for the proposed InP Doherty PA. The input and output are matched well at 120GHz. Fig. 6.22 shows the simulated stability μ factor. From the simulation, this design is unconditional stable. Fig. 6.23 shows the simulated PAE versus the output power. From this result, the peak PAE is 27% with above 16dBm output power. At 6dB power back off, the PAE is still above 20%. Fig. 6.24 shows the simulated gain and AM-PM over the input power. The phase varies from 77° to 50° while the gain varies from 5.7dB to 3dB.

The gain variation mainly due to the low gain for the main PA at class-C bias. This is the main difficulty in the design. If the auxiliary PA set to close to the class-B bias, the average DC current on the auxiliary PA would be too high at the power back off region

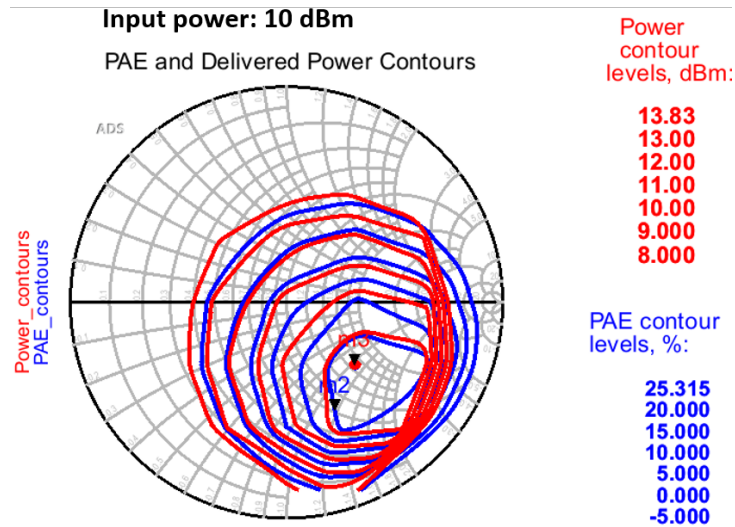


Figure 6.18: Load Pull simulation for $2 * 4\mu\text{m}$ differential CB PA with class-B bias at 10dBm input power

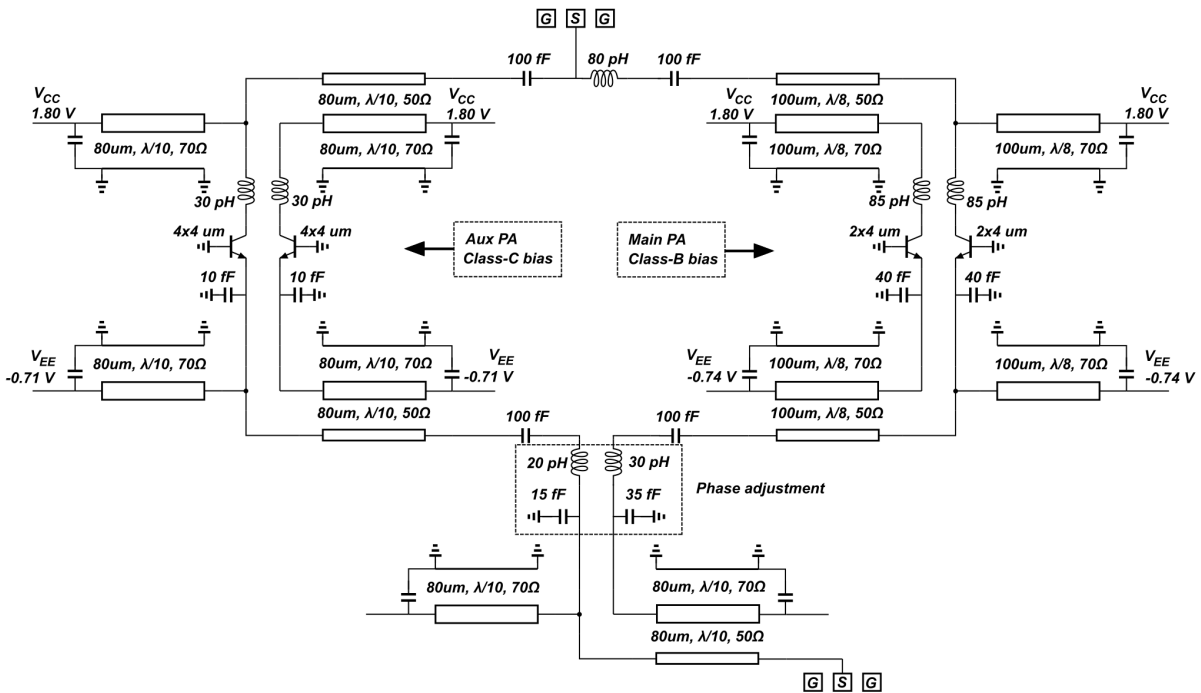


Figure 6.19: Schematic of the 120GHz Doherty PA

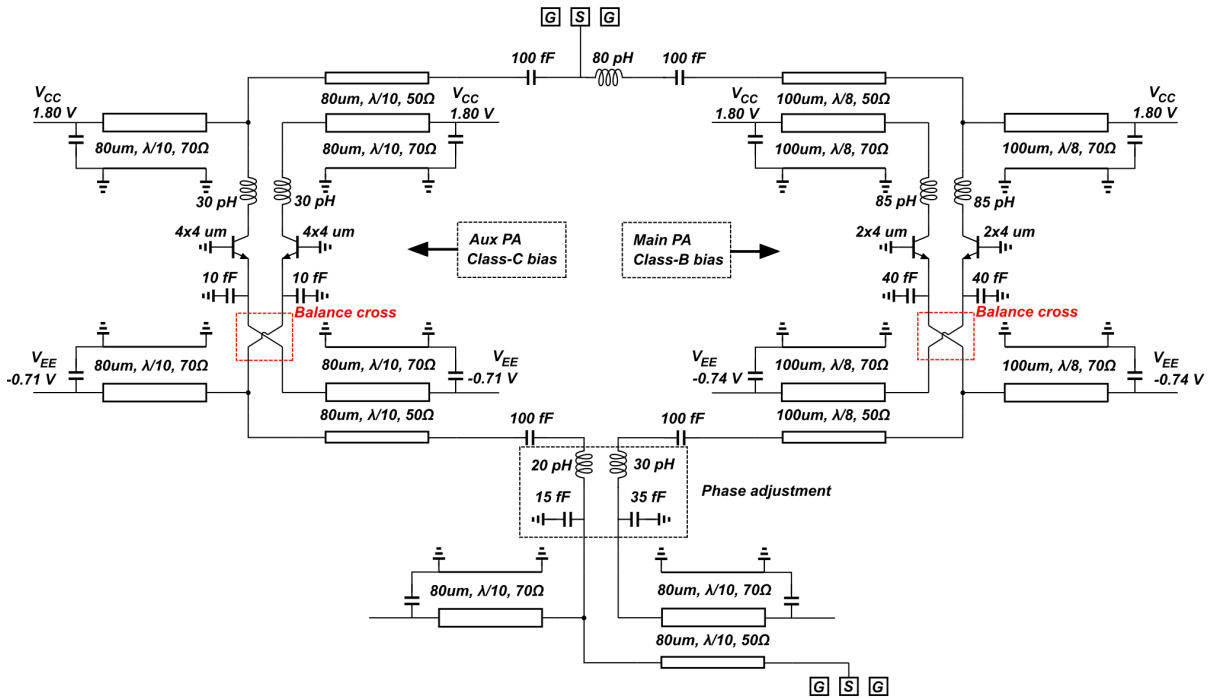


Figure 6.20: Schematic of the 120GHz Doherty PA with cross connection in PA cells

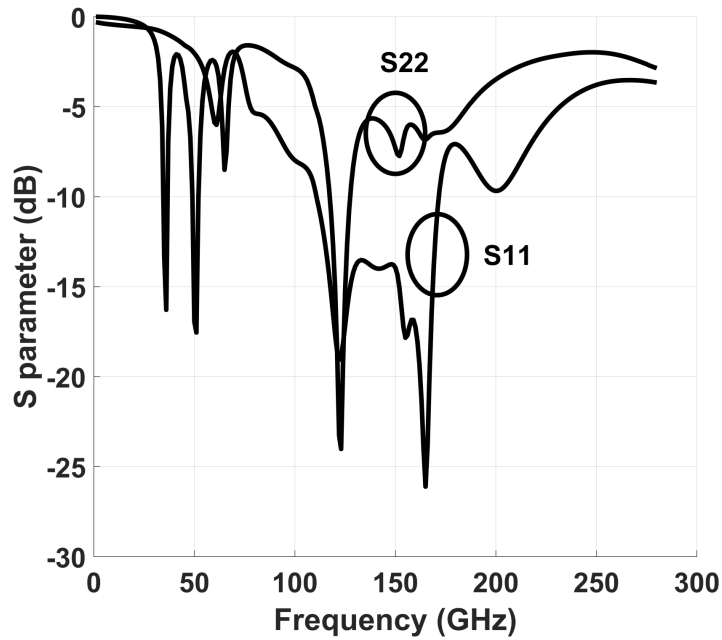


Figure 6.21: Simulated s parameter for the Doherty PA

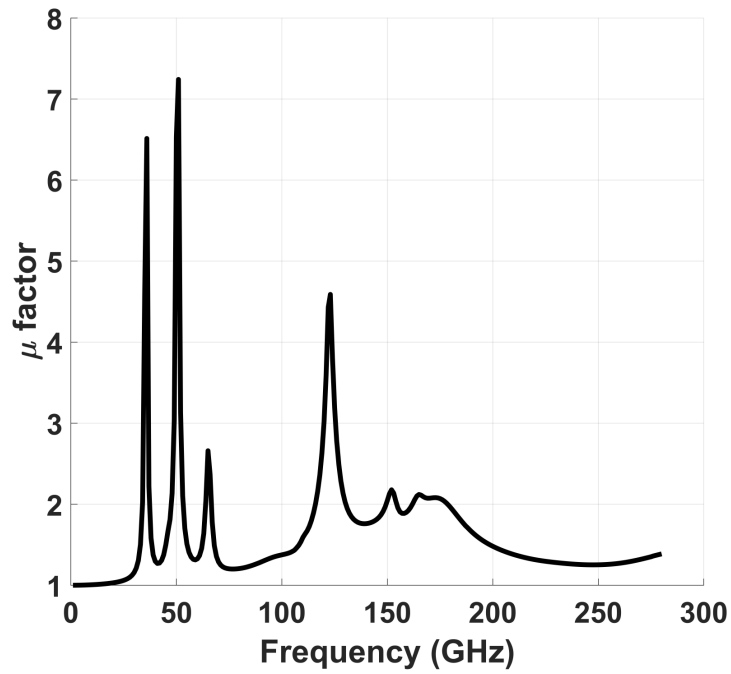
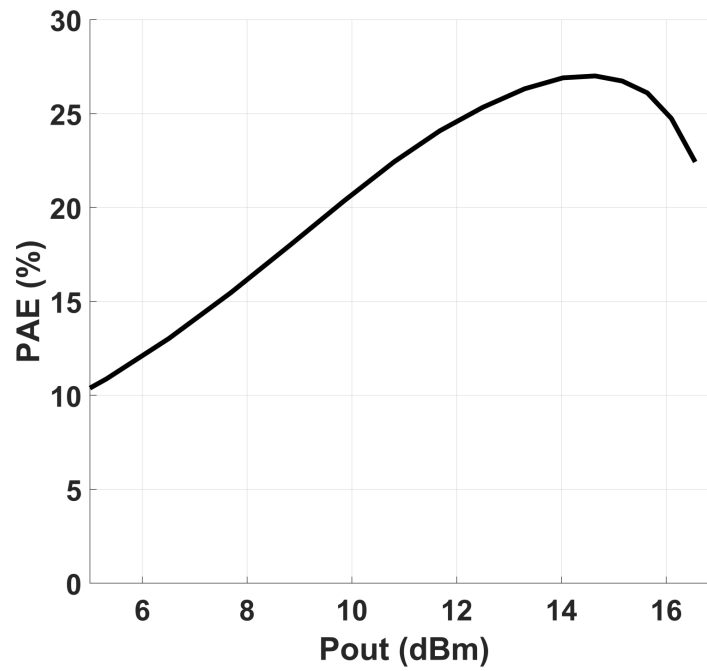
Figure 6.22: Stability μ factor of the Doherty PA

Figure 6.23: PAE of the Doherty PA

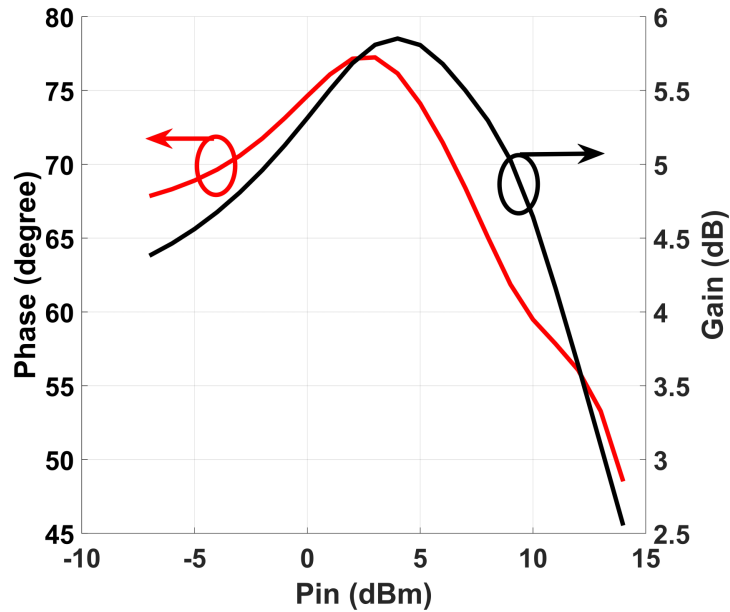


Figure 6.24: Simulated gain and AM-PM performance

that hurts the back off efficiency. However, the gain also drops once bias it to class-C region.

The phase variation mainly due to the AM-PM difference for two PAs. Especially the input matching network specifically choosing phase difference for the power matching at the peak output power, then the phase difference could be larger at the power back off region. So the total AM-PM is not fully under control.

As a conclusion in the above design, the 250nm InP process is used for the 120-140GHz PA design to achieve high PAE in class-B common base topology PA and high average efficiency in Doherty PA design. This work shows the potential of the InP HBT process for the high efficiency PA design for the next generation mobile communication system.

Chapter 7

Design Conclusion and Future Work

As demonstrated in chapter 1, the expectation on the frequency bandwidth pushes the carrier frequency to mm-wave band and requires for high efficiency PA design. With using the complex modulation techniques such as QAM signals to further extend the data transformation speed, the high average efficiency PA are expected. This work focused on the peak PAE improvement techniques in power amplifier design as a start to achieve high PAE in the linear PA. As a result, I designed the inductive-coupled efficiency improvement class-B PA which achieves 48% peak efficiency at 30GHz with 45nm SOI CMOS technology. The novel inductive-coupled method not only help to neutralize the C_{gd} and improve the efficiency, but also achieve the high output power while re-use the matching network inductors in the conventional stack-FET. At higher frequency band, a 32% PAE common base power amplifier at 130GHz has been designed with achieving the record power density.

For the average efficiency improvement PA design, the outphasing PA and Doherty PA are two most optimizing architecture. In the chapter 4, I described a design methodology for the outphasing PA by analyzing the PAE and power contours in load pull simulation. For the outphasing PA architecture, the constant envelope output power are combined with

the combiner. The PA cells are pushed into compression region for the highest possible output power and the PAE. Therefore, the output power and the DC power consumption changes with the impedance seeing into the combiner. The impedance varies with the outphasing angle. So the load modulation helps to achieve different output power level and change the DC power consumption while the input power does not change. In other words, the load pull output power and PAE contour on Smith chart is a power tool for the outphasing PA design since the contours shows output power and PAE under the all possible impedance conditions. By load pull simulation, the outphasing PA performance could be predicted without design a power combiner. In chapter 4, I demonstrated the importance of neutralization and unilateralization circuit for the PA cells and how it impact the PA performance. As a conclusion, the outphasing PA wants to have a PA cell which has separated power contours and PAE contours. The relation behind the linearity, power contour and PAE contour is an untouched area for understanding deep insight of the relationship between device characteristic and outphasing PA performance. However, outphasing PA architecture naturally has disadvantage on PAE. Due to the constant input power of the PA, gain drops with the power back off lineally. This means in the mm-wave band, the outphasing PA may give high drain efficiency, but at the power back off, the PAE could drops to 0% due to low gain.

Doherty PA is another candidate for the mm-wave high average efficiency PA design. In Chapter 6, I demonstrated the novel combiner-less Doherty PA design. The advantage of this Doherty PA is removing the output power combiner which normally lossy and occupies large area. In the further work, the controlling on the linearity of the Doherty PA need to be addressed.

The novel topologies are expected for the average efficiency improvement. Some architecture has been proved promising for improving average efficiency such as [40] yet still need to be proven for the efficiency improvement for the total transmitter.

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