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High-Gain Gated Lateral Power Bipolar Junction Transistor

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***Abstract*— We demonstrated a prototype Gated Lateral power bipolar junction transistor (GLP-BJT) on wide bandgap semiconductor. The device combined the intrinsic advantages of high current gain of a Gated Lateral-BJT and good current handling and voltage blocking capabilities of GaN material. As a result, the common-emitter current gain remained over 300 at a high collector current density of 2 kA/cm^2 despite a wide *p*-base region of 2μm. The open base breakdown voltage BV_{CEO} was over 300 V corresponding to a high critical field of 2.5 MV/cm. These figures of merit show great promise of GaN-based GLP-BJT in power applications and also shed light on the development of state-of-the-art bipolar transistors based on other wide bandgap semiconductors.**

***Index Terms*— Bipolar transistors, gain, gallium nitride, MOSFET, power semiconductor devices, silicon carbide.**

I. Introduction

POWER bipolar transistors based on wide bandgap semiconductors such as GaN and SiC are attractive candidates for high power applications [1], [2]. The high critical field and high electron saturation velocity lead to their distinctive advantages such as high current and power handling capability. For power bipolar transistors, high current gain is one of the most desirable figures of merit especially under high current condition [3]–[7]. For switching application, a high current gain (>200 [8]) can significantly reduce drive current I_B, which is important for low on-state power dissipation and high-efficiency base drive circuit [9]–[11]. However, both 4H-SiC-based bipolar junction transistor (BJT) and GaN-based heterojunction bipolar transistor (HBT) suffer from a low current gain especially at high collector current levels [5], [12]. To make matters worse, conventional approaches to increase the current gain such as reducing the width and doping level of base region seriously compromise the voltage blocking capability, which accounts for the tradeoff between these two critical metrics of a power bipolar transistor [13], [14].

On the other hand, Gated Lateral BJT has been theoretically and experimentally studied in Si to exhibit high current gain of up to several thousand at low current levels due to the potential barrier modulation by the MOS gate structure over the base region of the lateral BJT [15]–[21]. However, the device was not configured for high power operation. It is thus expected that such a device with modified structure on wide bandgap semiconductor could combine the advantages of high current gain with good current handling and voltage blocking capabilities and hence make possible a Gated Lateral power (GLP) BJT.

In this letter, we demonstrated a high-current gain GLP-BJT on GaN. The device was characterized with the fully lateral *n-p-n* structure which could further increase current gain at high current levels. The current gain reached a peak value of 1200 at low current level and remained over 300 at a high collector current density of 2 kA/cm^2, making it among the highest current gain achieved in power bipolar transistors. The open base breakdown voltage was as high as 300 V. The device structure, fabrication and characterization will be described in detail in the following sections.

II. Device Structure

The schematic illustrations of the GLP-BJT on GaN island are shown in Fig. 1 (a). The island consists of fully lateral GaN *n-p-n* homojunctions, as seen in the Section A-A, and the *p*-base region is sandwiched between the n^--collector drift region to the left and the n^+-emitter region to the right. The device structure is essentially like a power MOSFET in which the gate and *p*-base region are internally tied. The base region underneath gate oxide is fully depleted changing otherwise quasi-neutral base region (*qnr*-base) into space charge base region (*scr*-base), as depicted in the upper right band diagram in Fig. 1 (b). The potential barriers seen by electrons (ψ_{Be^-}) and holes (ψ_{Bh^+}) between the emitter and *qnr* base under forward bias are dictated by Eqn. (1) and Eqn. (2), respectively:

$$\psi_{Be^-} = \varphi_{bi} - V_{be}; \quad (1)$$

$$\psi_{Bh^+} = \varphi_{bi} - \frac{\Delta E_g}{q} - V_{be} \quad (2)$$

where φ_{bi} and V_{be} are built-in potential and applied forward bias across the emitter-base junction, respectively. ΔE_g is the bandgap narrowing between *p*-base and n^+-emitter regions. It is also known that V_{be} serves as the underlying driving force for the high current density in a BJT [14]. As depicted in the upper left band diagram in Fig. 1(b), the barrier for

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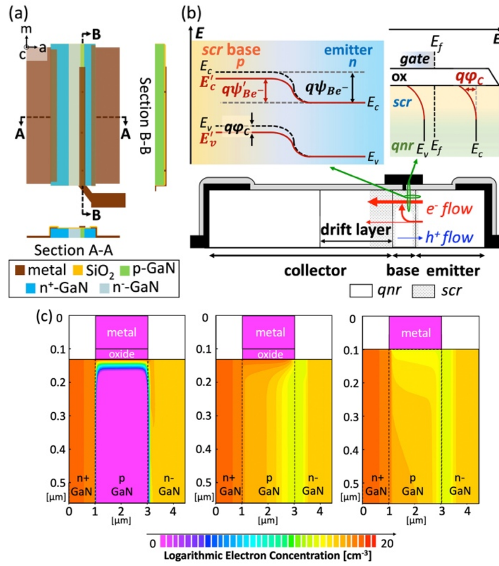

Fig. 1. (a) Schematic illustrations of device structure (the color of SiO_2 gate oxide is semi-transparent in the top-view illustration to make underlying materials discernable). (b) The band diagrams across the *scr* base-emitter junction and the MOS structure in the forward active mode of the device. The electron and hole current components are marked by red and blue arrows, respectively. (c) Distribution of electron concentration in *n*-channel MOSFET (inversion mode), *npn* GLP-BJT (forward active mode) and conventional *npn* lateral BJT (forward active mode) by SILVACO TCAD, respectively.

electrons (ψ'_{Be^-}) injected from the emitter into *scr* base is reduced by a potential of φ_c due to the gate-modulated band bending, as shown in Eqn. (3) [15]:

$$\psi'_{Be^-} = \varphi_{bi} - V_{be} - \varphi_c \tag{3}$$

As a result, electrons are injected from emitter to *scr* base more easily due to the reduced barrier, whereas few holes are injected from *scr* base into emitter. The modulation of potential barriers for electrons and holes to cross the emitter-*scr* base junction fundamentally increases the current gain in a GLP-BJT. It is worth mentioning that compared to a Si Gated Lateral BJT [15], the fully-lateral *n*-*p*-*n* structure depicted in Fig. 1(b) greatly enlarges the injection area of electrons and eliminates the parasitic vertical BJT, leading to a further increased current gain. Finally, the difference of electron concentration distribution among MOSFET, GLP-BJT and conventional lateral BJT is illustrated by TCAD simulation as shown in Fig. 1(c). Unlike conventional BJT, the *scr* base underneath the oxide provides preferential pathway for electron injection which leads to different electron distribution in *p*-base region of the GL-BJT. Compared with the unipolar MOSFET, minority carrier injection occurs throughout the entire emitter-base junction thus giving rise to more uniform electron distribution and good current handling capability. In addition, due to the vertical electric field in the *scr* base, a significant portion of the electrons injected into *qnr base* are attracted into the *scr* base devoid of holes as is indicated by the red curved arrow in Fig. 1 (b), thereby reducing the recombination current and further increasing the current gain of the device. As a result, the simulation result showed that the current gain can increase from less than 5 in the conventional lateral BJT in Fig. 1 (c) to a few hundred (>200) in the GL-BJT by virtue of *scr*-base induced by the MOS gate on top of *p*-base region.

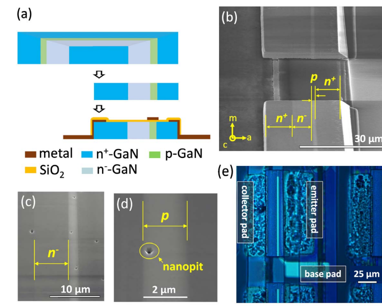

Fig. 2. (a) Cross-sectional schematics of the key steps of growth and process for the GLP-BJT fabricated on the GaN island. (b) Angled-view scanning electron microscopic image of the GaN islands consisting of the lateral n^+-n^--p -n^+ homojunctions which was taken before metallization and oxide deposition process. (c)(d) Magnified-views of (b) which reveal the width of n^--collector drift region and *p*-base region as well as hexagonal nanopit on the surface of *p*-base region. (e) Bright-field optical microscopic image of the as-processed devices (mercury lamp was used as illumination source).

III. Device Fabrication

The schematic illustrations of the key growth and process steps are shown in Fig. 2 (a) which were similar to our previous work on GaN diodes [22]. GaN stripes were grown by metalorganic vapor phase epitaxy on a LPCVD-SiN_x mask-patterned sapphire substrate through a combination of the epitaxial lateral overgrowth with *in-situ* doping, resulting in the $n^+/n^-/p/n^+$ core-shell doping structure. Then, a double-step Cl_2-based ICP-RIE (ICP power 150 W, RF power 30 W) was utilized with Ni mask to tailor GaN stripes into arrays of islands characterized by the non-polar *a*-plane lateral *n*-*p*-*n* homojunctions (Fig. 2(b)). Here n^+-GaN has [Si] $>$ 1×10^{19} cm^{-3}, n^--GaN has $|N_d - N_a| = 6 \times 16$ cm^{-3} and *p*-GaN has [Mg] $= 3-5\times 10^{18}$ cm^{-3} which contributes to a calculated hole concentration of 0.7–1.6 $\times 10^{17}$ cm^{-3} (assuming compensated $N_d = 6 \times 16$ cm^{-3} and acceptor ionization energy $\Delta E_{A,0} = 220$–245 mV) [23], [24]. The resistivity of *p*-GaN was measured to be 3.5 Ω.cm by the transfer length method. As can be distinguished in the magnified views due to the secondary electron dopant contrast in the SEM [25], [26], the collector drift region has a width of 6–7 μm and is sandwiched between the slightly darker n^+-collector on the left (Fig. 2 (c)) and brighter *p*-base of $\sim$2 μm width on the right (Fig. 2 (d)).

The inverted hexagonal pyramidal pits with $\{10\bar{1}1\}$ facets and 200–400 nm diameter were introduced by ICP-RIE process on the etched top surface of GaN islands (Fig. 2(d)). The appearance and diameter of nanopits were modulated by the ICP and RF power of the etching process. SiO_2 of $\sim$40 nm was sputtered as gate oxide (with non-rotating substrate holder) leading to incomplete oxide coverage inside the nanopits. After that, Si ($\sim$5 nm) was sputtered followed by thermal annealing (750 °C, 1 hour) to render the diffusion of Si atoms as n-type dopant into the surface atomic layers of *p*-GaN nanopits for an N-P tunnel junction (TJ). After TMAH solution treatment to remove residual Si, photolithography and BOE were used to create openings in the passivation layer followed by sputtering of Ti (20 nm)/Al (150 nm) as collector and emitter contacts/pads and annealing (800 °C, 30 s). Then, after photolithography again, Al (180 nm) was sputtered as metal gate and pad followed by annealing (400 °C, 1 hour).

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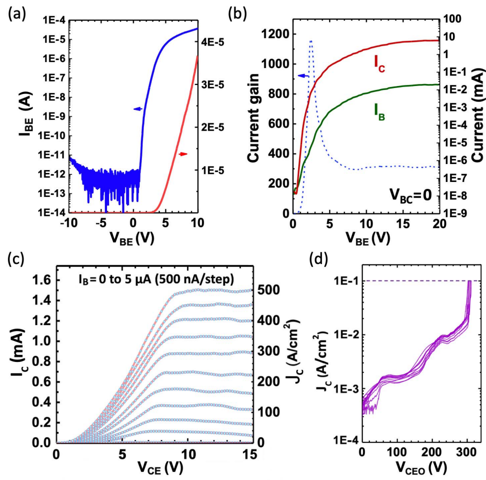

Fig. 3. (a) Open collector *I-V* characteristics showing *p-n* junction between base and emitter. (b) Gummel plot. (c) Common-emitter output characteristics. (d) Open base blocking *I-V* characteristics.

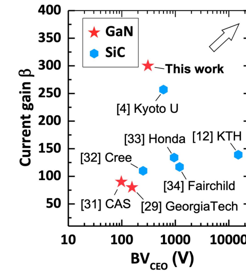

Fig. 4. Benchmark of common-emitter current gain β *vs* open base breakdown voltage BV_{CEO} of the GaN-based HBTs and 4H-SiC-based BJTs reported in the literature which satisfied the levels of $\beta > 80$ and $BV_{CEO} > 50$ V. The arrow indicates the desired corner.

The metal gate also formed Ohmic contact to *p*-base via the TJ at the nanopits. (Fig. 2(e)). In principle, other than Si diffusion-enabled TJ, the Ohmic contact can be alternatively enhanced by the similar diffusion process of deposited Mg into *p*-GaN with conventional Ni/Au metal contact for future work [27], [28]. Moreover, electron beam lithography can be utilized to make orderly nanoholes in the gate oxide instead of randomly-distributed nanopits in the *p*-base region in order to improve the device yield.

IV. Electrical Characterization

The electrical measurements were carried out in the common emitter configuration by an Agilent B1505A semiconductor analyzer. The entire cross-sectional area of the device (i.e., the section B-B in Fig. 1 (a)) was taken into calculation for current density, which has typical dimensions of 100 μm (width) $\times$ 3 μm (height).

Fig. 3 (a) is the open collector *I-V* characteristic showing that a good rectifying GaN *p-n* junction was demonstrated between base and emitter regions, which also implied the Ohmic contact was formed between metal gate and *p*-base region. The Gummel plot is shown in Fig. 3 (b). I_C was greater than I_B even at low-voltage level, suggesting that the recombination current was suppressed [29]. The current gain β (= I_C/I_B) peaked at 1200 and remained a plateau of around 300 until $I_C = 6$ mA corresponding to a collector current density J_C of 2 kA/cm^2. Given that the *p*-base region is $\sim$2 μm wide, a higher current gain is readily accessible should the *p*-base region be narrowed into sub-micrometer scale.

The common-emitter output *I-V* characteristics of the GaN GLP-BJT is shown in Fig. 3 (c). The input I_B was varied from 0 to 5 μA at a step of 0.5 μA and the output I_C ranged from 0 to 1.5 mA exhibiting a current gain of $\sim$300, which is among the highest values of current gain achieved in power bipolar transistors (see Fig. 4). Furthermore, the Early effect was not pronounced which embodied an inherent advantage of wide base region [13], [14]. The open base *I-V* characteristics were measured on the same device for a number of times, as seen in Fig. 3 (d), the open base breakdown occurred at 300–310 V at 0.1 A/cm^2 (corresponding to a critical electric field of 2.5 MV/cm). In principle, the BV_{CEO} is expected to reach 900 V should the doping concentration of n^--collector drift region be reduced below 2×16 cm^{-3} [30].

To highlight the potential of achieving otherwise tradeoff metrics of high current gain and breakdown voltage, this work is benchmarked in Fig. 4 with the state-of-the-art GaN-based HBTs and 4H-SiC-based BJTs which satisfied $BV_{CEO} > 50$V and $\beta > 80$ [4], [12], [29], [31]–[34]. The current gain at high current and power density levels ($\beta = 300$), instead of that at low-current level ($\beta > 1000$), is chosen for this work. It can be seen that compared to a few existing works in the literature that meet the above-described levels, the GLP-BJT stands out as a competitive candidate to combine the merits of high current gain and high breakdown voltage.

V. Conclusion

In summary, we demonstrated a prototype high-gain *n-p-n* GLP-BJT on wide bandgap semiconductor. Reduced potential barrier seen by electrons were injected from n^+-emitter into the depleted *p*-base region underneath the gate devoid of holes, leading to high current gain in a Gated Lateral BJT. Meanwhile, it exhibited much higher current and power handling capability than Si-based Gated Lateral BJT due to the intrinsic advantages of GaN. As a result, the fabricated GaN GLP-BJT featured a high current gain of 300 and a base region capable of withstanding high blocking voltage ($BV_{CEO} > 300$ V) and high critical electric field. These figures of merit thus show strong promise of GLP-BJT in power applications. In this sense, although the high-gain GLP-BJT was demonstrated on GaN in this work, it also provides new insights to the development of state-of-the-art bipolar transistors based on other wide bandgap semiconductors such as SiC thanks to the good generalizability of this device. Once the bottleneck of achieving high current gain in the wide bandgap semiconductor BJT can be overcome, the true benefits of the bipolar transistors, such as the potential to achieve conductivity modulation, are expected to be fully realized.

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