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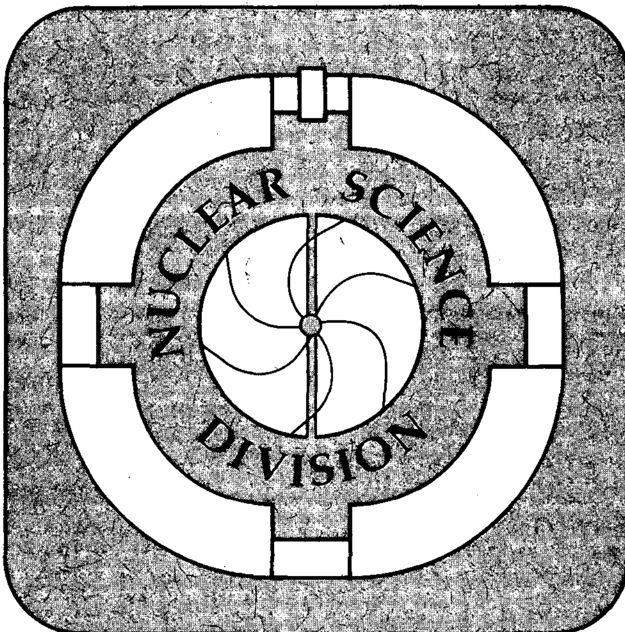
June 1995



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Abstract

We have fabricated a 4 cm x 4 cm, position-sensitive silicon drift detector using high purity, p-type silicon as the substrate. In this paper, we describe the double-sided planar process used to fabricate the detectors and the strategy used to suppress surface carrier inversion due to the presence of fixed positive charge at the Si/SiO_2 interface. The key issue in optimizing the fabrication process has been to minimize leakage currents and prevent breakdown at low voltages. Tests show that a drift signal can be measured across the entire length of the detector and that the transit time of the holes varies linearly with the position of the induced charge signal.

I. INTRODUCTION

First introduced ten years ago, silicon drift detectors (SiDDs) are capable of extremely precise energy and two-dimensional position resolution [1, 2]. Notable features of silicon drift detectors include a very small (~0.1 pF) output capacitance that is independent of detector area, modest readout electronics requirements, and minimal cooling requirements. Recently, an energy resolution of 143 eV FWHM at 5.89 keV was reported for a cooled SiDD [3], while position resolution of a few micrometers was reported for a room temperature SiDD [4].

Until now, all silicon drift detectors have been fabricated on n-type substrates. For good position resolution, the starting material must have a very uniform radial dopant distribution which, for high resistivity n-type silicon, can only be obtained via neutron transmutation doping. P-type, float-zone silicon, with radial dopant variations of ~6% [5], is more homogeneous than n-type, float-zone silicon and is only slightly less homogeneous than n-type, neutron transmutation doped material. P-type, float-zone silicon is readily available and relatively inexpensive; in addition, using float-zone silicon obviates any possible complications arising from defects created by the neutron transmutation doping process [6]. Furthermore, there has been some evidence recently that p-type silicon is more radiation-resistant than n-type [7]. These reasons have prompted us to begin developing a SiDD based on p-type substrates.

II. DETECTOR OPERATION AND STRUCTURE

Silicon drift detectors are based on the concept of using an electric field parallel to the detector surface to collect charge. A SiDD consists of a series of parallel p-n junctions formed on both sides of the silicon substrate, as shown schematically in Figure 1. The junctions are reverse biased to deplete the entire bulk of the detector. The voltage at each junction is increased linearly along the length of the detector, and the gradient is set so that a constant electric field is created in the direction parallel to the surface of the detector. When electron-hole pairs are created by a particle passing through the p-type SiDD (p-SiDD), the electrons are swept out by the reverse biased junctions, and the holes are focused down the mid plane of the detector and drift at constant velocity toward the row of readout electrodes at one end of the detector. The distance of the incident particle from the row of readout electrodes is given by the transit time of the holes. The location of the readout electrode gives the second position coordinate. Resolution better than the electrode size can be achieved because of charge division among adjacent readout electrodes.

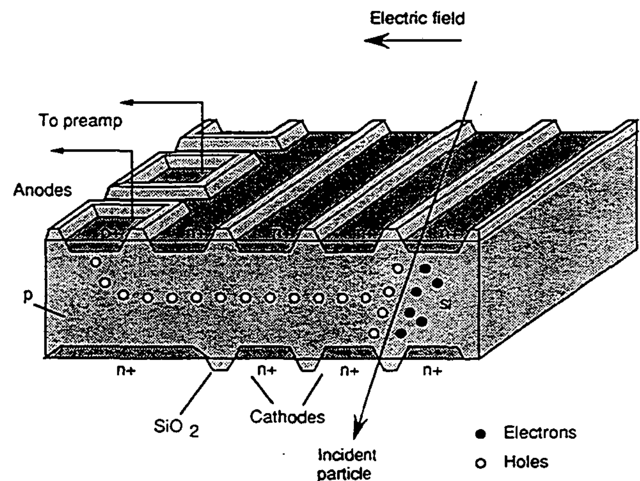

Figure 1 A cross-section of the p-SiDD illustrating the operating principle of the silicon drift detector.

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The geometry of our p-SiDD design is based on an n-type SiDD developed by P. Rehak at Brookhaven National Laboratory. Consequently, we have retained the n-type SiDD nomenclature: i.e., we will refer to the rectifying, p-n^+ junctions as 'cathodes' and the p^+ contacts as 'anodes' throughout this paper. A schematic of the detector geometry is shown in Figure 2. The active region of the detector is 3.98 cm long and consists of 332 parallel, 90 μm wide cathode strips separated by 30 μm wide SiO_2 regions. A high voltage guard structure of floating n^+ strips surrounds three sides of the active region. These were designed to allow the potential to decrease gradually away from the biased cathodes. Since more guarding is needed around the high voltage cathodes than at the low voltage cathodes, the length of the cathodes decreases from 4.99 cm to 3.51 cm to accommodate a larger number of guard strips at the high voltage end. At the low voltage end of the detector are a row of 178 rectangular p^+ anodes for reading out the signals. The anodes have a pitch of 250 μm. At the bottom edge of the detector, 210 μm from the row of anodes, is a 20 μm wide, continuous p^+ 'guard anode' which is grounded in order to provide a sink for the detector leakage current and divert it from the readout anodes.

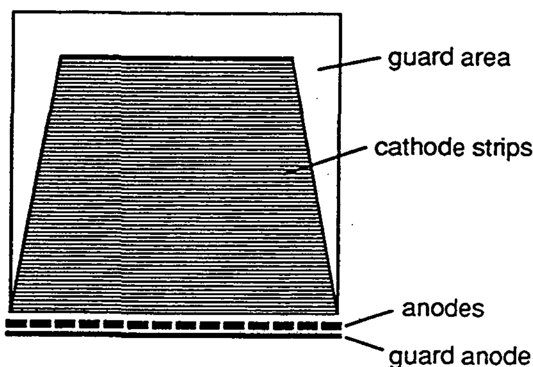

Figure 2 Top view of the p-SiDD geometry. The cathodes and the guard region are p-n^+ diffused strips and the anodes are p^+ implanted regions.

III. DETECTOR FABRICATION

We fabricated the p-SiDDs on 3" diameter, 300 μm thick, float-zone, (111), p-type silicon from Wacker Chemitronics. Capacitance-voltage measurements on diodes fabricated around the periphery of the detectors showed a substrate boron density of ~2×10^{12} cm^{-3}, corresponding to a bulk resistivity of ~7 kΩ-cm.

One of the challenges of fabricating oxide-passivated devices on high purity p-type silicon is related to the fact that positive charge at the Si/SiO_2 interface will attract electrons towards the wafer surface. This can result in inversion of the carrier population at the surface from p-type to n-type. In the p-SiDD, carrier inversion will create conducting channels between neighboring n^+ cathodes. Thus, fabricating p-SiDDs with low leakage currents requires a strategy to prevent electrons from becoming the majority carrier at the Si/SiO_2 interface.

To compensate the positive oxide charge, we increased the hole concentration near the surface of the silicon with a uniform boron implant over both sides of the detector before the oxidation step [8]. However, a trade-off is involved in that, when the surface boron concentration is increased, the p-n^+ junctions suffer avalanche breakdown at lower voltages. To determine an optimal boron concentration that is sufficient to compensate for the positive interface charge but which allows high breakdown voltages, we fabricated a series of detectors with different boron implant doses.

The implant study was carried out as follows: each side of the wafer was implanted at three different energies– 25, 65, and 100 keV. The first p-SiDDs were fabricated with implant doses of 5×10^{11} cm^{-2} at each energy (for a total dose of 1.5×10^{12} cm^{-2} on each side) and were followed by detectors fabricated with higher total implant doses of 3×10^{12} cm^{-2}, 4.5×10^{12} cm^{-2}, and 7.5×10^{12} cm^{-2}. We discuss the results of these different implant doses in the following section.

After the blanket boron implant, the wafers were oxidized in wet O_2 at 1000°C for 2 hrs and in dry O_2 and 1,1,1-trichloroethane at 1060°C for 1 hour. This oxidation process yielded a 6500 Å thick SiO_2 layer that was uniform to within 10 Å over the 3" wafer. The SiO_2 layer was designed to be thick enough to provide an effective diffusion barrier during the phosphorus doping of the cathodes. C-V measurements on MOS capacitor structures fabricated around the periphery of the detectors showed that the areal density of fixed oxide charge was 2×10^{11} cm^{-2} and the interface state density at the flat-band voltage was 4×10^{11} cm^{-2} eV^{-1} for SiO_2 grown under these conditions.

The double-sided mask alignment fixture shown in Figure 3 was used to pattern the windows for the n^+ cathode regions on both sides of the wafer [9]. Using this technique, we have reproducibly obtained top-to-bottom alignment of within 5 μm. The double-sided fabrication process used five mask levels.

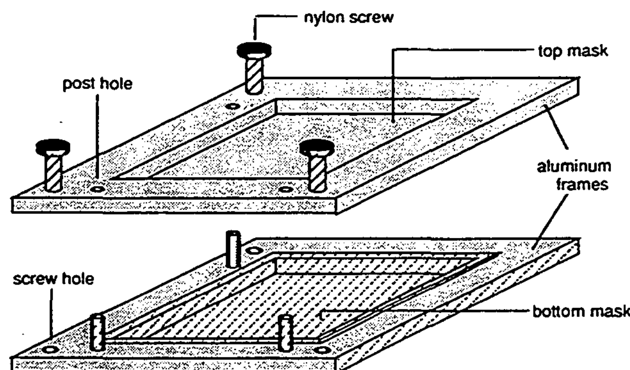

Figure 3 The double-sided mask alignment fixture. Photolithography masks are aligned to each other and epoxied to the aluminum frames. The wafer, sandwiched between the two frames, is then patterned with the top mask aligned to the bottom mask.

After the cathode strips were patterned in the oxide, the n^+ junctions were diffused at 950°C, using $POCl_3$ as the dopant source. The expected dopant profile of the junction with the $3x10^{12}$ cm^{-2} pre-oxidation boron dose is shown in Figure 4. The dopant profile was calculated using the process simulation model, SUPREM-IV [10]. After the phosphorus diffusion, p^+ regions were patterned and implanted with a boron dose of $2x10^{14}$ cm^{-2} at an implant energy of 25 keV. The wafers were annealed in N_2 at 800°C for 30 minutes. Finally, we evaporated 1200 Å thick layers of aluminum and patterned the contacts to the doped regions.

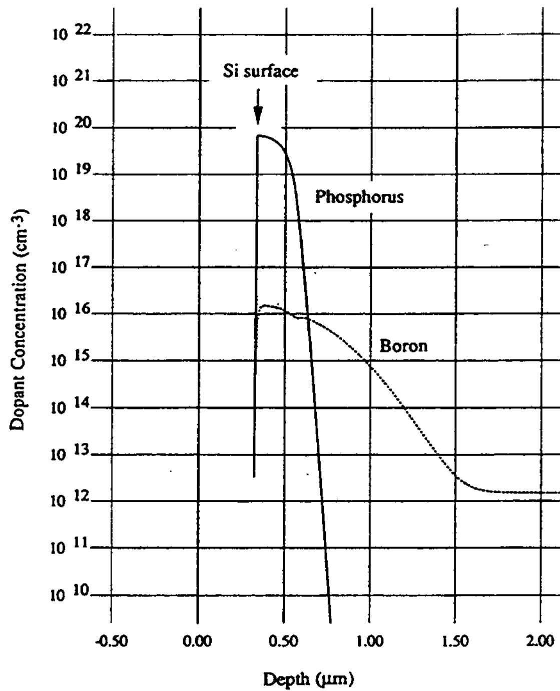

Figure 4 Simulated profile of the phosphorus and boron dopant distributions after thermal processes, for the $3x10^{12}$ cm^{-2} boron implant dose.

IV. MEASUREMENTS

We tested the fabricated detectors in two steps. First we measured the current-voltage characteristics of selected p-n junctions on the detector and test diodes on the same wafer. The I-V measurements were used to determine whether the p-n^+ junctions demonstrated high breakdown voltages and low leakage currents and whether there were any shorts between the cathode strips. After passing this preliminary check, the detectors were diced, then mounted and wire-bonded on to a board for position-sensing measurements.

The dependence of breakdown voltage on boron implant dose is shown in the I-V characteristics of the cathode used to focus the charge signal into the anodes (Figure 5). The $1.5x10^{12}$ cm^{-2} implant dose was not sufficient to prevent surface inversion and resulted in very high leakage currents. The $7.5x10^{12}$ cm^{-2} implant resulted in much lower leakage currents but a breakdown voltage of 50 V, which was less than the depletion voltage of the detector. The $4.5x10^{12}$ cm^{-2} implant gave higher breakdown voltages, but measurements on these detectors were inconclusive and will be pursued further. Optimal results were obtained with detectors fabricated with a $3x10^{12}$ cm^{-2} implant.

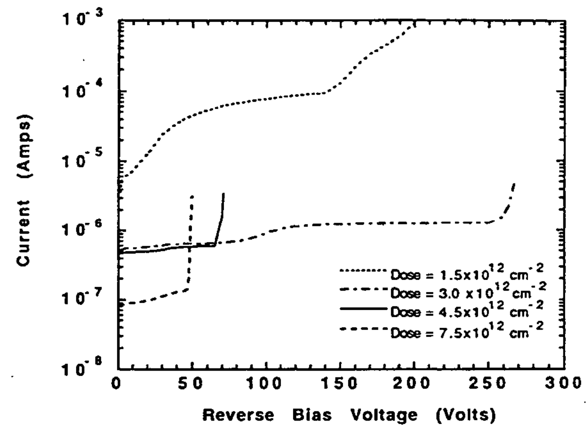

Figure 5 Current-voltage characteristics of the p-n^+ junction used to focus charge into the anode for different pre-oxidation boron implant doses.

The $3x10^{12}$ cm^{-2} implant resulted in junctions with breakdown voltages of 250 V. However, if cathodes over the entire 4 cm x 4 cm active region were biased, the cathode farthest from the anodes could be biased up to 1300 V (corresponding to a drift field of 325 V/cm) before breakdown was seen. This shows that the high voltage guard structure is effective in helping to suppress high local fields that lead to breakdown. Sufficiently high voltages could be applied to the $3x10^{12}$ cm^{-2} implanted p-SiDDs to allow measurement of drift signals created over the entire length of the detectors.

For position-sensitive testing, the detectors were attached to a computer-controlled x-y stage that could be moved in 0.5 µm increments. Weakly absorbed, 1.06 µm light from a pulsed Nd:YAG laser was focused through a microscope objective to a 5 µm diameter spot on the detector. An external resistor voltage divider supplied voltages to the cathodes. The anodes were individually read out through discrete preamplifiers and shaping amplifiers.

Figure 6 shows signals measured with the laser focused at 0.5, 1.0, 2.0, 3.0, and 3.8 cm from the collecting anode. Note that the time before the signal peaks increases as the laser is moved farther from the anode. This demonstrates that charge generated farther from the anode takes longer to drift and be collected at the anode. Note also the increase in the signal width at larger drift distances. This is due to the longer collection time during which the charge packet diffuses.

The electric field applied in the drift direction was nominally 300 V/cm. However, in this measurement only every fifth cathode was wire-bonded, because the board on which the detector was mounted was designed to accommodate every fifth cathode bond. This arrangement probably caused the electric field to be lower in the regions between biased cathodes, resulting in the slow hole drift velocity exhibited in Figure 6.

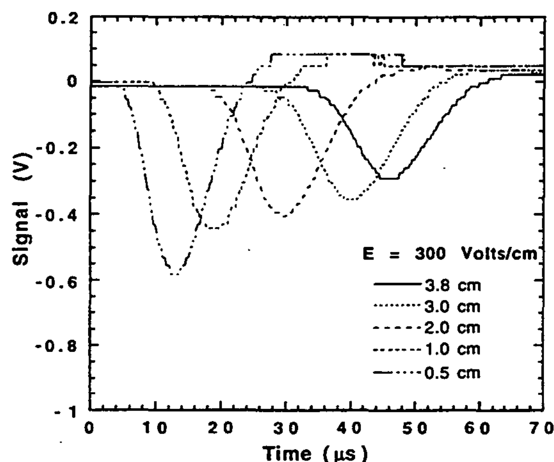

Figure 6 Signals generated with laser focused at 0.5, 1.0, 2.0, 3.0, and 3.8 cm from the anode. Note the increase in peak time and width with drift distance.

To determine if a more uniform electric field would produce the correct hole mobility, we wire-bonded and biased every cathode over a 2.5 mm length of a detector. Figure 7 shows the signal arrival time vs. the distance of the incident light from the anodes. The arrival time varies linearly with position, and the slope of the plot gives the drift velocity of the holes. A plot of the drift velocity at four different electric fields is shown in Figure 8. The hole mobility calculated from these drift measurements was 526 cm^2/V-sec. This agrees well with the expected mobility value of 498 cm^2/V-sec at 22°C. Also, it confirms that the low drift velocity seen in Figure 6 was most likely due to regions of low electric field near the floating cathodes.

When the detector was fully biased, the leakage current of a single anode was seen to vary between 3-4 nA over drift fields ranging from 100-700 V/cm, while the current at the 'guard anode' varied between 7-13 μA. This shows that the guard anode is effective in draining the majority of the detector leakage current, resulting in low leakage currents at the individual readout anodes.

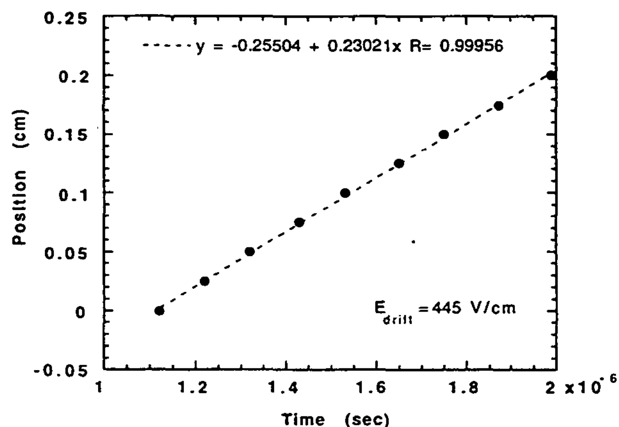

Figure 7 Laser position vs. signal arrival time.

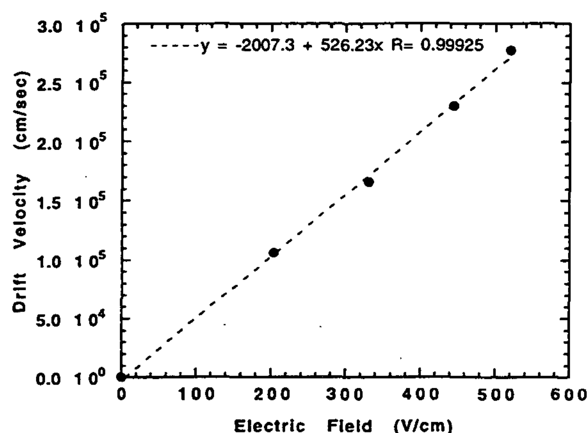

Figure 8 Drift velocity vs. electric field.

V. SUMMARY AND FUTURE WORK

We have fabricated, for the first time, a silicon drift detector using p-type silicon as the starting material. A uniform boron implant of $3x10^{12}$ cm^{-2} before oxidation has been seen to effectively prevent surface inversion due to positive fixed oxide charge while allowing voltages of up to 1300 V to be applied to the detectors without breakdown. Drift measurements conducted for electric fields of up to 520 V/cm show that the signal transit time is linear with position for these devices. The measured hole mobility agrees with the predicted value to within 10%.

For the detector structures presented in this paper, the cathodes must be individually biased using an external resistor voltage divider. Work is presently underway to integrate a voltage divider on the p-SiDD using ion-implanted polycrystalline silicon resistors. Initial results indicate that the ion-implanted polycrystalline silicon yields the very uniform sheet resistances that would be needed for generating constant drift fields in the p-SiDD.

The existence of SiDD technology that uses commercially available and inexpensive high resistivity p-type silicon may encourage broader applications of silicon drift detectors. For example, spectroscopy and imaging applications could use the high energy resolution and large area of the SiDD, and in situ radiation monitoring applications could benefit by its minimal need for cooling. Future developments which will allow the practical use of SiDDs in many applications include the integration of preamplifier electronics on to the SiDD, a self-triggering mechanism, and an improved high voltage guard structure. The existence of the p-type SiDD will also allow comparisons of radiation hardness in p-type and n-type SiDDs, creating a new method by which to compare the effect of irradiation on hole and electron trapping centers in silicon.

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