UCLA
UCLA Electronic Theses and Dissertations

Title
Process Development of Large Wafer Gallium Nitride Reconstitution on Silicon Carrier using Gold to Gold Thermocompression Bonding

Permalink
https://escholarship.org/uc/item/0277d0xz

Author
Kuchhangi, Ankit

Publication Date
2023

Peer reviewed|Thesis/dissertation

eScholarship.org Powered by the California Digital Library
University of California

UNIVERSITY OF CALIFORNIA

Los Angeles

Process Development of Large Wafer Gallium Nitride Reconstitution on Silicon Carrier using Gold to Gold Thermocompression Bonding

A thesis submitted in partial satisfaction

of the requirements for the degree Master of Science

in Materials Science and Engineering

by

Ankit Kuchhangi

2023

© Copyright by

Ankit Kuchhangi

2023

ABSTRACT OF THE THESIS

Process Development of Large Wafer Gallium Nitride Reconstitution

on Silicon Carrier using Gold to Gold Thermocompression Bonding

by

Ankit Kuchhangi

Master of Science in Materials Science and Engineering

University of California, Los Angeles, 2023

Professor Subramanian Srikanteswara Iyer, Chair

III-Vs like GaN and InP are the most promising substrates for high performance RF, photonics, and power electronics. However, III-V processing has been a gating factor in achieving smaller features and better devices. A primary cause of this setback has been large feature sizes resulting from limitations of older equipment. Older equipment must be used because it is compatible with III-V wafer sizes, which are smaller, costlier, and of lower quality compared to silicon wafers. To use the same cutting-edge tools and systems that silicon has immensely benefited from, III-V wafers must be made in a 300 mm format so that they can be processed in the same facilities as Si wafers. This thesis proposes and demonstrates one method of reconstituting gallium nitride (GaN) to create a large wafer that can be processed using large wafer tooling. Investigating these techniques also develops thermocompression bonding process capability that can be transferred to eventual III-V to Si vertical monolithic integration. For example, a GaN power amplifier can be vertically bonded (3D stacked) to a silicon dielet, decreasing the scale of

power delivery networks by almost 1000x (from mm scale to µm scale). However, integration of gold into active silicon devices would require significant reliability study that is outside the scope of this work.

In this thesis, GaN on (111) silicon was chosen as a starting III-V material. After dicing, these dielets were bonded face-to-face to a (100) silicon handler with a gold-to-gold thermocompression bonded interface. The bulk of the dielet thickness is silicon, and it is removed with a hydrofluoric acid, nitric acid, and acetic acid etch (HNA). This leaves behind a thin (< 1 µm) film of III-V substrate, which is planarized and passivated with plasma enhanced chemical vapor deposition (PECVD) oxide and chemical mechanical planarization (CMP). The techniques developed in this thesis can be adapted to reconstitute other III-V materials, like GaN on sapphire, indium phosphide (InP), and gallium arsenide (GaAs).

The thesis of Ankit Kuchhangi is approved.

Mark S. Goorsky

Ya-Hong Xie

Subramanian Srikanteswara Iyer, Committee Chair

University of California, Los Angeles

2023

DEDICATION PAGE

This work is dedicated to my grandparents Rajamma Ajji, Basavaraju Tatha, Jayamma Ajji, and Mahadevappa Tatha who supported me unconditionally throughout my education journey.

TABLE OF CONTENTS

1. Introduction ... 1
1.1. Significance of III-Vs for Power Delivery, RF, and Photonics ... 1
1.2. Current Limitations III-V Substrates ... 2
1.3. Introduction to Packaging – Wafer Reconstitution ... 4
1.4. III-V to Si Integration Possibilities ... 6
1.5. Objective of This Work ... 6
1.6. Organization of This Work ... 8
2. Experimental Process Development ... 9
2.1. Incoming III-V Materials Selection ... 9
2.2. Si Removal ... 9
2.3. Substrate Backside Protection ... 13
2.4. Dicing Development ... 15
2.5. Dielet Bonding ... 15
2.6. PECVD / CMP for Planarization ... 21
2.7. Heterogenous Integration of Multiple Dielets onto Large Substrate ... 23
2.8. Thermal Simulations ... 28
3. Results and Discussion ... 31
3.1. Incoming III-V Materials Selection ... 31
3.2. Si Removal ... 32
3.3. Substrate Backside Protection ... 33
3.4. Dicing Development ... 33
3.5. Dielet Bonding ... 34
3.6. PECVD / CMP for Planarization ... 37
3.7. Heterogenous Integration of Multiple Dielets on Large Substrate ... 37
3.8. Thermal Simulation ... 41
4. Future Work ... 42
5. Conclusions ... 45
References ... 46

LIST OF FIGURES

Figure 1.1.1. Power amplifiers of different substrate technologies offer different efficiencies at different frequencies. 2
Figure 1.3.1. Historical progression of advanced packaging. 5
Figure 1.4.1. 3D stacking heterogenous of III-V to Si. 6
Figure 1.5.1. Diagram of a reconstituted III-V wafer. 8
Figure 2.1.1. Rocking curve (RC) scan of ~400 nm GaN grown on silicon by HVPE (as received). 9
Figure 2.2.1. Si etch rate as a function of composition of HNA etchant. 11
Figure 2.2.2. 2 mm x 2 mm 525 µm thick Si die bonded to a 5 mm x 5 mm 525 µm thick Si “substrate” with an Au-Au bond. 12
Figure 2.3.1. Image of thin film GaN transfer bonded to Si carrier with Au-Au interface. 14
Figure 2.5.1. Micrographs and AFM image of SoG processed with different conditions. 16
Figure 2.5.2. Cured SoG on Si handler that has cracked. 17
Figure 2.5.3. Labelled components of K&S Apama bonder. 19
Figure 2.5.4. Image of die holder that is compatible with the SB-8e that allows for coarse die placement. 19
Figure 2.5.5. Images of shear test failure modes. 21
Figure 2.6.1. Process flow for test vehicle for planarization. 22
Figure 2.6.2. Micrograph of fabricated sample after planarization. 22
Figure 2.6.3. AFM scan measuring topography at the edge of the test structure. 23
Figure 2.7.1 Final experimental process flow for fabrication of a reconstiuted large III-V wafer. 24
Figure 2.7.2. Images of assembled reconsituted wafer. 25
Figure 2.7.3. Reconstituted wafer after HNA etching. 26
Figure 2.7.4. Peeling of PECVD SiO_2 deposited film. 26
Figure 2.7.5. Photograph of reconstituted III-V wafer after CMP. 27
Figure 2.7.6. Stylus profilometer scan data of transferred GaN film. 28
Figure 2.8.1. Finite element analysis of temperature rise in different GaN substrates. 30
Figure 3.3.1. Corrosion of underlying silicon due to gold film discontinuities. 33
Figure 3.5.1. Schematic illustrating problems arising from variations in die thickness. 35
Figure 3.7.1. Micrograph of cracked GaN thermocompression bonded to a Si handler with Au-Au interface. 38
Figure 3.7.3. Micrograph of remaining Si (grey) on top of GaN film (green) resulting from incomplete HNA etch of silicon. 40
Figure 4.0.1. Modified process flow using mechanical grinding to avoid formation of Si islands. 43
Figure 4.0.2. Modified process flow using Au sputtering to avoid formation of Si islands. 44

LIST OF TABLES

Table 1.2.1. Summary of wafer metrics. 4
Table 2.5.1. Important process parameters for bonding. 20
Table 2.6.1. Process conditions for CMP for planarization of 3 µm PECVD oxide on test pattern from Figure 2.6.2. 23
Table 3.1.1. Properties of selected III-V substrates. 32

LIST OF ACRONYMS

AFM	atomic force microscopy
AMHS	automated material handling system
CMOS	complementary metal oxide semiconductor
CMP	chemical mechanical planarization/polishing
CTE	coefficient of thermal expansion
DI	deionized
DRIE	deep reactive ion etch
DSP	double sided polish
EMC	epoxy molding compound
EPD	etch pit density
FCC	face centered cubic
FR-4	flame retardant 4
GaAs	gallium arsenide
GaN	gallium nitride
HCP	hexagonal close packed
HF	hydrogen fluoride
HNA	hydrofluoric acid, nitric acid, and acetic acid
HVPE	hydride vapor phase epitaxy
ICP	inductively coupled plasma
III-V	semiconductor made from group III and group V elements
InFO	integrated fan out
InP	indium phosphide
IOT	internet of things

KGD	known good dies
KOH	potassium hydroxide
LDMOS	laterally diffused metal oxide semiconductor
LLO	laser lift off
LPCVD	low pressure chemical vapor deposition
PECVD	plasma enhanced chemical vapor deposition
PPAC	power, performance, area, and cost
PTFE	polytetrafluoroethylene
RC	rocking curve
RF	radio frequency
RTA	rapid thermal annealing
SERDES	serializer/deserializer
Si	silicon
SiGe	silicon germanium
SiN	silicon nitride
SoG	spin on glass
SSP	single sided polish
TCB	thermocompression bonding
TEOS	Tetraethyl orthosilicate
TMAH	Tetramethylammonium hydroxide
wt%	weight percent
XRD	x-ray diffraction

ACKNOWLEDGEMENTS

My time at UCLA was very enjoyable, despite having a difficult start due to COVID-19 restrictions. I want to thank my fellow UCLA MSE graduate students for making life bearable during the first few quarters. Thanks to Alex, David, Helene, Isabelle, Jack, Julian, Katya, Makenna, Olivia, Siddharth, Stephanie, and partners for showing me how to have fun as a grad student. Thank you to my frisbee friends James, Yotam, Allison, and Michael for getting me out of the apartment on Sunday afternoons and making me run. Thank you to my KRec friends that inspired me to work hard in and out of the gym. Thank you to my MSJ friends for support and general advice during this time of my life.

Thank you to my Keysight coworkers that shared their expertise with me, helping me develop my understanding of semiconductor processing. Thank you to my lab members for your company and your samples. Vineeth Harish, Randall Irwin, Guangqi Ouyang, Siyun Qiao, Golam Sabbir, Dr. Arsalan Alam, Dr. Steven Moran, Dr. Ujash Shah, Dr. Niloofar Shakoorzadeh, and Dr. Yu-Tao Yang have provided engaging academic and nonacademic conversations in our office and lab spaces. I will never forget the times we spent fixing equipment together. I especially want to thank Haoxiang Ren and Krutikesh Sahoo for their time in training me and helping immensely me in the last few months at UCLA. I also want to thank Kyle Jung and Athena Sung-Miller for their support in managing orders and supplies.

Thank you to the members of the UCLA CHIPS consortium for providing funding for my research. Thank you to Minji for help in laser dicing. Thank you to the UCLA NPC and Nanolab/CNSI cleanroom staff for their nearly year-round support. I especially want to thank Lorna, Brian, and Angelica for their continued equipment support during my most stressful hours. I could not have done it without them.

I want to thank my committee members for lending their time and expertise in critically reviewing my thesis. Lastly and most importantly, I want to thank my advisor, Prof. Subramanian Iyer, for his wealth of knowledge and humorous aphorisms. I am humbled to know someone as intelligent as Subu that is always eager to learn. Subu will always be my inspiration to become a better engineer.

1. Introduction

1.1. Significance of III-Vs for Power Delivery, RF, and Photonics

The most widespread semiconductor material used today is silicon. Although silicon has many excellent properties, it too has its limitations. Compound semiconductors formed by group III and group V elements (known as III-Vs), have higher electron mobility and a larger bandgap compared to Si [1.1.1]. These attributes are desired for RF, photonics, and power electronics because larger bandgap materials have higher breakdown voltage, lower leakage current, higher thermal stability (during operation), and improved switching performance due to higher electron mobility (and velocity) [1.1.2][1.1.3]. Although some RF, photonics, and power electronics work has been demonstrated in silicon (e.g. by Iyer and Xie [1.1.1]), such work is admittedly not manufacturable or scalable. From a materials perspective, it is evident silicon is limited and alone may not be able to meet the constant exponential increase in demands of transistor performance and system bandwidth.

In the digital world, silicon CMOS has been the easy choice due to its low leakage current, good power efficiency (for digital logic), and most notably the exponential increase in transistor counts, as predicted by Moore's law. However, for RF and power amplifier applications requiring frequencies greater than 10 GHz, silicon is not the best choice. Figure 1.1.1 plots power amplifier efficiency trends of different technologies. LDMOS and SiGe are all technologies based on silicon wafers substrates and are the lowest performers in the graph. However, because of the ease of integration with CMOS logic, SiGe especially has remained popular. Unfortunately for silicon, the diagram illustrates that LDMOS and SiGe are poor performers compared to III-V materials like GaAs, GaN, and InP, which are three of the most popular and readily available III-V semiconductors.

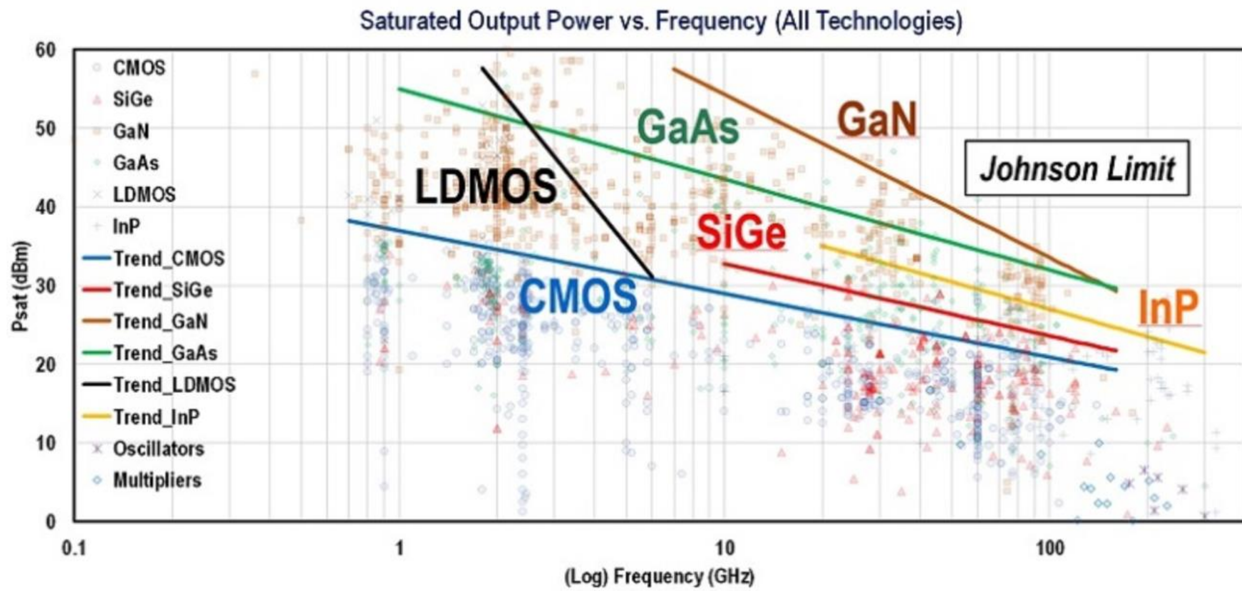


Figure 1.1.1. Power amplifiers of different substrate technologies offer different efficiencies at different frequencies.
Reproduced from [1.1.4].

The choice between implementing a device in the III-V regime or the silicon regime is nuanced and is governed by the needs of the entire system, often summarized by power, performance, area, and cost (PPAC). For example, many mobile and IOT applications have low power, low/medium performance, small area, and low-cost requirements, which is where Si and Si derivative technologies excel. III-V materials are the better choice at the opposite end of the requirement spectrum. Arguably the biggest challenge for implementing technology with a III-V semiconductor is its limitation on integration with other components.

1.2. Current Limitations III-V Substrates

As established, silicon's material properties aren't ideal, but the silicon wafer is fantastic. Firstly, Si wafers can be manufactured in large diameters. 300 mm Si wafers are readily available, and it is the dominant form factor for most commercial fabs. 450 mm wafers are also feasible but have not been adopted due to non-technical reasons. Large wafer diameters are important because it directly impacts chip yield. Larger wafers have a lower periphery to area ratio, so a fewer percent of reticles/parts are lost

at the edges. Edge exclusion zones also waste proportionally less of the wafer. Secondly, silicon wafers have high quality and purity. Typical purity values are 99.9999999% (nine nines purity) [1.2.1] and can later be doped as desired. Wafer quality can be determined by etch pit density (EPD), a technique that exploits faster etch rates of defects (e.g. threading dislocation defects). Automated optical inspection can then reveal defect rate per area. Silicon wafer EPD has been found to be on the order of only 10 – 100 cm^{-2} [1.2.2]. Thirdly, silicon wafers are very cheap. A single 300mm wafer can be purchased for around USD $200 (in January 2023), and bulk discounts probably decrease this price to roughly USD $100 [1.2.3]. It is evident that silicon substrates are big, high quality, and cheap. These three factors have made it easy and convenient to build on silicon.

In contrast, no III-V substrate offers those three qualities. Because silicon wafers are formed from a melt of only silicon atoms, Czochralski growth is simple and straightforward. However, compound semiconductors have an additional challenge: controlling vapor pressure of the two constituent elements. For example, in an InP melt, phosphorous overpressure must be maintained because phosphorous has a higher vapor pressure than indium. Controlling of vapor pressure requires more complicated boule growth techniques, like liquid encapsulated Czochralski, Bridgman growth, or vertical temperature gradient freezing. Some III-V wafers are not even bulk substrates. For example, GaN is most typically grown on sapphire or silicon substrates. Although freestanding GaN exists, it is about ten times more expensive [1.2.4] than either of the other two GaN films heteroepitaxially grown. Admittedly, freestanding GaN is higher quality than the heteroepitaxy films, so the substrate choice must be carefully chosen to balance cost and quality. Lastly, all III-V wafers are more expensive than Si wafers and are also lower quality. Table 1.2.1 summarizes some of aforementioned criteria of substrates.

Table 1.2.1. Summary of wafer metrics. Dislocation densities and wafer costs are approximate order-of-magnitude values.			
Substrate	Common Size (mm)	Dislocation Density (cm^{-2})	Bulk order wafer cost (USD/in^2)
Si	300	< 1E2	1
GaN on Si	300	5E8	25
GaN on Sapphire	100	5E8	25
GaN (bulk)	100	1E5	> 100
InP (bulk)	100	1E4	30
InP on Si	300	1E8	5
GaAs (bulk)	150	1E5	25
GaAs on Si	300	1E7	5

As a result of small III-V wafer sizes (especially native GaAs and InP), III-V wafers have been segregated to their own fabs with tooling designed for smaller equipment. Lots in such fabs are handled manually (without AMHS) and equipment is typically old and lacks modern features. For example, immersion lithography is not possible with InP wafers because such systems are not tooled to handle the small 3” or 4” wafers. Old PECVD, ICP, CMP, AOI, etc. tools lack new features as well. Consequently, due to equipment limitations, minimum feature sizes in III-V wafers are approximately 250 nm, almost two orders of magnitude larger than that of Si, which has feature sizes under 10 nm [1.2.5]. III-V processing has been stuck 20 – 40 years behind Si because its tools are 20 – 40 years behind.

1.3. Introduction to Packaging – Wafer Reconstitution

As Moore’s law becomes increasingly harder to follow, the semiconductors industry has turned to electronics packaging as a cost-effective method of improving system scaling. Figure 1.3.1 depicts the advances made in packaging over the last few decades. Some of the latest innovations in packaging technology, especially wafer level packages, have borrowed heavily from foundry technologies and have blurred the lines between packaging facilities and foundry facilities. One example is TSMC’s Integrated Fan Out (InFO) packaging in which known good dies (KGD) are reconstituted into a new wafer. While still on the wafer, unpackaged dielets are tested and sorted. The wafer is diced, and epoxy molding compound (EMC) iss flowed around precisely placed dielets [1.3.1]. This results in a new composite wafer made of

silicon and polymer that can (for the most part) continue to be processed like a single silicon wafer. Compared to organic FR-4 panels, the wafer form factor is compatible with most advanced semiconductor tooling, which gives InFO wafers an advantage over conventional packaging schemes. Such wafer level packaging (like InFO) is only viable with reconstitution because it allows for the selection of only KGD to be processed. Requiring the whole silicon wafer to undergo RDL buildup, bumping, etc. would otherwise be a waste of valuable processing resources.

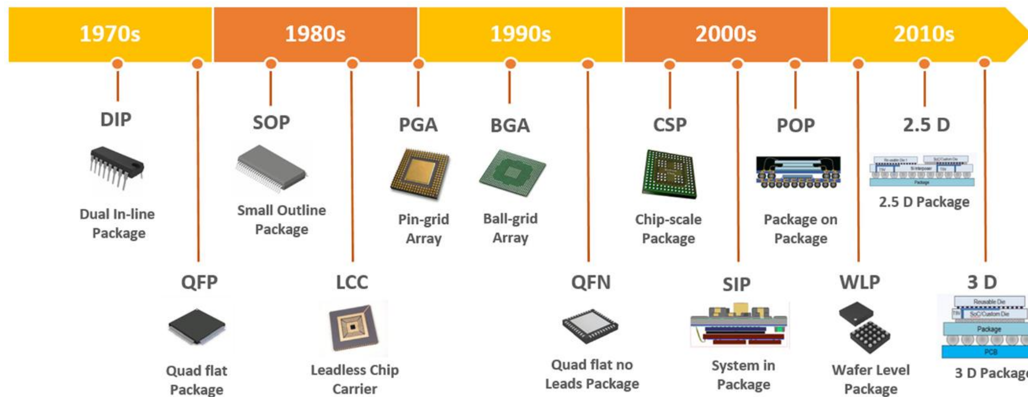


Figure 1.3.1. Historical progression of advanced packaging.
Reproduced from [1.3.2].

This idea of testing, separating KGD, and reassembling parts is a powerful and widely applicable technique that can be used to make low yielding small parts into a high yielding larger part. This technique is the basis behind the Silicon Interconnect Fabric (SiIF) a novel heterogenous interconnect platform [1.3.3]. Instead of just producing a reconstituted wafer as is done in InFO, the SiIF produces a reconstituted datacenter by assembling KGD processors, memory, SERDES, thermal dissipation units, and other individual components onto a single patterned 300mm silicon wafer.

The same concept of reconstitution can also be applied to III-V substrates. As previously mentioned, III-V substrates are lacking, so reassembling dielets into a larger substrate can resolve many problems. Larger III-V wafers could be processed using the same tooling as Si, which may drastically decrease the feature size and improve performance of III-V devices. Analogous to KGD testing/sorting, only high quality regions of a III-V wafer can be reconstituted. For example, our GaN on Si vendor indicated

that the GaN thickness has a ± 50 nm within wafer thickness that is nonlinear and not monotonic as a function of the radius. Wafer reconstitution allows for the selection of only the desired regions of GaN, e.g. a ring that excludes the very center and edges of the wafer. This can improve the overall processability and uniformity of the wafer.

1.4. III-V to Si Integration Possibilities

In addition to the aforementioned benefits of III-V reconstitution, it also develops processing expertise in III-V to Si 3D stacking. Figure 1.4.1 illustrates an example of 3D stacking. A GaN HEMT power amplifier is vertically bonded on top of a Si CMOS chip. The Si CMOS can act as the brains and send and receive information through the GaN dielet, which has RF power amplifiers. All of this can be bonded to a substrate, so this compact stack can act as an entire system. Without 3D stacking technology, each of these components would have to be packaged separately and signals would have to be routed through longer and lossier wiring which can generate significant heat. A structure like what is shown in Figure 1.4.1 would offer superior performance and throughput while requiring less power and less space.

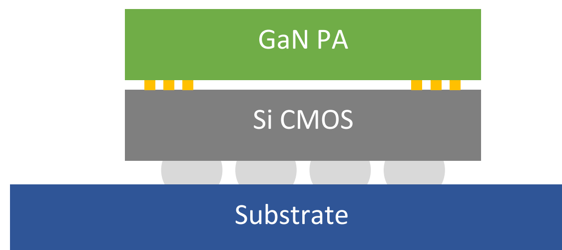


Figure 1.4.1. 3D stacking heterogenous of III-V to Si.

1.5. Objective of This Work

The focus of this work is to create a reconstituted III-V substrate. As described in the previous section, tradeoffs must be made to balance III-V substrate cost, size, and quality. However, using packaging-like technologies, primarily thermocompression bonding, the substrate itself can be improved and can ameliorate lackluster III-V substrates.

Unlike silicon FinFETs which are partially built into the wafer (e.g. the fin is subtractively formed), most III-V devices are built on top of the wafer. III-V devices are built above the surface of the wafer with epitaxially grown layers. The substrate material is important insofar as the epi quality is good and the lattice is transferred to the epi. Thus, the desired reconstituted wafer only needs to be thick enough to ensure templated growth. For strain purposes, the III-V substrate film should be at least the as thick as the epi stack. Using InP HBTs as an example, this would translate to a thickness of around 1 µm. As presented in Section 1.1, InP, GaAs, and GaN are the most promising materials. However, due to challenges with material sourcing, InP/GaAs toxicity concerns, and outsourced fabrication turnaround time, GaN on silicon was chosen as the starting material.

The main contributions of this work are to:

1. Demonstrate thin layer transfer of GaN to a silicon carrier wafer using thermocompression bonding.
2. Reconstitute a III-V wafer to a larger diameter.
3. Planarize the reconstituted wafer to prepare it for subsequent epi growth.

An abstract generic vision of such a reconstituted III-V substrate is shown in Figure 1.5.1. On a handler wafer, like a Si wafer, a bonding layer exists. This bonding layer can be applied directly to the handler, to the dielets, or to both. This bonding layer needs to be dimensionally and thermally stable. Next, the dielet must be flip chip attached to the handler wafer. If thin film (and not bulk III-V) is desired, the thick dielet must somehow be reduced in thickness. Lastly, the dielets must be planarized using a gap fill material. The exact choice of materials will be discussed in Section 2, and the final comprehensive process flow will be presented in Section 2.7.

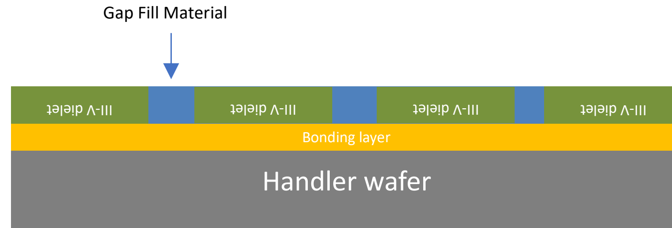


Figure 1.5.1. Diagram of a reconstituted III-V wafer.

The benefits of such a reconstituted wafer are numerous. First, larger diameter III-V wafers can be produced, enabling compatibility with newer tools. Second, the quality of III-V film can be improved by only selecting the best III-V dielets to reconstitute. Third, CTE mismatch between the handler and III-V can be addressed because the III-V films are segmented. Fourth, the use of a thermally conductive bonding layer can improve the thermal budget of fabricated devices.

1.6. Organization of This Work

Chapter 1 provides adequate background about the use of III-V semiconductors and why III-Vs can be a better choice for certain applications. This section also covers some of the shortcomings of III-V substrates. Chapter 2 describes the experimental process development, which includes the goals of process flow and explanations of individual experiments which were used to fine tune the process. Chapter 3 is a discussion on each of the sections of Chapter 2. Key results are highlighted, and shortcomings are explained. Chapter 4 integrates ideas to resolve issues faced during the experimental work. Chapter 5 is a conclusion that summarizes this work and explains its significance.

2. Experimental Process Development

2.1. Incoming III-V Materials Selection

For this work, three different III-V wafers were considered: GaN on sapphire, GaN on silicon, and InP. Although InP wafers were readily available and on hand, due to complications with toxicity of handling InP and difficulty in finding vendors for quality dicing, it was unfortunately ruled out of selection. GaN is beneficial in this regard as it is nontoxic. GaN on sapphire substrates are typically debonded using a process called laser lift off (LLO) [2.1.1]. However, LLO is a complicated process and lack of immediately available tools for LLO made this sapphire GaN impractical. For this critical reason, GaN on silicon is chosen as a the III-V substrate. 2" undoped GaN on silicon wafers were fabricated by and purchased from Kyma Technologies. As per manufacturer spec, GaN was deposited by HVPE and has a within waver uniformity of 400 – 500 nm. Figure 2.1.1 shows an x-ray rocking curve scan showing a FWHM of 1700 arcsec. Optical microscopy of the GaN revealed color variation across the wafer. Prior to any processing, the GaN- Si wafers were cleaned to remove any particles.

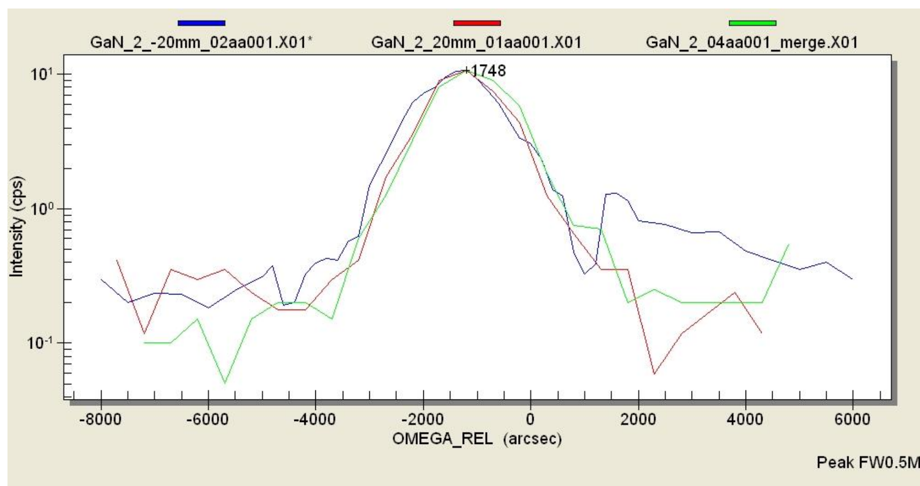


Figure 2.1.1. Rocking curve (RC) scan of ~400 nm GaN grown on silicon by HVPE (as received). Each colored curve is a different scan location. Scan is performed at an angle of 36.458° and x-axis is labelled relative to this.

2.2. Si Removal

To transfer only the thin GaN film from the GaN-Si substrate, the Si must be removed. Silicon removal can be done either through mechanical grinding, a Smartcut-like exfoliation process, or chemical/plasma etching. Mechanical polishing is fast but may result in breakage or deep scratching. An exfoliation process is very complicated and requires specialized high flux implanters. For this work, a chemical etchant solution, hydrochloric acid, nitric acid, and acetic acid (HNA) was employed to remove the bulk of the Si. Other liquid based chemical etchants like TMAH or KOH were considered. However, these etchants are anisotropic and etch slower against the (111) direction. KOH etch rate of the (111) plane is around 0.01 µm/min and the etch rate of TMAH is similarly slow at 0.017 µm/min [2.2.1]. Etching away 100 µm of silicon to release GaN would take close to 100 hours. HNA is much faster and is isotropic, up to tens of microns per minute.

Experiments were performed to maximize fast removal rate of Si and minimize GaN damage, while preventing thermal runaway. Robbins and Schwartz provide a ternary etch rate diagram, reproduced in Figure 2.2.1. Hydrofluoric acid (HF) is a well-known etchant of silicon dioxide. Nitric acid is a strong oxidizer, and it oxidizes the surface of the silicon, which is then etched away by the HF [2.2.2]. Acetic acid is added to slow down the reaction by diluting rate limiting species (which is important for safety). Because the exact mechanism works through hole injection, there does appear to be some effect of dopant type and concentration which affects the etch rate [2.2.3]. However, the silicon on which the GaN is grown is p type (boron doped, 1-10 Ωcm), similar to most literature, so no additional considerations need be taken.

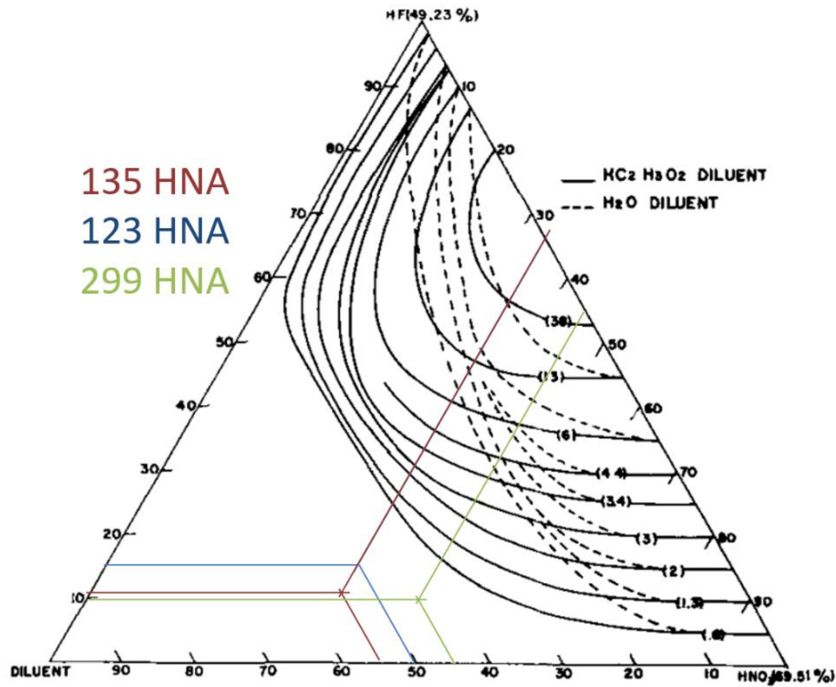
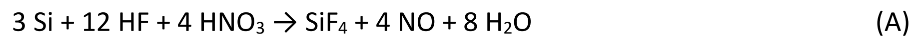


Figure 2.2.1. Si etch rate as a function of composition of HNA etchant.
Diluent refers to glacial acetic acid. The rate curves are specified in mils (thousandths of an inch) per minute. Modifications have been made to include points corresponding to the three different etch solutions that were investigated. Reproduced from [2.2.2].

The purchased GaN samples were grown on nominally 275 µm Si and maximum etch time was target to be 2h (chosen for reasonable throughput). Therefore, HNA chemistry must etch Si ~2.3 µm / min to be viable. All HNA tests were performed with small 2 mm x 2 mm die samples. Robbins and Schwartz provide stoichiometry for the HNA etch reproduced in Equation A:



$$3\,Si + 12\,HF + 4\,HNO_3 \rightarrow SiF_4 + 4\,NO + 8\,H_2O \qquad \text{(A)}$$

From this, a minimum quantity of HF must be supplied to completely remove the silicon. The nominal Si thickness is 275 µm, but samples have been measured to be up to 300 µm. At a density of 2.33 g/cm^3, every square millimeter of Si has a mass of 0.7 µg, or 2.5 × 10^{-8} mol atoms. By stoichiometry, this requires 1.0 × 10 $^{-7}$ mol HF and 3.3 × 10 $^{-8}$ mol nitric acid to completely etch. 49 wt% HF (in water) is used for all experiments. The solution has a density of 1.15 g/mL and HF has a molar mass of 20 g/mol, so 3.5 × 10 $^{-6}$ mL of HF solution are required per mm^2 of Si. 70 wt% nitric acid was used for all experiments. The

solution has a density of 1.41 g/mL and HNO_3 has a molar mass of 63 g/mol, so 4.2×10^{-6} mL of nitric acid solution are required per mm^2 of Si. This is well below the minimum recommendation of HNA solution to avoid runaway [2.2.4], so safety suggestions have been exceeded. Thermal runaway is minimized with a greater HNA volume, but solution disposal and handling are safer with lesser volume. A total solution volume of 300 mL was chosen as a suitable compromise. To avoid exothermic reactions associated with enthalpy of mixing, acetic acid was added to a PTFE beaker, followed by slow addition of nitric acid and finally slow addition of HF. The solution was stirred with a PTFE rod and swirled gently for around 5 minutes prior to addition of any samples to ensure good mixing.

20 nm of Ti and 200 nm of Au was deposited (either using evaporation or sputtering) on the front polished surface prior to dicing (see Section 2.3). Some dies were thermocompression bonded to a silicon substrate that also had the same Ti/Au stack up (see Section 2.5). For HNA Si etch rate experiments, most dies were 525 μm thick Si with no GaN present. Figure 2.2.2 is an image of a sample. Gold is exposed on the substrate and is not etched or otherwise attacked by the HNA solution.

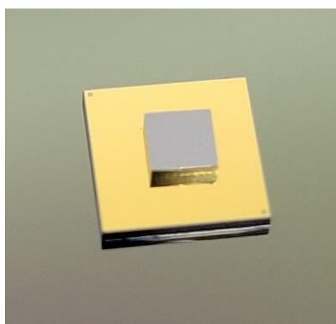


Figure 2.2.2. 2 mm x 2 mm 525 μm thick Si die bonded to a 5 mm x 5 mm 525 μm thick Si "substrate" with an Au-Au bond.

The first tested etch solution was HNA 135 made with 30 mL HF, 90 mL nitric acid, and 150 mL of acetic acid. Bonded samples were placed in solution and the solution was left unagitated for about 75 minutes. This resulted in a total thickness reduction of removal of about 100 μm (or roughly 50 μm from the die) as measured by an electronic thickness gauge. The calculated removal rate for the prepared HNA 135 solution was around 0.66 μm per minute, far too slow to be effective.

The second tested etch solution was HNA 123, made with 50 mL of HF, 100 mL of nitric acid, and 150 mL of acetic acid. Unbonded samples (a Si die piece with sputtered Au protection) were placed in solution. This solution was stirred vigorously with a PTFE rod for about 10 minutes, and then left stationary for another 60 minutes. The average thickness reduction measured across three dies was 173 µm, giving an average etch rate of 2.5 µm/min. This is an acceptable number and meets the criteria mentioned above.

The third tested etch solution was HNA 299. From Figure 2.2.1, this etch solution should be at least as reactive as HNA 123. The solution was made with 30 mL HF, 135 mL of nitric acid, and 135 mL of acetic acid. This ratio was chosen because it is safer than 123 due to the reduced HF concentration but just as fast. Samples were etched for 30 minutes and found to have a maximum etch rate of 1 µm/min, too slow to be effective.

Hot (80 °C) TMAH and KOH were tested on (111) silicon dies, but no thickness reduction was observed after 20 minutes of etching in either etchant. This is in agreement with literature values [2.2.1]. Although DRIE (Bosch process) systems are available for fast vertical silicon etch, due to the presence of gold, which is readily exposed at the surface of the handler, samples cannot be etched due to risk of contamination of the process chamber. From these experiments, HNA 123 was chosen as the best means to etch away the bulk of Si.

2.3. Substrate Backside Protection

Deepu [2.3.1] used LPCVD as a protection against HNA etch with good 400:1 selectivity. LPCVD films are generally denser than PECVD films, but are slower deposited [2.3.2]. For quick turnaround times and low volume, PECVD films were investigated. Three different types of films were investigated, a high frequency SiN film, a low frequency SiN film, and a low stress SiN film. Two different PECVD tools were used, an STS Multiplex PECVD and a Plasma-Therm Vision. Recipes were developed and maintained by UCLA cleanroom staff.

Approximately 100 nm of each film was deposited on the polished face of diced 2 mm x 2 mm Si pieces. Each recipe has a different deposition rate so times varied between 2.5 minutes to 14.5 minutes. Film thicknesses were verified with a Nanometrics Nanospec reflectometer. Each sample was placed in a HNA 299 solution for 30 minutes. No SiN remained after 30 minutes. It was later discovered that just 2.5 minutes of immersion in the HNA was enough to completely strip the nitride and the underlying 3 µm thick pad oxide (furnace deposited).

The next strategy was to use gold as an inert material to protect the backside of the handler wafer from HNA etching. Two options were investigated, a sputtered sample (fabricated with a Denton Discovery) that had 20 nm Ti, 30 nm Pt, and 200 nm Au and an evaporated sample that had 20 nm Ti and 200 nm Au (fabricated with a CHA MARK-40). To determine if the handler needed to be single sided polish (SSP) or double sided polish (DSP), sputtering was used to deposit the film both on the polished side as well as the unpolished side. The polished side is known to have a peak-valley roughness of < 1 nm, and the unpolished backside is known to have a peak-valley roughness in the 1-5 µm range, which would likely create conformality challenges for evaporation. The 3 samples were immersed in HNA 299 for 30 minutes.

Samples were bonded and etched away using the HNA etch, as illustrated in Figure 2.3.1. The etch removed some GaN, which is undesirable and didn't completely etch away the Si, which is also undesirable. Further discussion appears in Section 3.2 and 3.7.

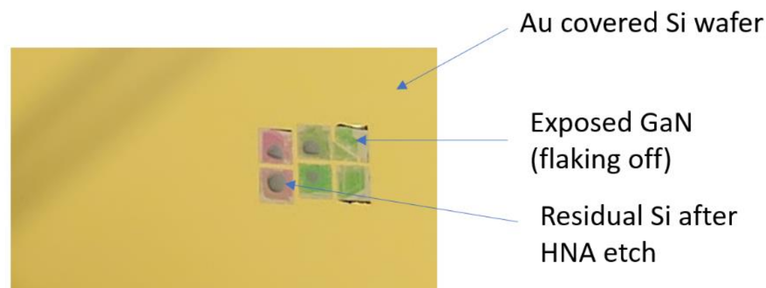


Figure 2.3.1. Image of thin film GaN transfer bonded to Si carrier with Au-Au interface.

2.4. Dicing Development

Prior to any dicing, the GaN wafer was protected with soft-cured AZ 5214 photoresist, then mounted on dicing tape for handling and mechanical rigidity. Laser dicing was performed using an LPKF ProtoLaser U4, a 355 nm UV laser micromachining tool. The GaN-Si wafer was diced into 2 mm x 2 mm dielets. Table 2.4.1 reports the parameters used in laser dicing. Cut depth was around 150 µm, after which samples could be separated manually and handled. Laser kerf width was 100 µm. After singulation, photoresist was removed with ultrasonic vibration in acetone, then cleaned further with methanol, water, and isopropyl alcohol. Only GaN dielets with a particle free and defect free surface were used for the forthcoming experiments.

Table 2.4.1. Parameters used for laser dicing of GaN on (111) Si.

Laser Power (W)	Laser Pulse Frequency (kHz)	Focused Laser Spot Size (µm)	Laser Scan Rate (mm/s)	Laser Defocus Height (µm)	Repetitions
5	50	30	200	650	16

2.5. Dielet Bonding

Two different methods of reconstituting dielets into a wafer were investigated. Both methods rely on a permanent adhesion between the dielet and the handler material. The first method is dielet attachment by oxide bonding. This typically refers to solid oxide films being bonded to other solid oxide films, but there are significant challenges with such bonding. The interface must be extremely flat, with sub-nanometer roughness, and free of any particles. Another alternative type of oxide bond can be made with the use of a spin on glass (SoG). SoG is a liquid solution of TEOS based molecules dissolved in alcoholic solvents, with optional additives [2.5.1]. As the name suggests, spin on glasses are spun on as a liquid. With appropriate heat treatment, the liquid film will transform into a solid glass like film. The film undergoes various morphology changes, evolving and consuming pores to self-densify. Figure 2.5.1 shows

two optical images of SoG spun onto silicon with different spin and cure conditions and an AFM image of the low porosity film.

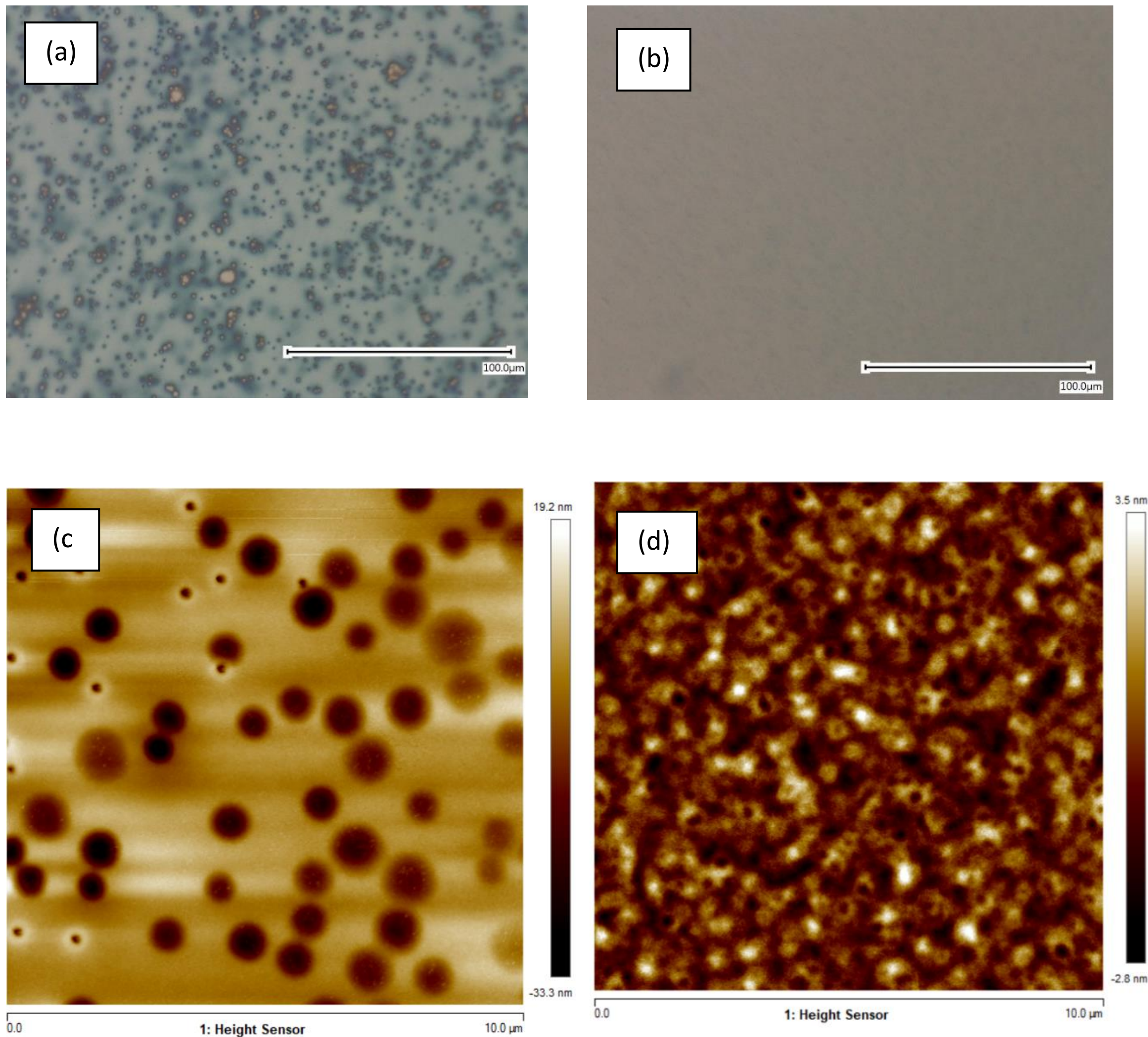


Figure 2.5.1. Micrographs and AFM image of SoG processed with different conditions.
(a) Micrograph of SoG film with significant porosity; (b) micrograph of SoG film with low porosity; (c) AFM scan of (a); (d) AFM scan of (b).

The advantage of SoG is the temperature and material compatibility. Cured undoped SoG primarily only contains silicon and oxygen, which are already present in most substrates. SoG films are also stable to temperatures above 600 °C, so it is not a limiting factor for future process steps. SoG films have three primary disadvantages. Firstly, they are prone to cracking. Humidity present in the atmosphere is sufficient

to spontaneously crack cured SoG films [2.5.2]. Any water present is a major concern. Figure 2.5.2 depicts cured SoG that has spontaneously cracked. The second disadvantage is that curing must occur at high temperatures (ideally > 400 °C) for extended time (ideally > 1h). This can create stress due to CTE mismatch. Lastly, the use of an oxide as an interface material results in lower thermal conductivity of the substrate in the Z direction. This is undesirable, as explained in Section 3.1.

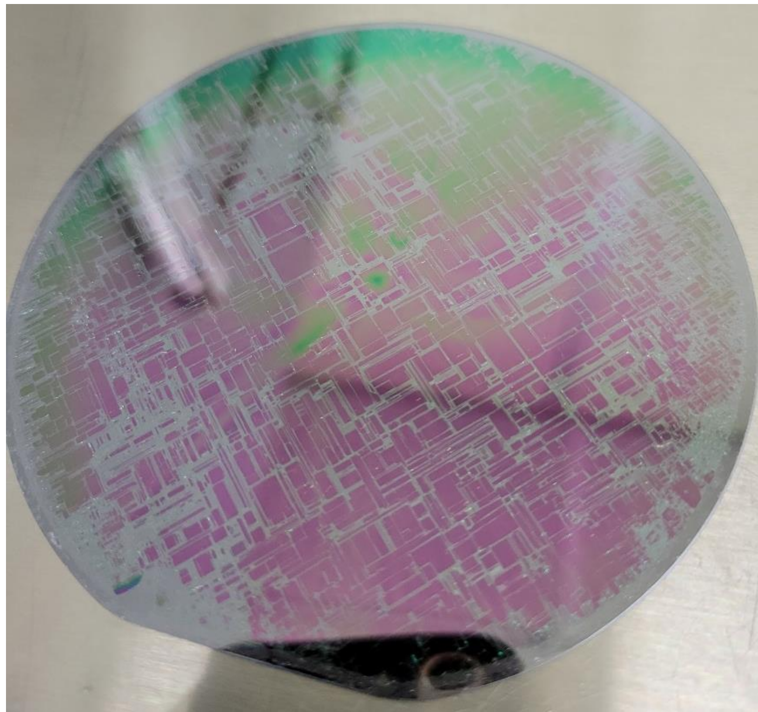


Figure 2.5.2. Cured SoG on Si handler that has cracked.

The other means of dielet attach is with a metal-metal bond with thermocompression bonding (TCB). TCB is the application of energy and pressure to two parts to force diffusion across the surfaces such that a mechanical joint is formed. A review of TCB is done by K&S [2.5.3]. TCB has three distinct advantages. Firstly, TCB is that is a widely used process, and TCB can be easily modelled, making TCB a more approachable solution to dielet attach. Second, the metal-to-metal interface creates a very low thermal resistance, which simplifies subsequent processing conditions. Third, because metals are more compliant than hard oxide, perfect surface conditions are not required because the metal will slightly deform with sufficient heat and pressure. However, TCB has two disadvantages. Firstly, the introduction of specific

metals can adversely affect the III-V and/or the Si handler. For example, the use of Au or Cu as a bonding interface presents a challenge due to atomic diffusion. This problem can be solved with diffusion barriers. Secondly, metal compatibility in tools is less guaranteed than oxide. Some tools are adversely affected by exposed metal features. Some fabs even prohibit certain metals from use due to contamination.

Both SoG and TCB were investigated as means for dielet attach. The metal interface layer was a multistack layer of 20 nm Ti (for adhesion), 30 nm of Pt (as a diffusion barrier), and 200 nm of Au (as the malleable contact bond layer). Two tools are available for bonding. A K&S Apama can align and bond individual dies to a substrate with force up to 300N, temperature up to 300 °C, and temperature ramp rates up to 200 °C/sec. A Karl Suss SB-8e wafer bonder is also available that offers temperatures up to 550 °C and forces up to 20 kN in a high vacuum environment (10^{-5} mbar). Both systems have their own advantage and bonding can be performed on both systems sequentially to improve throughput [2.5.4]. A close up image of the chuck, optic, and bond arm of the Apama is shown in Figure 2.5.3. For achieving coarse, unaligned die placement on the SB-8e, a mechanical aligner was fabricated on a silicon wafer, on which dies can be placed in pockets and bonded to within ~100 µm alignment. An image of this is presented in Figure 2.5.4. Only TCB dielet attachment was found to be successful. No processing conditions resulted in bonding of III-V (or III-V surrogates) to a Si handler using a SoG interface. As a result, only TCB data will be presented in this work.

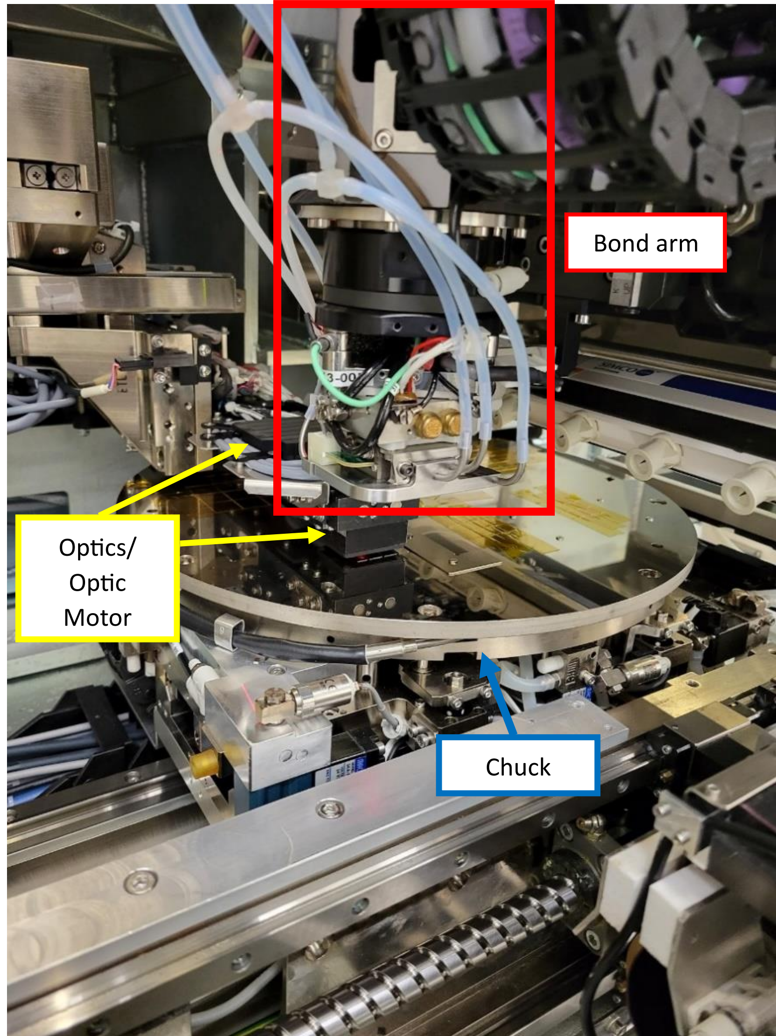


Figure 2.5.3. Labelled components of K&S Apama bonder.

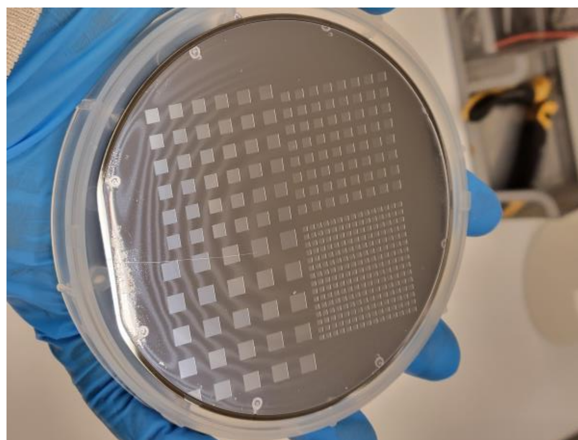


Figure 2.5.4. Image of die holder that is compatible with the SB-8e that allows for coarse die placement.

From prior work conducted at UCLA [1.3.3] [2.5.5], four variations of bond conditions were tested, the details of which can be found in Table 2.5.1. Bond quality was evaluated destructively using a Nordson Dage shear tool. For all trials, 6 bonded dies were sheared off a bonded substrate, an example of which is pictured in Figure 2.2.2. Shear force required to break or remove dies was well above the 1X specification set by MIL-STD-882-2 Method 2019.11 (Die Shear Strength), which is 2.5 kgf (25 N) [2.5.6]. Most dies also meet or exceed the 2X spec of 5.0 kgf (50 N). Two failure modes were observed, shown in Figure 2.5.5. Shearing of some parts either resulted in the disintegration of the die and/or substrate or in the delamination of the die at the bonding interface. Above ~ 80 N, it was observed for parts to fail due to the disintegration of the Si, and below ~80 N failure was typically caused by delamination at the bonding interface. The fourth iteration of TCB parameters was chosen for the final assembly as it met shear force criteria and did not rely on gang bonding from the Karl Suss. Reasons for avoiding the Karl Suss are explained in the discussion in Section 3.5.

Table 2.5.1. Important process parameters for bonding.
Other K&S Apama parameters include: 200 °C/sec ramp rate and a force ramp rate of 50%. Other Karl Suss SB-8e parameters include: 1.0×10^{-4} mBar chamber pressure and ~ 30 °C/min ramp rate.
Note: The diaphragm area of the Karl Suss SB-8e is approximately that of a 150 mm wafer.

	K&S Apama params				Karl Suss SB-8e params				Avg Shear Force (N)
TCB iteration	Force (N)	Bond Time (s)	Bond Arm Temp (°C)	Chuck Temp (°C)	Force per die (N)	Bond Time (s)	Lower Chuck Temp (°C)	Upper Platen Temp (°C)	
1	275	60	300	100	-	-	-	-	44
2	-	-	-	-	370	3600	250	250	170
3	275	60	300	100	370	3600	250	250	145
4	100	60	300	100	-	-	-	-	51

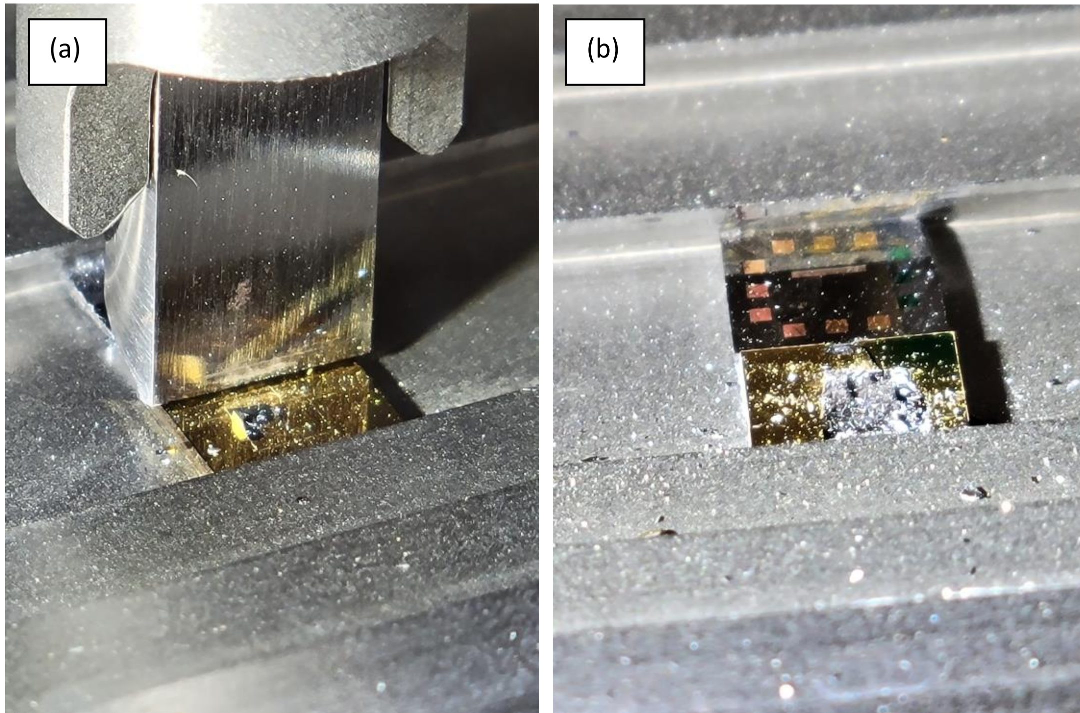


Figure 2.5.5. Images of shear test failure modes.
(a) Example of delamination. The gold surface of the substrate is still intact, and the die was sheared and forcefully ejected away (not pictured). (b) The Au-Au bond was so strong that the substrate silicon was the weakest material and it fractured, leaving behind a deeply gouged substrate. The substrate and/or die typically both break and crumble in this failure mode.

2.6. PECVD / CMP for Planarization

Process development and demonstration of oxide planarization was done with a different test vehicle. Figure 2.6.1 illustrates the fabrication of the test vehicle, and Figure 2.6.2 shows a micrograph of the sample. A high aspect ratio feature of 4 µm wide in X, 8 µm length in Y, and 0.5 µm tall in Z was chosen to test the limit of the CMP process. CMP dishing occurs where softer material abrades and/or is chemically etched away faster than the harder material (the polish stop). In this case, the PECVD oxide is the softer material which will dish and PECVD nitride is the harder material which will act as the polish stop. On the real sample, PECVD oxide is again the softer material, and GaN is the harder material which acts as the polish stop. SiN has a reported hardness of 10 - 13 GPa [2.5.7], GaN has a reported hardness of 19 GPa

measured [2.6.1], and SiO_2 which has a reported hardness of 3-4 GPa [2.6.2], all measured by Berkovich indentation at a depth of 50 nm. Thus, it is established that for simplicity, SiN can be used as a cost-effective surrogate for development of CMP planarization.

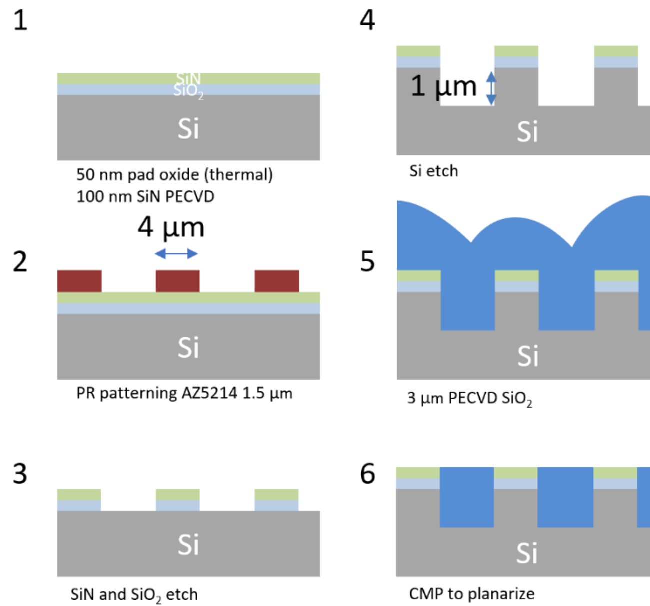


Figure 2.6.1. Process flow for test vehicle for planarization.

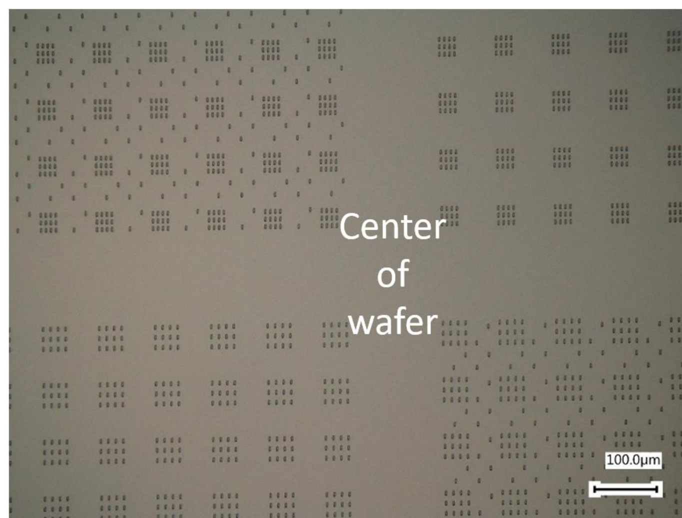


Figure 2.6.2. Micrograph of fabricated sample after planarization.

The final process conditions required to planarize the wafer are given in Table 2.6.1. Planarity was first measured with a Veeco Dektak 6 stylus profilometer, and then confirmed with AFM, which is presented in Figure 2.6.3.

Table 2.6.1. Process conditions for CMP for planarization of 3 µm PECVD oxide on test pattern from Figure 2.6.2. CMP was performed on a G&P Poli-400L. The polishing slurry was Unicol 50 from Universal Photonics, diluted 1:1 with DI water. Slurry pump rate was ~45 mL /min. A 30 second DI water rinse follows the last step that maintains the same pressures and speeds but stops the flow of slurry and instead sprays DI water to remove debris and slurry particles from the wafer surface.					
Step	Wafer Pressure (g/cm^2)	Ring Pressure (g/cm^2)	Platen Speed (RPM)	Head Speed (RPM)	Time (s)
1	170	210	70	75	300
2	70	100	70	73	30
3	30	60	70	73	30

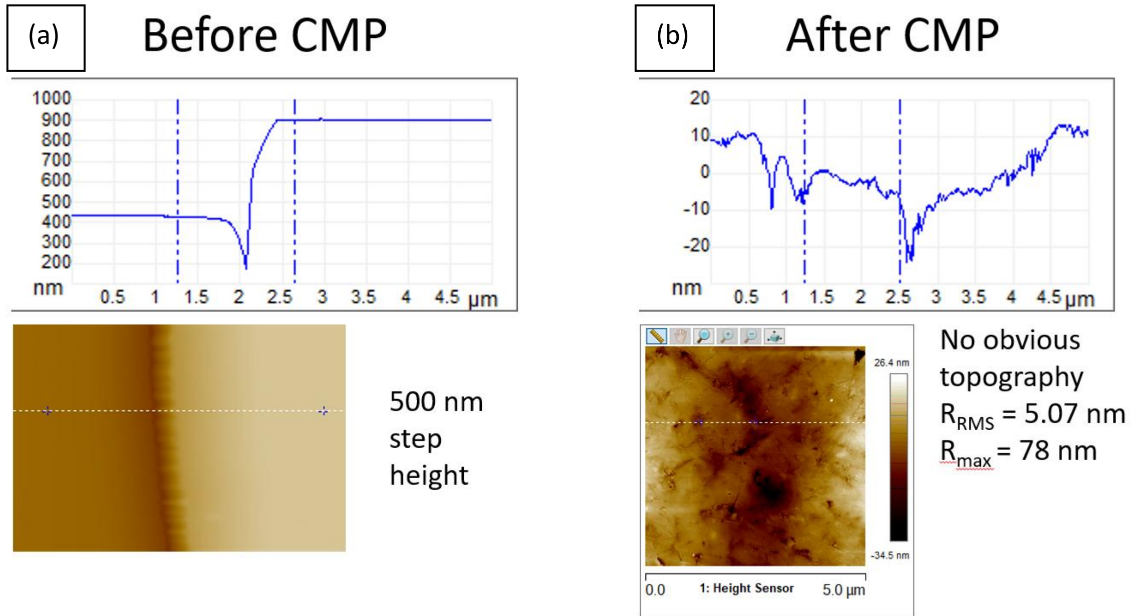


Figure 2.6.3. AFM scan measuring topography at the edge of the test structure.
After CMP, there was no topography on the sample (measured at the edge of the test structure), demonstrating that the sample had been planarized.

2.7. Heterogenous Integration of Multiple Dielets onto Large Substrate

Incorporating the results of the previous learnings, Figure 2.7.1 illustrates the final experimental process flow. Further improvements to this are suggested in Section 4.

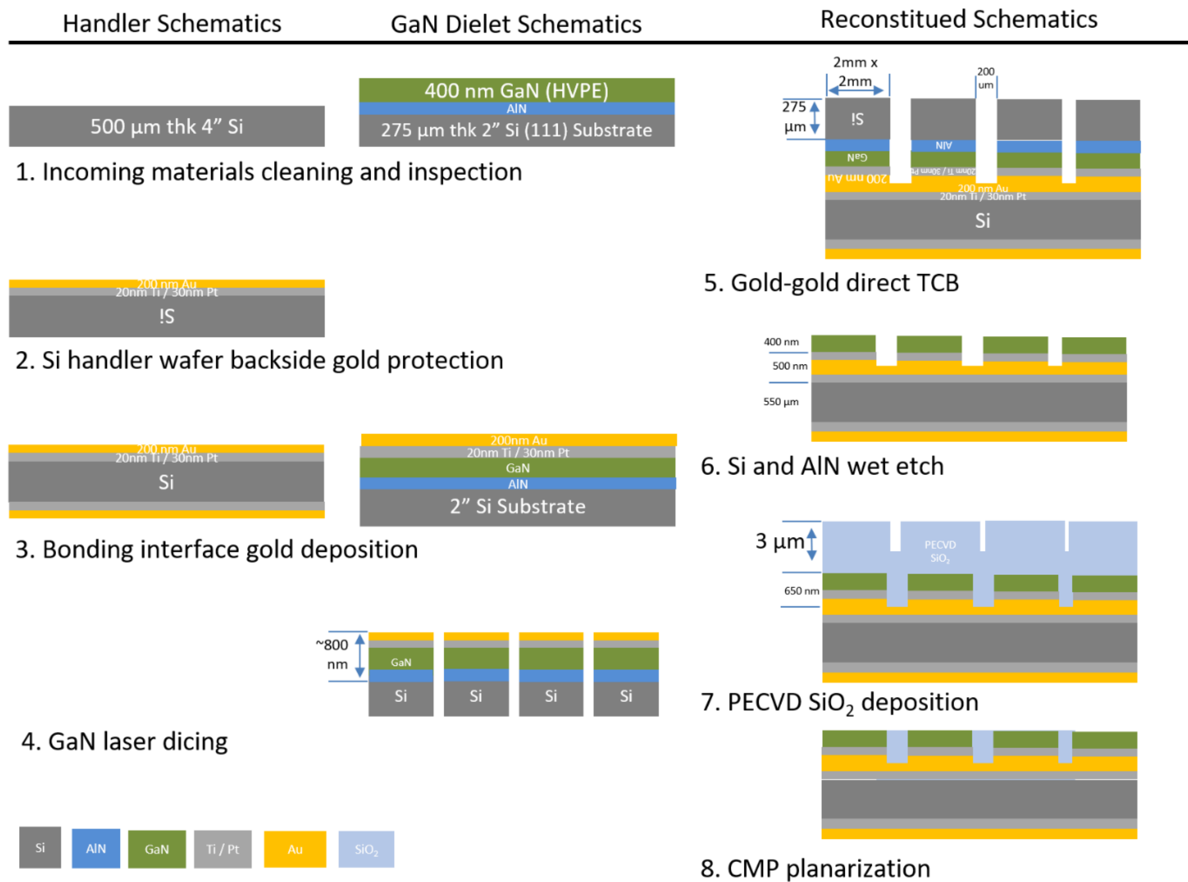


Figure 2.7.1 Final experimental process flow for fabrication of a reconstiuted large III-V wafer.
Steps 1-4 are shown as occurring in parallel for the dielet material and the handler wafer. By step 5 they are bonded together, and the process flows merge.

A total of 52 GaN dielets were bonded to the 4" wafer. A 6x6 grid of dielets were bonded in the center to mimic the local environment of a fully reconstituted wafer. At each of 4 edges of the wafer, 4 additional dies were bonded to understand additional considerations (if any) for dielets bonded to the edge of a reconstituted wafer. This is also an effective means to collect data to further adjust the CMP parameters, as the two zone (edge and center) wafer pressures can be adjusted independently. Images of the assembled sample are presented in Figure 2.7.2. All dies were inspected, and no visible cracking of Si could be observed with optical microscope using darkfield illumination.

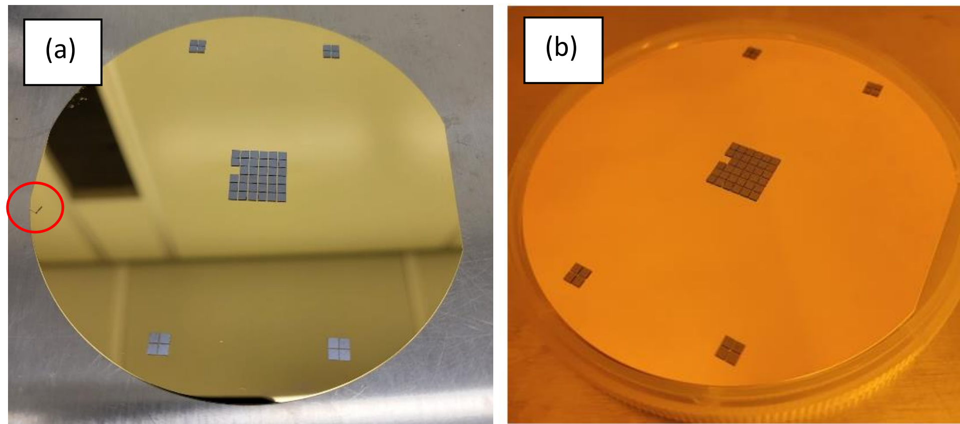


Figure 2.7.2. Images of assembled reconsituted wafer.
(a) one die is missing from the 6x6 grid. Likely due to some debris at the site, no bond was made. The die can be seen at the edge of the wafer in the left image. Three other bond sites were found to be defective when dies immediately unadhered after submersion into HNA etchant. (b) the same sample under different lighting.

Next, samples were immersed in HNA 123 solution for approximately 2 hours. Figure 2.7.3 shows a photo of the reconstituted wafer after etching. Because the GaN is highly stressed when it is grown, after etching some of the GaN is cracked or flaked off. The protective gold on both the top and bottom of the Si handler wafer is found to be completely intact. No pinholes were observed. The only visible defects are from scratches that were caused by tweezer handling. The ~200 nm thick AlN buffer layer was determined to be etched away by HNA based on stylus profilometry measurements.

Next, PECVD oxide was deposited. Unfortunately, the first deposited 3 µm thick film completely peeled due to excessive stress buildup, as depicted in Figure 2.7.4. Remnants of the delaminated film were mechanically removed with a cleanroom wiper and high-pressure DI water rinse to attempt rework. A different PECVD tool was used, and oxide was successfully deposited on the surface.

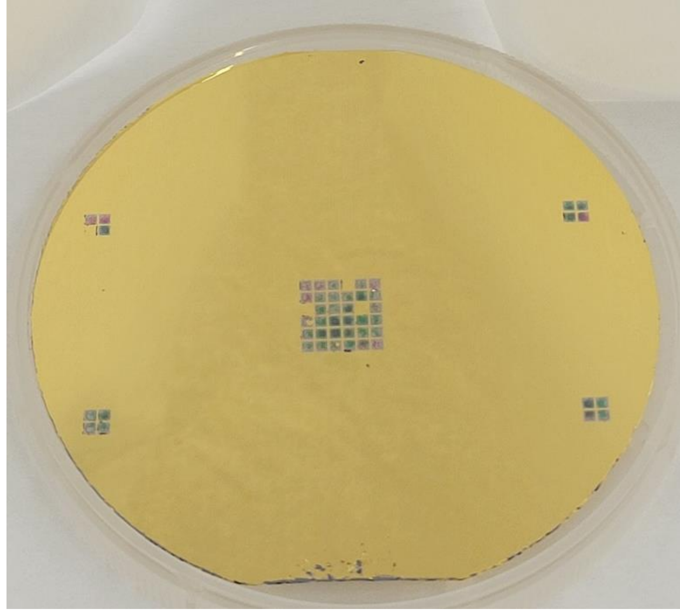


Figure 2.7.3. Reconstituted wafer after HNA etching.
Gold delamination and subsequent silicon etch can be seen primarily at the bottom of the wafer near the primary flat.

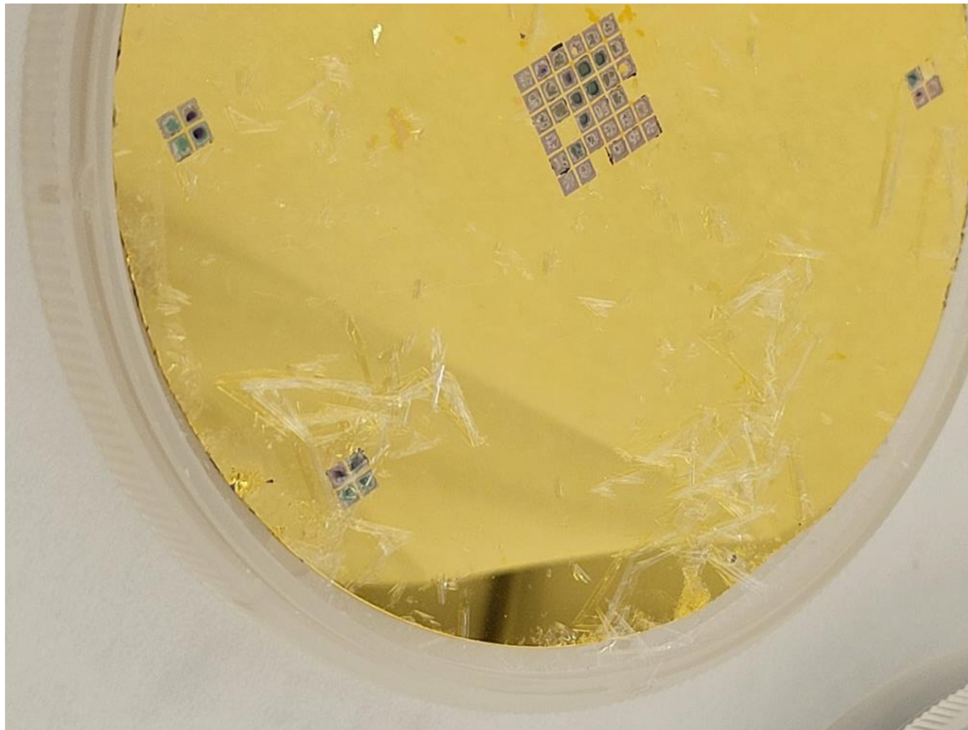


Figure 2.7.4. Peeling of PECVD SiO_2 deposited film.

Finally, CMP was performed on the sample to planarize the surface. Figure 2.7.5 shows a photograph of the sample after CMP. Good uniformity is observed across the majority of the wafer, but the film is over polished at the center and under polished at the edges.

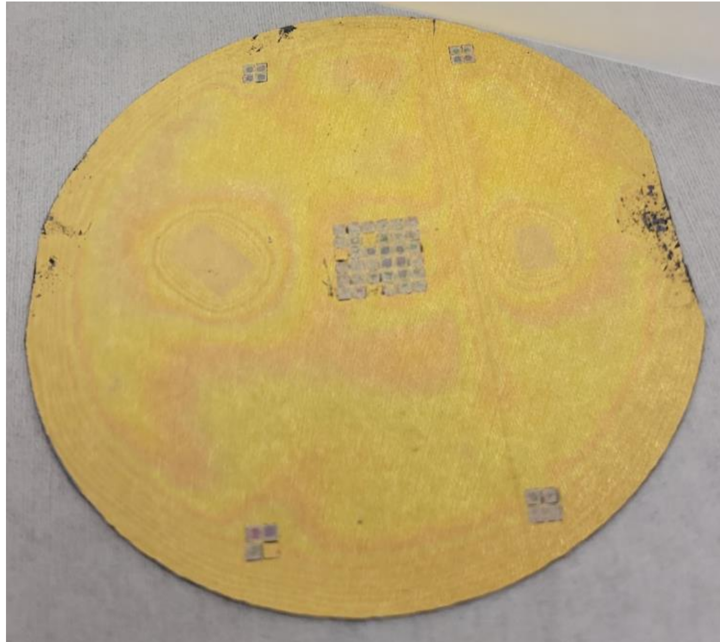


Figure 2.7.5. Photograph of reconstituted III-V wafer after CMP.
The variations in thickness of the polished SiO2 create constructive and destructive interference patterns. Two small Si pieces were placed on the wafer to measure thickness of deposited oxide, which accounts for the fringe patterns seen on the left and right of the 6x6 grid. The outline of these Si pieces (which were removed) is faintly visible at the center of the left/right fringe patterns.

Finally, a stylus profilometer can be used to measure the planarity of the sample. Unfortunately, the combination of cracking of the die, the failed PECVD deposition, and the nonuniformity resulting from the CMP, the sample could not be completely planarized. Figure 2.7.6 shows profilometry scan data. Aside from the negative spike at x = 200 µm, other negative peaks are a result of GaN cracking and delaminating, which is exacerbated by mechanical force from CMP. Ignoring these two detriments, the difference between the PECVD oxide covered gold “field” and the top of the GaN was only around 100 nm. Without PECVD oxide and CMP, the height difference should have been greater than 650 nm.

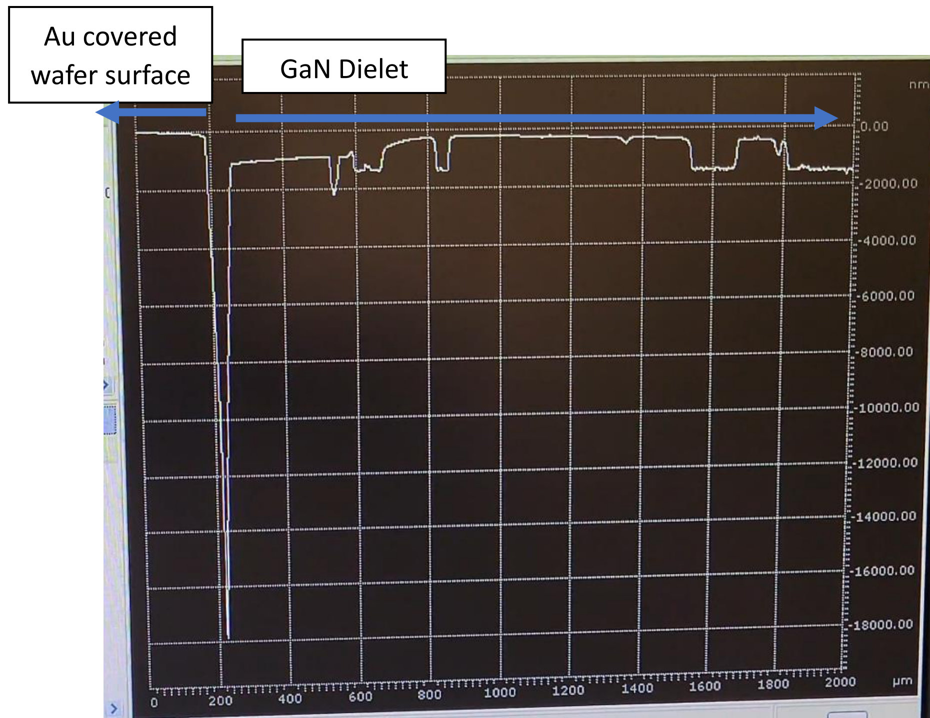
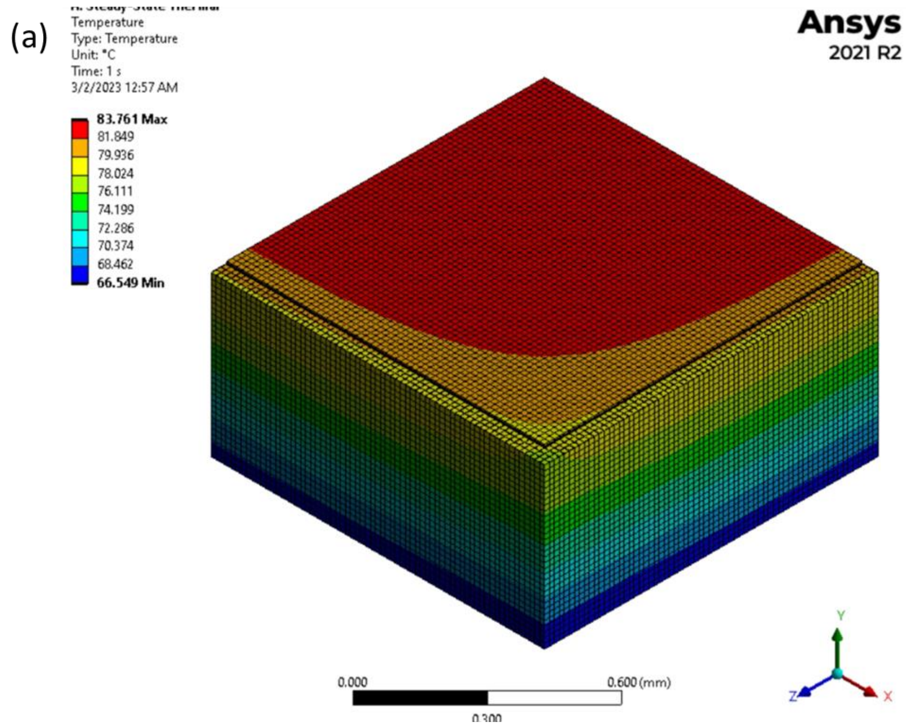
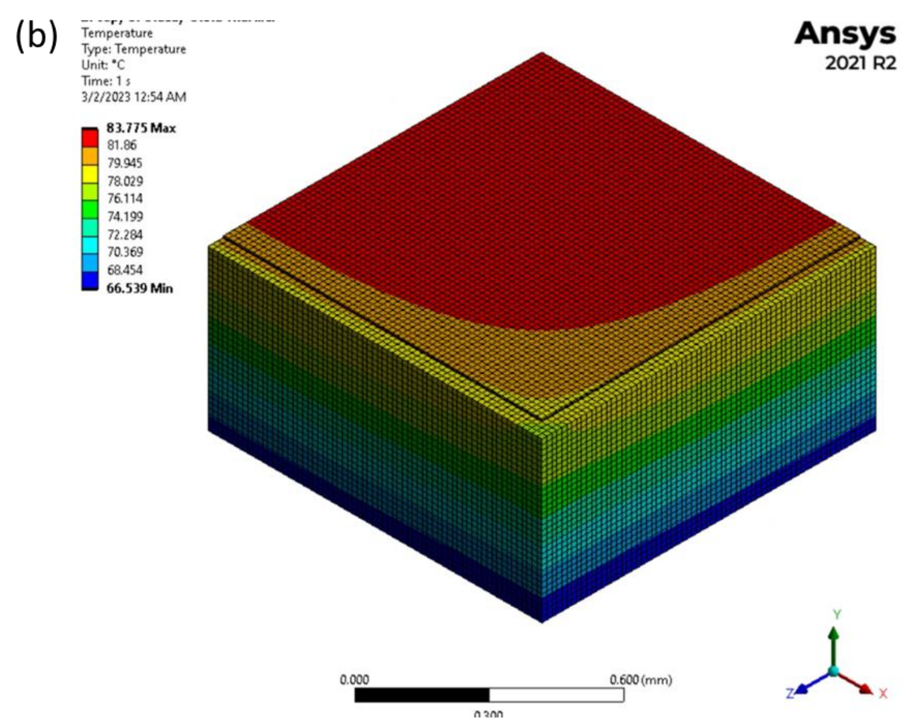


Figure 2.7.6. Stylus profilometer scan data of transferred GaN film.
The sharp negative spike at x = 200 µm is a result of gold delamination at the corner of the GaN die, resulting in slight Si etch.

2.8. Thermal Simulations

Finite element analysis simulations of the thermal performance of the reconstituted wafer was performed in Ansys. Analogous to the experimental samples, the simulated model also consisted of 2 mm x 2 mm GaN bonded to a Si wafer using a thin 200 nm Au interface. A quarter model of the transferred dielet was modelled due to symmetry. The four vertical boundaries of the Si are set as adiabatic interfaces from the assumption that the modelled part is surrounded by other similar dielets (i.e. it is not at the edge of the reconstituted wafer). The bottom of the Si substate was assumed to be heatsinked, which is modelled by forced convection with a film coefficient of 0.1 W / °C mm^2 and an assumed ambient temperature of 22 °C. The last specified boundary condition was a constant 5 W / mm^2 generated in the GaN film. This represents heat generation during device operation. Figure 2.8.1 shows thermal simulations for different GaN systems.


(a)
Temperature
Type: Temperature
Unit: °C
Time: 1 s
3/2/2023 12:57 AM
83.761 Max
81.849
79.936
78.024
76.111
74.199
72.286
70.374
68.462
66.549 Min
Ansys
2021 R2
0.000
0.600 (mm)
Y
Z
X


(b)
Temperature
Type: Temperature
Unit: °C
Time: 1 s
3/2/2023 12:54 AM
83.775 Max
81.86
79.945
78.029
76.114
74.199
72.284
70.369
68.454
66.539 Min
Ansys
2021 R2
0.000
0.600 (mm)
Y
Z
X

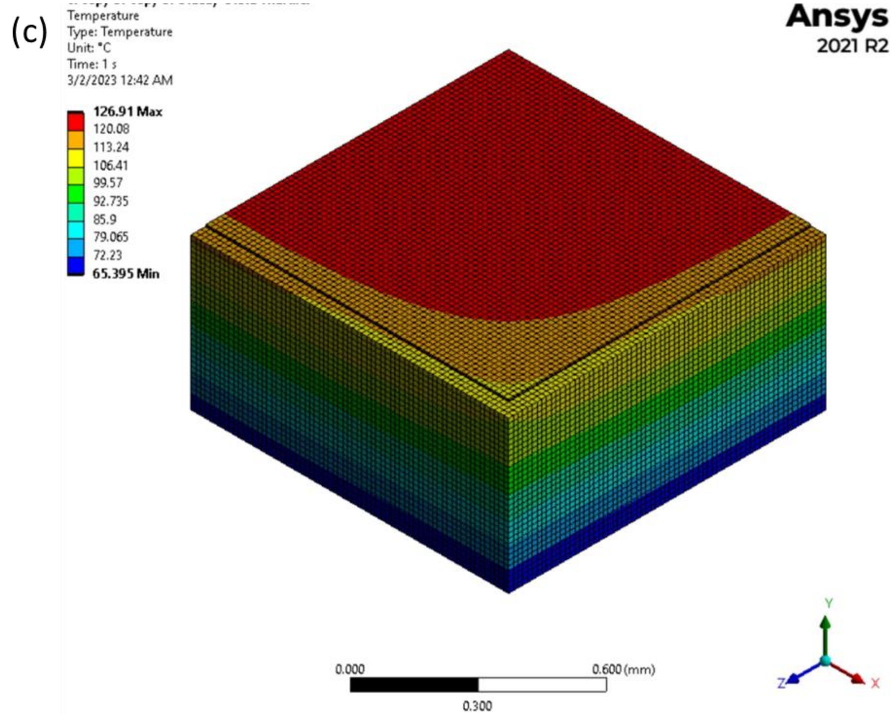


Figure 2.8.1. Finite element analysis of temperature rise in different GaN substrates.
(a) illustrates the steady state temperature of the GaN – Au – Si reconstituted wafer demonstrated in this work. (b) illustrates the steady state temperature of the GaN-Si substrate. (c) illustrates the steady state temperature of the GaN-sapphire substrate.

3. Results and Discussion

3.1. Incoming III-V Materials Selection

As mentioned in Section 2.1, GaN on silicon was chosen as the substrate for this work. However, a discussion on merits of other substrate is still valuable as it provides motivation for further research. GaN on sapphire is the highest quality, widely available form of GaN substrates. Some of the first successful work in development of blue LEDs were done on GaN on sapphire [3.1.1], and it remains to be the more popular substrate. However, it was not used due to the complexity of LLO, as mentioned in Section 2.1.

Firstly, the growth of GaN must be considered. The GaN film must be high quality because it will be the template for subsequent epi growth. To grow a GaN with minimal defects, the film must be as unstressed as possible during and after growth. Lattice mismatch plays the most significant role in the generation of dislocations in grown films. GaN has a hexagonal close packed (HCP) crystal lattice, which rules out the ubiquitous FCC (100) silicon surface. Silicon can be still be used, but the wafer must be cut on the (111) face. Sapphire, a HCP material, is the more common substrate. It is typically cut on the c-plane (0001 plane) and (0001) GaN is grown on this facet. Both silicon and sapphire have large lattice mismatches with GaN and it was previously assumed that such a strained system could not produce a usable film [3.1.2].

The second consideration is matching the coefficient of thermal expansion (CTE). Whereas the lattice mismatch dictates the strain and quality of the film, the CTE dictates the temperature stability. It is best to have no CTE mismatch between GaN and the foreign substrate. Large swings in temperature creates immense stress and may cause the GaN film to delaminate or crack upon cooling down after epi growth.

The third consideration is thermal conductivity. Because GaN is grown on a foreign substrate, there will be nonuniform temperature gradient across the thickness of the substrate. Sapphire is thermally insulating, which makes temperature control of the GaN thin film difficult. Backside heating (e.g. for RTA

or PECVD) and cooling (e.g. ICP) will be adversely affected. These three factors are summarized in Table 3.1.1.

Table 3.1.1. Properties of selected III-V substrates.					
Material	a Lattice Constant (Å) [3.1.3]	Lattice Mismatch vs GaN (%)	CTE (ppm/°C) [3.1.3]	CTE Mismatch vs GaN (%)	Thermal Conductivity (W/mK) [3.1.4] [3.1.5]
GaN	3.19	-	5.6	-	230
Silicon	5.43 3.84 (effective)	20	2.6	54	130
Sapphire	4.758 2.747 (effective)	14	7.5	34	30

The rocking curve scan presented in Figure 2.1.1 shows a broad peak of about 1700 arcsec FWHM. This indicates a mediocre GaN quality that has a low degree of crystallinity or has high dislocation density. It is expected that subsequent epi growth would suffer because the GaN film is not as crystalline as ideally possible. Experimental work to validate or reject this hypothesis is out of the scope of this thesis. The stress state in the GaN can be determined using XRD to measure the lattice spacing, and by comparing shifts in the peak, the native stress of the GaN on Si samples and the stress after reconstitution can be determined. After the GaN dielet is flip-chipped and the Si substrate is etched away, the gold must provide the necessary force to keep the GaN in equilibrium. If the gold cannot, then the GaN will likely contract (based on the difference in lattice constants) and may crack (depending on the forces).

3.2. Si Removal

Incomplete Si etch was observed in some areas of the fully reconstituted sample. Although etch rates were measured to be high at the start of the etch, it is unclear how the etch chemistry changes over the course of hours. It is also unclear how temperature gradients from the exothermic reaction and component densities affect the etch rate. For safety, HNA solution was not agitated, but future work should investigate whether agitation of the solution can improve uniformity, which would reduce or eliminate the topography of the Si islands, as seen in Figure 2.3.1.

3.3. Substrate Backside Protection

On the bulk of all samples, no pinholes or etching was observed. However, at the bottom of all samples, minor etching occurred. This is likely due to overly aggressive handling with metal tweezers which may have delaminated the gold film. Figure 3.3.1 shows an image of a sample with delaminated metal and corroded Si at areas that are touched by metal tweezers during manual handling. Figure 3.3.1 also illustrates corrosion at the left edge of the sample. This was due to cleavage of the wafer after gold deposition. During the breakage, the gold likely delaminated from the top, leaving microscopic regions unprotected. That, combined with the lateral etching through the depth of the wafer created macroscopically visible defects. Thus, gold is chosen as the layer to protect Si from HNA etching where not desired.

Figure 3.3.1. Corrosion of underlying silicon due to gold film discontinuities.
Slight corrosion of the sample is also visible at the left edge. The bulk of the sample (both the gold film and the silicon wafer) is intact after two hours of HNA submersion.

3.4. Dicing Development

Parts received from laser cutting were still intact as one piece, but easily fractured during handling. The laser cutting was aligned as close as possible to the major flat, but because the substrate is (111) the

fracture surfaces may not always cleave cleanly. However, the laser cutting already ablated away the majority of the thickness of Si, so even if fracture occurred on mishap planes, the irregularities of the backside of the die is negligible.

This issue can be entirely avoided by reducing the number of laser cut repetitions from 16. This will make the remainder of the Si thicker and stronger, and will require post processing using a dicing saw to completely singulate parts. This will also require an increasing of the laser cut kerf to at least 150 µm to allow for a dicing saw to pass through the groove without contacting the pristine laser cut edges.

Dielet size was primarily chosen as 2 mm x 2 mm due to historic experience with dielets of this size. Additionally, the 2 mm x 2 mm size falls within Iyer's suggestion for the golden dielet regime (between 1 – 100 mm^2) [3.4.1]. Section 3.7 elaborates on additional considerations required to choose dielet sizes. As seen in Section 2.7 (specifically Figure 2.7.3), there is some cracking of the GaN, but there are large pieces that are close to 2 mm length, so the choice of dielet size is valid from the context of stress.

3.5. Dielet Bonding

This work relied on long bond times, which may not have been necessary. With bond arm temperatures of 300 °C and chuck temperatures of 100 °C diffusion and plastic flow of gold typically will occur in under 10 seconds, so a 60 second bond time is unnecessary. However, longer bond times typically show fewer t_0 defects, and so to maximize yield, bond times were maximized.

Because all shear forces were sufficiently high, it was decided to minimize bonding pressure to reduce likelihood of damaging the thin GaN surface. The Karl Suss SB-8e alone cannot be used for bonding because it does not offer any alignment unlike the Apama's alignment accuracy of up to 1 µm. The SB-8e was also not used for gang bonding because of concerns of differences in die thickness and global planarity issues. Figure 3.5.1 illustrates this concern. If all dies are the exact same thickness, the SB-8e can apply uniform force across all dies, and if this force is within a safe range, no cracking will occur. However, if the substrate is warped, dies are of slightly different thickness, or the top chuck is not compliant enough, more

force will be applied to the tallest features (like the die on the left), and little or no force will be applied to the shorter dies. This can cause cracking of the tallest dies and/or no bonding of the shorter dies. Because the uniformity of the as-received GaN-Si sample is unclear, the safest route is to avoid gang bonding altogether. If the thickness of the GaN dielets is known precisely, then gang bonding can be used to reduce TCB time and to significantly increase bonding strength. Gang bonding may also improve yield by deforming the gold sufficiently to plastically flow around any small particles (which were the cause of yield loss seen in Fig. 3.1.4. Such high forces are not possible on the Apama.

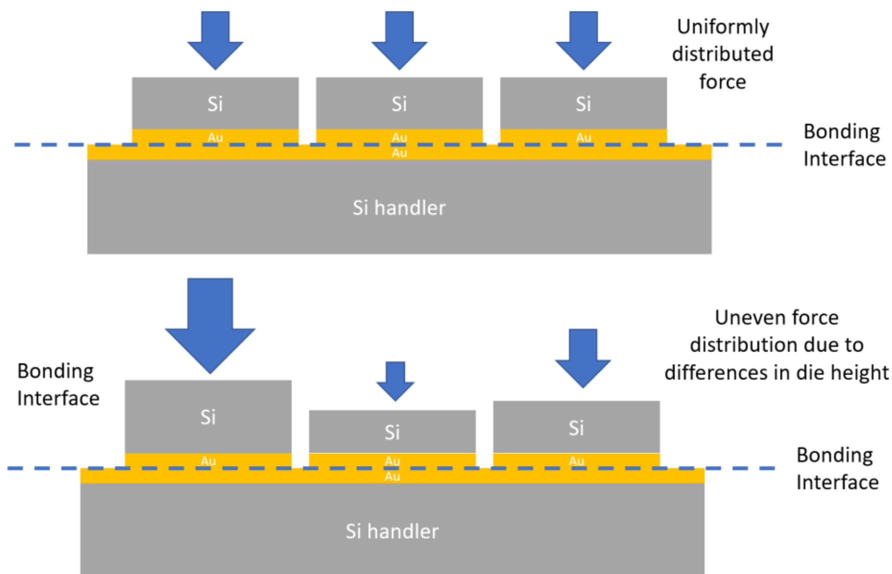


Figure 3.5.1. Schematic illustrating problems arising from variations in die thickness.

The use of gold as a bonding layer in silicon may be alarming because gold is a known deep level trap generator in Si. These defects greatly decrease the lifetime of carriers and destroy any active devices present. However, in this work, Si is only used as a handler, so diffusion of gold into the Si is not a critical concern. The structures in this work used a 30 nm Pt layer was used as a diffusion barrier, however its efficacy was not carefully studied. In this experiment the substrate experienced temperatures between 150 °C and 300 °C for only a few seconds, so diffusion is limited. However, the subsequent step of the reconstituted wafer would be to grow epi, which would require temperatures of ~ 600 °C for MOCVD. This

is a huge challenge for any diffusion barrier layer, as the diffusion coefficient will increase exponentially with an increase in temperature. In addition to the Pt used in this work, other contemporary diffusion barriers including titanium nitride, tantalum nitride, tungsten, and cobalt need to be tested to ensure that brittle intermetallics do not form, which would pose mechanical reliability concerns.

Different integration challenges will arise if attempting to use this work's techniques to bond III-V dielets onto an active silicon wafer. The III-V material must be face-to-face flip chip bonded. Bonding face to back, like the work presented in this thesis, and subsequently growing epi is impossible because the MBE and MOCVD temperatures will destroy any devices on Si. Therefore, the III-V must be fully fabricated with BEOL using III-V equipment before it is attached using a face-to-face connection. This is the first challenge.

The second challenge is choosing a diffusion barrier, like what is discussed in the case of Si used as a mechanical handler. The choice of diffusion barrier is just as important despite lower TCB temperatures (compared to epi growth). The substrate will only experience temperatures between 150 °C and 300 °C for a few seconds, so the diffusion problem is inherently minimized. However, the barrier must be extremely robust because the electronic properties of devices are significantly more sensitive to gold contamination than the mechanical properties of the handler. Thus, extremely low diffusivity is required even at these moderate temperatures.

One possible solution in 3D stacking of III-V onto active Si is to avoid using Au as the TCB material. For example, copper is well established in Si BEOL and Cu TCB has been studied [1.3.3]. However, copper has its own challenges: it is etched in HNA and it grows a native oxide that must be removed prior to bonding. If no additional III-V chemical thinning is required (e.g. LLO or exfoliation), then no further processing is required and copper is immediately suitable. However, if III-V chemical thinning is required (e.g. with HNA), then the TCB attach material and the Si active wafer needs to be passivated against HNA using a material that is compatible with Si devices (i.e. not gold). Additional work is required to identify

conformal, low temperature (< 300 °C), robust films that can withstand extended exposure to hydrofluoric and nitric acid. Al_2O_3 is one such film candidate, but experimental work is needed to qualify it.

3.6. PECVD / CMP for Planarization

As evidenced by the minor topography still present in the profilometry scan of Figure 2.7.6, the CMP step was only partially successful due to the within-wafer nonuniformity. The GaN and oxide were overpolished at the center of the wafer and underpolished at the edges. Fortunately, the G&P machine has two independent pressure regions, so edge and center pressure can be independently controlled to reduce within-wafer nonuniformity.

The test vehicle presented in Figures 2.6.1 and 2.6.2 may have been challenging to polish, but the geometry of the individual features and the overall layout of the reticles across the wafer did not adequately represent the sample that was ultimately fabricated. The small 4 µm x 8 µm features were closely packed, which minimized oxide dishing in between these small features. This may be acceptable because the analogous structure in the reconstituted sample is continuous GaN, which will have no dishing. Inter-reticle spacing on the test structure was 100 µm, which is approximately the same as the inter-dielet spacing of the reconstituted sample of 200 µm. There is likely no incompatibility here either. The biggest difference arises from the uniformity of the pattern across the entire wafer. Whereas the test pattern was repeated over a 70 mm x 70 mm square, the reconstituted wafer was only uniform for a small 13 mm x 13 mm region in the center. Development of a better CMP recipe will require either removing most of the reticles from the test structure to mimic the reconstituted wafer or fully populating the reconstituted wafer so it resembles the test structure. The former is the simpler solution, but it has limited long term utility because the goal is to reconstitute a full wafer with dielets covering the entire surface.

3.7. Heterogenous Integration of Multiple Dielets on Large Substrate

There were primarily two shortcomings in this work. Firstly, the thin GaN was observed to crack. Figure 3.7.1 shows an example of a dielet with significantly cracked GaN. It is interesting to note that the

cracks are all straight lines, suggesting the cracking occurs crystallographic planes. Two causes of GaN cracking are proposed. One hypothesis is that the HNA is damaging the GaN. This can be tested by directly placing GaN dielets (with GaN exposed) into HNA solution. Figure 3.7.2 depicts the result of this. Some of the GaN appears to be cracked at the edges, initially suggesting the HNA does indeed attack the GaN. However, because the GaN is so stressed due to CTE and lattice mismatch between the Si, it can be argued the degradation of the GaN is actually the result of removal of Si. As the Si is removed, there is not enough mechanical support to endure the intrinsic strain of the GaN at the edges of the sample, causing it to crack. Thus, it can be concluded that HNA is not detrimental to GaN.

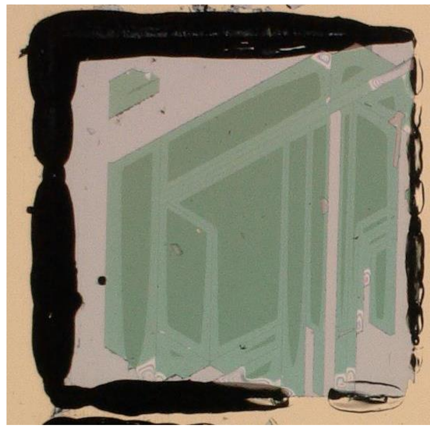


Figure 3.7.1. Micrograph of cracked GaN thermocompression bonded to a Si handler with Au-Au interface.

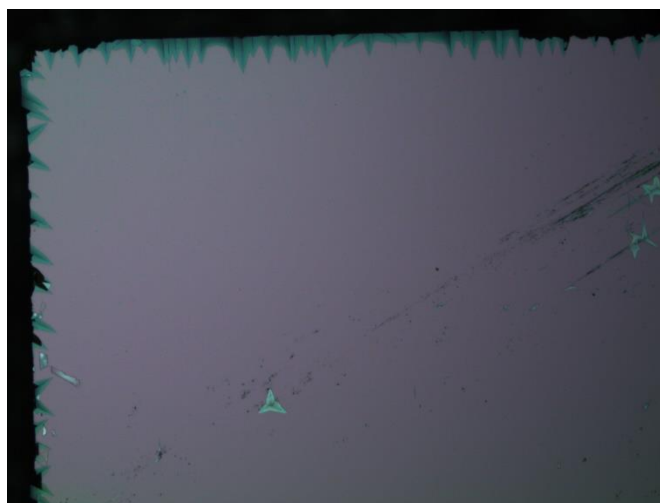


Figure 3.7.2. Micrograph of GaN surface after exposure to HNA 123 etchant for 30 min.

The other hypothesis is that the adhesion between the Si and the GaN fails. The metal layers of Ti/Pt/Au are used to bond the GaN to the Si handler. If the GaN begins to delaminate from the Ti, the stress can only be relieved through deformation with enough magnitude that the GaN cracks and flakes away. This is most likely the mechanism, as HF alone etches Ti, and the combination of HF and nitric acid etches Ti even faster. Even dilute solutions of 3% HF and 3% nitric acid were found to etch Ti at a rate of 17 µm / min [3.7.1]! Thus, it can be concluded that the Ti adhesion layer needs to be protected in future iterations to prevent GaN cracking. A solution to this problem will be addressed in Section 4.

The second concern is that the Si die was not entirely etched away by the HNA, requiring additional etch time and leading to the unnecessary exposure of GaN to HNA. This is a result of the square corners and aspect ratio of the Si feature. Figure 3.7.3 depicts the remaining Si after etching. The measured height of the remaining Si is between 5 µm to 20 µm after a 2h etch, as measured by stylus profilometer. Figure 3.7.4 schematically illustrates why this mound-like profile remains after ample Si etch. Because the etch is isotropic, HNA reacts with Si everywhere and etches in all directions at the same speed. As the etch removes material in the Z direction, Si recedes in the XY direction as well. This creates Si islands. The major concern is that the HNA is a very caustic and damaging environment, and so it can be difficult to time the etch such that all Si is removed without unnecessarily overexposing the other materials to such harsh chemicals. A solution to this problem will be addressed in Section 4.

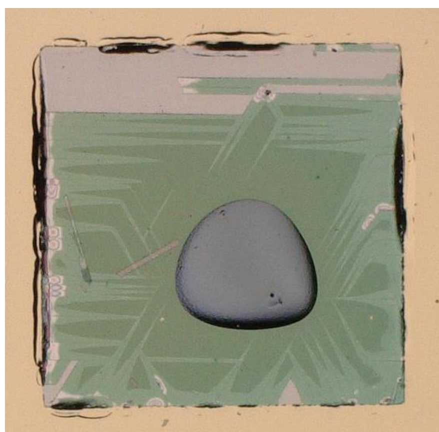


Figure 3.7.3. Micrograph of remaining Si (grey) on top of GaN film (green) resulting from incomplete HNA etch of silicon.
The GaN film is Au-Au thermocompression bonded to a Si handler. The width of the remaining Si island is about 1mm.

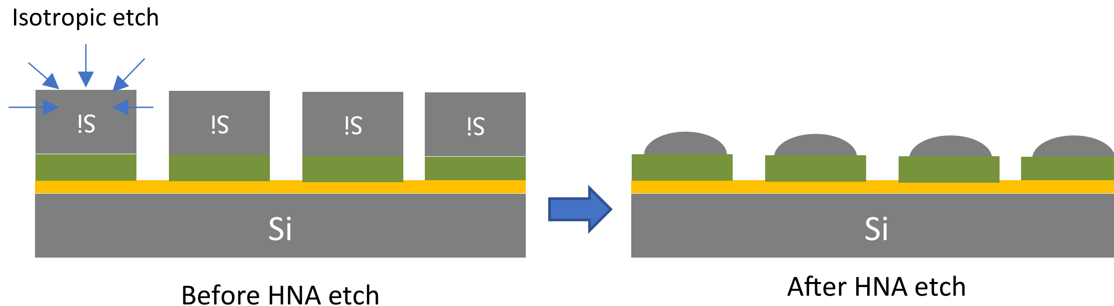


Figure 3.7.4. Diagram illustrating cause of Si islands remaining after HNA etch.

As mentioned previously, the dielet based large wafer reconstitution of GaN on Si is not necessary (because GaN can be natively grown on 300 mm Si wafers), but the techniques adapted to other III-Vs. The dielet strategy is advantageous because it enables segmentation of the substrate. Due to inherent insurmountable CTE mismatch between III-V and Si, any thermal cycling (and even the cooling of the part post-TCB) introduces stress into the assembly. CTE mismatch causes dielets to expand and contract from the neutral point, which is the center of each dielet. CTE is a dimension ratio, so larger dielets will correspondingly expand larger distances. Gold is soft and ductile, so if the adhesion between the dielet and gold is strong, dislocations will be generated as the dielet expands and shrinks which will help to relieve some of the strain.

The minimum allowable dielet size is dictated by handling concerns and mechanical practicality. Reasonable minimum values are 300 µm – 400 µm. An upper limit of allowable dielet size exists too, but the value is unclear at this point. A dielet that is too large will crack due to the CTE mismatch. This size limit is driven by reliability concerns, which is a function of the adhesion properties of the III-V to the bonding metal, the CTE mismatch between the III-V and Si, the fracture toughness of the III-V, thermal cycling range, the bond metal thickness, initial III-V stress, and any stress anneals performed. Only experimental work will be accurate enough to create a spec for this and it remains one of the future works.

Different works find the stress of such thin film bonded / thin film transferred samples to vary between 100 - 200 MPa [3.7.2][3.7.3].

3.8. Thermal Simulation

Results shown in Fig. 2.8.1 show that GaN-Si and GaN-Au-Si systems perform very similarly. This confirms intuition because the Au interlayer is thin compared to the bulk of the material (which is the Si handler). Additionally, GaN, Au, and Si are all excellent thermal conductors, so the addition of another 200 nm of Au is akin to slightly thicker GaN. As a result, it is unsurprising that GaN-Ai-Si has the same thermal properties as GaN-Si.

However, both stackups are drastically better than GaN-sapphire. For the same boundary conditions, the resulting GaN surface would be more than 40 °C warmer at steady state compared to the Si substrate. To achieve similar thermal performance, the power output of the GaN layer would have to be capped to 2.9 W / mm^2, air cooling would have to be bolstered (perhaps with additional heatsinking of liquid cooling) to achieve a film coefficient of 0.25 W / °C mm^2 and ambient temperature of the forced convection medium would need to be lowered from 22 °C to 5 °C. The simulation results clearly illustrate the shortcomings of the popular GaN-sapphire substrate. Although this substrate is typically debonded using LLO, any prior processing may be adversely affected, especially processes that occur at higher temperature. For example evaporation or PECVD conditions may be slightly different for sapphire wafers compared to Si wafers (which are typically used for process monitors). Exact differences cannot be quantified because of the wide variety of process chambers that have different thermal properties (e.g. vacuum levels, chamber size, RF network matching, etc.).

4. Future Work

Two alternative modifications are proposed to combat the issues presented in Section 3.7. The first option is to anisotropically remove Si mechanically. Figure 4.0.1 illustrates the modified steps of the process flow from Figure 2.7.1. In this new process, dies are bonded in the same manner as presented in the original process flow. However, the bulk of the silicon is then mechanically removed by CMP, lapping, or grinding. Damage to the Si dielet need not be considered, as it will be etched away anyways chemically afterwards with HNA. The advantage to this process flow is that mechanical removal of material can be very fast. Whereas the HNA chemical etchant still left Si islands after two hours, a mechanical grind of almost 300 µm may take 30 – 60 minutes and can offer better uniformity than HNA etching. The grind will only remove material in the Z direction to reduce the thickness of the silicon without any lateral change in dimension. As a result, HNA should not cause excessive recession of the silicon edge and the GaN and other materials need not be excessively exposed to HNA.

As mentioned in Section 3.7, it is unclear if there is an upper limit to the size of the dielet. It is desirable to maximize the size to minimize the number of thermocompression bonds required in the final substrate. However, the durability of differently sized dielets remains unknown. High aspect ratio (i.e. long rectangular) dielets should be possible as well, but this needs to be confirmed as well to verify there is no unexpected strain issues.

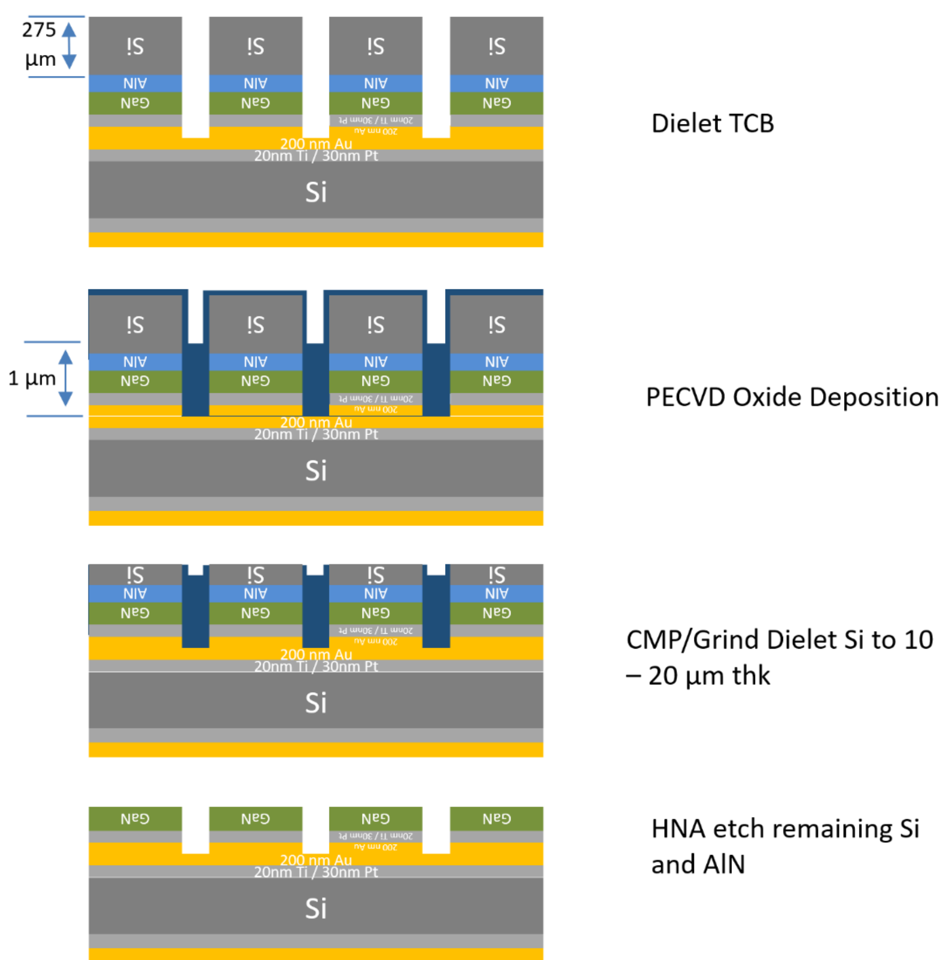


Figure 4.0.1. Modified process flow using mechanical grinding to avoid formation of Si islands.

For this process to work, the GaN dielets must be so securely bonded to the handler that the huge shear forces from the mechanical abrasion do not cause debonding of the dielets. This is likely not an issue due to the excellent bonding quality observed (that exceeded or nearly met the stringent MIL-STD-882 spec). The other concern with this process is the debris that will be formed during the grind. Debris from the abrasive medium or small particles of abraded Si may redeposit on the surface of the reconstituted wafer. One possible method of protection is to use a sacrificial layer like a PECVD oxide that is deposited prior to mechanical polishing. The sacrificial layer can be removed prior to HNA or removed in situ, as would be the case for PECVD oxide, as depicted in Figure 4.0.1 step 4. Because the height of the gap from

the top of the GaN to the gold is only 650 nm (see Figure 2.7.1), a thin 1 µm sacrificial layer will suffice to stop any debris from getting caught at the corners of the GaN dielet.

The second to alter the process flow is to use a thin ~100 nm conformal sputtered gold film to protect the sidewalls of the GaN dielet from HNA. Then, with only the top of the Si exposed, the HNA will only be able to etch in the vertical direction. Thus, the problematic isotropic etch can be made anisotropic. This method also has the added benefit of protecting the sides of the GaN and Ti from HNA etching. It was mentioned in Section 3.7 that HNA etches Ti, so sidewall protection of the dielets with Au is a simple solution to this issue. This process is illustrated in Figure 4.0.2.

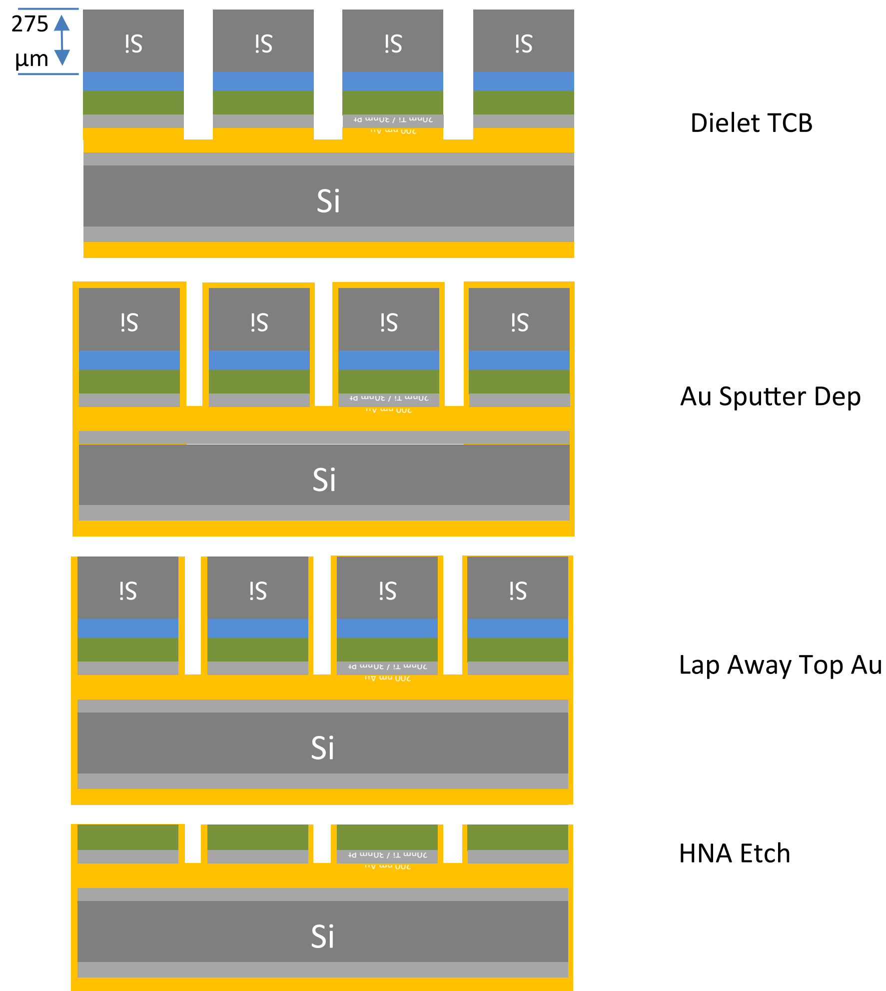


Figure 4.0.2. Modified process flow using Au sputtering to avoid formation of Si islands.

5. Conclusions

In this thesis, a new type of reconstituted III-V substrate was proposed. This work is important because it breaks ground on a radically new method of improving III-V semiconductors by improving the substrate itself. The idea of reconstitution was borrowed from Si packaging and was applied to III-V substrates to reconstitute dielets into a large wafer. Different types of attach mechanisms were investigated. Spin on glass was not found to be a feasible attach medium, whereas gold to gold thermocompression bonding was verified to be a robust method of dielet attach. Techniques were discussed to separate a thin layer of III-V semiconductor, specifically relating to removing the Si substrate from a GaN on Si dielet. Various chemistries for fast, selective Si removal were investigated, but only a mixture of 1 hydrofluoric acid: 2 nitric acid: 3 acetic acid was found to be a suitable candidate. Together, thermocompression bonding and HNA etching steps constituted a thin film transfer process. Oxide deposition and subsequent CMP to planarize the reconstituted wafer was partially successful. Overall, the process is still under development, but this work is an earnest demonstration that the technology and process are viable and promising. Alternative processes and steps were also proposed to fix some of the shortcomings in the experimental work. A combination of mechanical grinding and HNA etching can be used to quickly remove Si. Alternatively, the sidewall can be protected to minimize damage caused by HNA.

Besides the reconstitution of GaN on silicon (which is the primary focus of this work), the developed process can be applied to other III-V semiconductors as well, with slight modifications. For GaN on sapphire, the thin film transfer can be accomplished with laser lift off. For homogenous III-Vs like InP, GaAs, or free-standing bulk GaN, a thin film can be produced simply with mechanical polishing of the substrate. Another option is to use a Smartcut like exfoliation process, which can enable the reuse of costly III-V substrates.

References

[1.1.1] S. S. Iyer and Y.-H. Xie, “Light Emission From Silicon,” *Science*, vol. 260, no. 5104, pp. 40–46, Apr. 1993.

[1.1.2] T. P. Chow, “Progress in high voltage SiC and GaN Power Switching Devices,” Mater. Sci. Forum, vols. 778–780, pp. 1077–1082, 2014.

[1.1.3] T. P. Chow, “Wide Bandgap Semiconductor Power Devices for Energy Efficient Systems,” in Proc. IEEE Workshop Wide Bandgap Power Devices Appl. (WiPDA), Nov. 2015, pp. 402–405.

[1.1.4] Hua Wang, Tzu-Yuan Huang, Naga Sasikanth Mannem, Jeongseok Lee, Edgar Garay, David Munzer, Edward Liu, Yuqi Liu, Bryan Lin, Mohamed Eleraky, Hossein Jalili, Jeongsoo Park, Sensen Li, Fei Wang, Amr S. Ahmed, Christopher Snyder, Sanghoon Lee, Huy Thong Nguyen, and Michael Edward Duffy Smith, "Power Amplifiers Performance Survey 2000-Present," [Online]. Available: https://gems.ece.gatech.edu/PA_survey.html

[1.2.1] “Silicon Wafers, Silicon Wafer Processing and Related Semiconductor Materials and Services.,” *Silicon wafers, silicon wafer processing and related semiconductor materials and services.* [Online]. Available: https://www.addisonengineering.com/about-silicon.html. [Accessed: 11-Mar-2023].

[1.2.2] M. Akatsuka, K. Sueoka, and T. Yamamoto, “Classification of Etch Pits at Silicon Wafer Surface Using Image-Processing Instrument,” *Journal of Crystal Growth*, vol. 210, no. 1-3, pp. 366–369, Mar. 2000.

[1.2.3] “Silicon Wafers & Other Semiconductor Substrates in Stock,” University Wafer. [Online]. Available: https://order.universitywafer.com/default.aspx?cat=Silicon. [Accessed: 11-Mar-2023].

[1.2.4] “Free Standing GaN Crystal Substrates: Gallium Nitride Crystals,” *MSE Supplies LLC*. [Online]. Available: https://www.msesupplies.com/collections/free-standing-gan-crystal. [Accessed: 11-Mar-2023].

[1.2.5] L. Li, X. Liu, S. Pal, S. Wang, C. K. Ober, and E. P. Giannelis, “Extreme Ultraviolet Resist Materials For Sub-7 nm Patterning,” *Chemical Society Reviews*, vol. 46, no. 16, pp. 4855–4866, Jan. 2017.

[1.3.1] “InFO (Integrated Fan-Out) Wafer Level Packaging - TSMC,” *TSMC*. [Online]. Available: https://3dfabric.tsmc.com/english/dedicatedFoundry/technology/InFO.htm. [Accessed: 12-Mar-2023].

[1.3.2] K. Rahim and A. Mian, “A Review on Laser Processing In Electronic and MEMS Packaging,” *Journal of Electronic Packaging*, vol. 139, no. 3, Jun. 2017.

[1.3.3] S. C. Jangam, "Heterogeneous Integration on Silicon-Interconnect Fabric Using Fine-Pitch Interconnects (≤10 µm)," PhD. Dissertation, CHIPS, Univ. California, Los Angeles, CA, 2020. Available: https://www.proquest.com/docview/2414751535?pq-origsite=gscholar&fromopenview=true

[2.1.1] G. Ezhilarasu, A. Hanna, A. Paranjpe, and S. S. Iyer, "High Yield Precision Transfer and Assembly of GaN µLEDs using Laser Assisted Micro Transfer Printing," 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), May 2019.

[2.2.1] "Wet-Chemical Etching and Cleaning of Silicon," *Virginia Semiconductor Inc*. [Online]. Available: https://www.virginiasemi.com/?cont_uid=54. [Accessed: 11-Mar-2023].

[2.2.2] H. Robbins and B. Schwartz, "Chemical Etching of Silicon," *Journal of The Electrochemical Society*, vol. 107, no. 2, p. 108, 1960.

[2.2.3] E. S. Kooij, "Silicon Etching in HNO_3/HF Solution: Charge Balance for the Oxidation Reaction," *Electrochemical and Solid-State Letters*, vol. 2, no. 4, p. 178, Feb. 1999.

[2.2.4] W. C. Hui, "How To Prevent a Runaway Chemical Reaction in The Isotropic Etching of Silicon with HF/HNO_3 /CH_3COOH or HNA Solution," *SPIE Proceedings*, Apr. 2004.

[2.3.1] B. R. Deepu, P. Venkatachalam, F. N. Mirji, V. Littin, H. Naveen, P. Savitha, and Y. B. Basavaraju, "A Surface Micromachining: HNA Etchant for Stiction-Free Release of Micro/Nanomechanical Structures," *Materials Today: Proceedings*, vol. 42, pp. 1218–1223, Feb. 2021.

[2.3.2] C. Yang and J. Pham, "Characteristic Study of Silicon Nitride Films Deposited by LPCVD and PECVD," *Silicon*, vol. 10, no. 6, pp. 2561–2567, Apr. 2018.

[2.5.1] O. A. Shilova, "'Spin-on Glass' Films for Semiconductor Technology," *Surface Coatings International Part B: Coatings Transactions*, vol. 86, no. 3, pp. 195–202, Sep. 2003.

[2.5.2] R. F. Cook and E. G. Liniger, "Stress-Corrosion Cracking of low-Dielectric-Constant Spin-on-Glass Thin Films," *Journal of The Electrochemical Society*, vol. 146, no. 12, pp. 4439–4448, Jul. 1999.

[2.5.3] H. Clauberg, A. Marte, Y. Yang, J. Eder, T. Colosimo, D. Buergi, A. Rezvani, and B. Chylak, "High Productivity Thermocompression Flip Chip Bonding," *2015 IEEE 65th Electronic Components and Technology Conference (ECTC)*, May 2015.

[2.5.4] N. Asahi, Y. Miyamoto, M. Nimura, Y. Mizutani, and Y. Arai, "High Productivity Thermal Compression Bonding for 3D-IC," *2015 International 3D Systems Integration Conference (3DIC)*, Aug. 2015.

[2.5.5] Y.-T. Yang, "Niobium-based Superconducting Silicon Interconnect Fabric for Future Cryogenic Applications," PhD Dissertation, CHIPS, Univ. California, Los Angeles, CA, 2022. Available: https://escholarship.org/uc/item/600993hd

[2.5.6] "Mechanical Test Methods for Microcircuits," Department of Defense, vol. 2. Columbus, Ohio: Defense Logistics Agency, 2022, pp. 243–247. Available: https://landandmaritimeapps.dla.mil/Downloads/MilSpec/Docs/MIL-STD-883/std883-2.pdf

[2.5.7] Z. Gan, C. Wang, and Z. Chen, "Material Structure and Mechanical Properties of Silicon Nitride and Silicon Oxynitride Thin Films Deposited by Plasma Enhanced Chemical Vapor Deposition," *Surfaces*, vol. 1, no. 1, pp. 59–72, Aug. 2018.

[2.6.1] C.-H. Tsai, S.-R. Jian, and J.-Y. Juang, "Berkovich Nanoindentation and Deformation Mechanisms in GaN Thin Films," *Applied Surface Science*, vol. 254, no. 7, pp. 1997–2002, Jan. 2008.

[2.6.2] G. Subhash, P. Hittepole, and S. Maiti, "Mechanical Properties of PECVD Thin Ceramic Films," *Journal of the European Ceramic Society*, vol. 30, no. 3, pp. 689–697, Feb. 2010.

[3.1.1] J. I. Pankove, E. A. Miller, D. Richman, and J. E. Berkeyheiser, "Electroluminescence in GaN," *Journal of Luminescence*, vol. 4, no. 1, pp. 63–66, Jul. 1971.

[3.1.2] H. Amano, "Nobel Lecture: Growth of GaN on Sapphire via Low-Temperature Deposited Buffer Layer and Realization of p-type GaN by Mg Doping Followed by Low-Energy Electron Beam Irradiation," *Reviews of Modern Physics*, vol. 87, no. 4, pp. 1133–1138, Oct. 2015.

[3.1.3] "Low GaN Lattice Mismatch on Silicon Carbide (SiC) Substrates," *XIAMEN POWERWAY*, 26-Apr-2021. [Online]. Available: https://www.powerwaywafer.com/gan-lattice-mismatch-sic-substrates.html. [Accessed: 11-Mar-2023].

[3.1.4] GaN on Sapphire Substrates for Visible Light-Emitting Diodes. Jae-Hyun Ryou 1, Wonseok Lee 2 University of Houston, Houston, TX, United States; 2LED Business Unit, LG Innotek, Paju-si, Korea

[3.4.1] S. S. Iyer, S. Jangam, and B. Vaisband, "Silicon Interconnect Fabric: A Versatile Heterogeneous Integration Platform for AI Systems," *IBM Journal of Research and Development*, vol. 63, no. 6, Sep. 2019.

[3.7.1] R. Markle, "Etching Titanium with HF and Nitric Acid Solutions Part 1," *Chemcut Corporation*, Feb-2015. [Online]. Available: http://www.chemcut.net/wp-content/uploads/2015/02/Etching-Titanium-with-HF-and-Nitric-Acid-Solutions-Part1.pdf. [Accessed: 12-Mar-2023].

[3.7.2] W. Zhai, J. Zhang, X. Chen, R. Bu, H. Wang, and X. Hou, "FEM Thermal and Stress Analysis of Bonded GaN-on-Diamond Substrate," *AIP Advances*, vol. 7, no. 9, p. 095105, Sep. 2017.

[3.7.3] S. C. Hsu, B. J. Pong, W. H. Li, T. E. Beechem, S. Graham, and C. Y. Liu, "Stress relaxation in GaN by transfer bonding on Si substrates," *Applied Physics Letters*, vol. 91, no. 25, p. 251114, Dec. 2007.